Erase voltage impact on 0.18 μm triple self-aligned split-gate flash memory endurance

Dong Yaoqi(董耀旗)[1,2,3,†], Kong Weiran(孔蔚然)[2], Nhan Do[4], Wang Shiuh-Luen(王序伦)[4], and Lee Gabriel(李荣林)[2]

(1 Shanghai Institute of Microsystem and Information Technology, Chinese Academy of Sciences, Shanghai 200050, China)
(2 Grace Semiconductor Manufacturing Corporation, Shanghai 201203, China)
(3 Graduate University of the Chinese Academy of Sciences, Beijing 100049, China)
(4 Silicon Storage Technology Inc., 1171 Sonora Court, Sunnyvale, CA 94086, USA)

Abstract: The erase voltage impact on the 0.18 μm triple self-aligned split-gate flash endurance is studied. An optimized erase voltage is necessary in order to achieve the best endurance. A lower erase voltage can cause more cell current degradation by increasing its sensitivity to the floating gate voltage drop, which is induced by tunnel oxide charge trapping during program/erase cycling. A higher erase voltage also aggravates the endurance degradation by introducing select gate oxide charge trapping. A progressive erase voltage method is proposed and demonstrated to better balance the two degradation mechanisms and thus further improve endurance performance.

Key words: split-gate flash; endurance; erase voltage
DOI: 10.1088/1674-4926/31/6/064012 **PACC:** 7220J; 7340Q

1. Introduction

Split-gate flash memory is well-known for its high program efficiency and immunity to "over-erase"[1−4], thus attracting much research interest in recent years[5−8]. Among various split-gate flash memories, the self-aligned split-gate flash proposed by Silicon Storage Technology Inc. (SST) is widely used in standalone and embedded applications for its many advantages, including fast erase speed with low erase voltage, modular process and compatibility with the CMOS process[9−12]. It uses field enhanced poly-to-poly Fowler–Nordheim (F–N) tunnelling for erasing[13], and drain-coupling source side hot carrier injection (SSI) for programming[14,15].

Endurance is one of the flash memory's most important reliability aspects. It determines how many times the flash memory can be programmed and erased. The endurance is sensitive to the memory cell structures and fabrication process conditions. As the split-gate flash technology shrinks to 0.18 μm node, the mechanism of the cell endurance characteristics becomes more complicated. In this paper, the erase voltage impact on the 0.18 μm triple self-aligned split-gate flash endurance is investigated. Compared with previous studies[16,17], both the tunnel oxide charge trapping and the select gate (SG) oxide charge trapping are taken into consideration. It is found that an optimized erase voltage exists for a certain tunnel oxide thickness. Either lower or higher erase voltages cause more degradation, but through different mechanisms. A progressive erase voltage method is finally proposed and demonstrated to further improve the endurance.

2. Device fabrication

The flash cells used in this paper were fabricated by 0.18 μm triple self-aligned split-gate flash technology[7,8]. Compared with its non-self-aligned counterpart, a high-temperature-oxide (HTO) was deposited to form both the tunnel oxide and the SG oxide. The thickness is about 16 nm. Then, a poly-silicon spacer was formed as the SG. During erase, positive voltage was applied to the SG to facilitate poly-to-poly F–N tunnelling. The cell schematic cross-section and operation conditions are shown in Fig. 1 and Table 1 respectively.

3. Experiment results and discussion

The split-gate flash cells are cycled with different erase voltages ($V_{\rm ERS}$). As shown in Figs. 2(a) and 2(b), the best endurance performance is achieved with 12 V $V_{\rm ERS}$ for 16 nm tunnel oxide thickness. The erased state cell read current ($I_{\rm r1}$) degrades 9% (from 41.4 to 37.7 μA) after 60 000 program/erase (P/E) cycles. When $V_{\rm ERS}$ is reduced to 11 V or even lower voltage, not only does the initial $I_{\rm r1}$ decrease, but the $I_{\rm r1}$ degradation percentage also increases. However, if $V_{\rm ERS}$ is raised to 13 V, the $I_{\rm r1}$ degradation is also aggravated. The $I_{\rm r1}$ degradation sharply increases to 60% with 14 V $V_{\rm ERS}$, indicating that the degradation is very sensitive to $V_{\rm ERS}$. Furthermore, when the

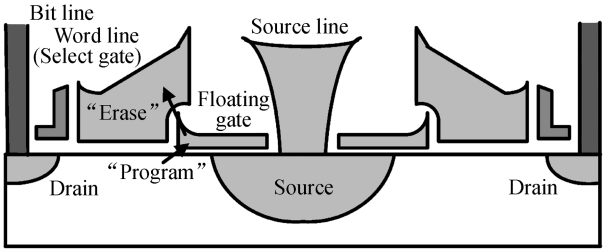

Fig. 1. Schematic diagram of cell structure cross-section.

† Corresponding author. Email: dongyaoqi@gmail.com
Received 18 December 2009, revised manuscript received 18 January 2010

Table 1. Cell operation conditions.

	Source (V)	Drain (V)	SG (V)	Substrate (V)
Program	7.4	0.6	1.6	0
Erase	0	0	11–13	0
Read	0	0.8	2.5	0

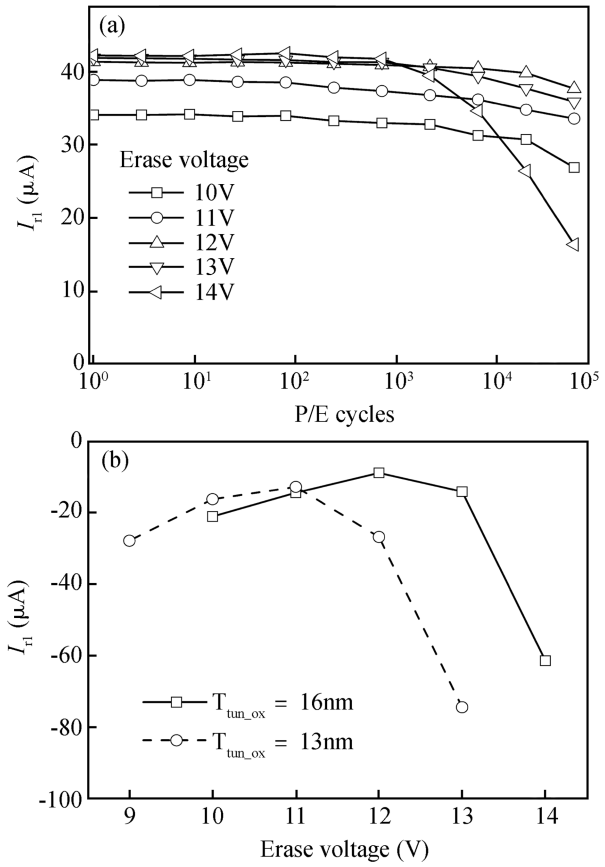

Fig. 2. (a) I_{r1} cycling degradation with different erase voltages (the tunnel oxide thickness is 16 nm). (b) I_{r1} degradation percentage after 60 000 program/erase cycles with different erase voltages. 13 nm tunnel oxide data is also shown as a comparison.

tunnel oxide thickness is reduced to 13 nm, the most optimized V_{ERS} is reduced to 11 V.

This observation is related to the split-gate structure of the flash cell, in which the cell current flows through the serially connected FG channel and SG channel during read operation. The erased FG potential keeps increasing with increasing V_{ERS}. When the FG potential is high enough, the FG channel resistance decreases significantly and the cell current becomes limited by the SG channel. Consequently, the cell current becomes insensitive to the FG potential's minor variation and tends to saturation with increasing V_{ERS}, as shown in Fig. 3.

The phenomenon that lower V_{ERS} causes more I_{r1} degradation has been explained in Ref.[12]. After P/E cycling, electrons trapped in the tunnel oxide cause erase efficiency drop and subsequent FG potential drop, which has a similar effect to applying a lower erase voltage. Points A, B, C and A′, B′, C′ shown in Fig. 3 signify the initial (cycling number = 0) and final (cycling number = 60 000) I_{cell} with V_{ERS} = 12 V, 11 V and 10 V, respectively. When V_{ERS} is reduced from 12 V, the I_{cell}–V_{ERS} curve becomes steeper thus even less tunnel oxide

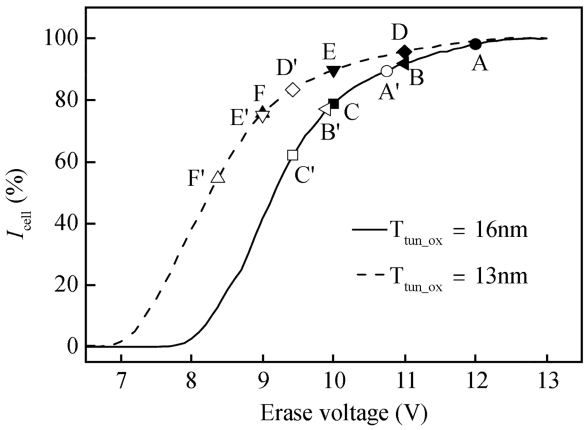

Fig. 3. I_{cell1}–V_{ERS} curves. All I_{cell} values are normalized to the I_{cell} at V_{ERS} = 13 V. The solid and open symbols denote the cell current before and after 60 000 program/erase cycles with different erase voltages respectively (A, B, C: 12 V, 11 V, 10 V; D, E, F: 11 V, 10 V, 9 V).

charge trapping causes more significant I_{r1} degradation. This explanation can also be demonstrated by points D, E, F and D′, E′, F′, which denote the initial and final I_{cell} with V_{ERS} = 11 V, 10 V, 9 V and 13 nm tunnel oxide thickness.

When V_{ERS} is increased to 13 V, the initial I_{r1} may still benefit a bit from the higher V_{ERS}. However, as the high voltage stress across the SG oxide also increases, charge trapping is more likely to be generated in the SG oxide. Moreover, because the SG voltage remains constant (equals to V_{ERS}) during the entire erase duration, the stress across the SG oxide increases directly with increasing V_{ERS}. When FG channel fully turns on and I_{r1} is mainly determined by the SG channel, the SG oxide charge trapping can cause more I_{r1} degradation.

The above explanation is verified by the I_D–V_{SG} curves. As shown in Figs. 4 (a) and 4(b), after P/E cycling with 13 V V_{ERS}, a significant threshold voltage (V_{TH}) shift is observed, whereas the V_{TH} shift is not significant after P/E cycling with 12 V V_{ERS}. This is further confirmed by the Synopsys TCAD simulation (shown in Fig. 4(c)). Cell A represents the normally erased cell, with 2.0×10^{-15} C/μm charge in the FG. Cell B has 1.2×10^{-15} C/μm charge in the FG, less than cell A, as a representation of charge trapping only in the tunnel oxide, which consequently reduces the erase efficiency. Cell C also has 1.2×10^{-15} C/μm charge in the FG, but has additionally 1×10^{12} cm^{-2} fixed electrons in the SG oxide/silicon interface, representing a cell that has charge trapping in both the tunnel oxide and the SG oxide. The I_D–V_{SG} curve of cell B is similar to 11 V V_{ERS}, while cell C is similar to 13 V V_{ERS}. The simulation result demonstrates that with 13 V V_{ERS}, charge trapping is generated in the SG oxide and causes I_{r1} degradation.

When the tunnel oxide (as well as the SG oxide) thickness is reduced to 13nm, the optimized V_{ERS} with the best endurance is also reduced, as shown in Fig. 2(b). This observation is consistent with the above discussion. From Fig. 3, the I_{r1}–V_{ERS} curve of 13 nm tunnel oxide enters a gradual region with lower V_{ERS} than 16 nm tunnel oxide. Moreover, the SG oxide charge trapping could be generated at lower V_{ERS} due to the thinner SG oxide thickness.

To further improve the endurance performance, both the tunnel oxide charge trapping and the SG oxide charge trapping

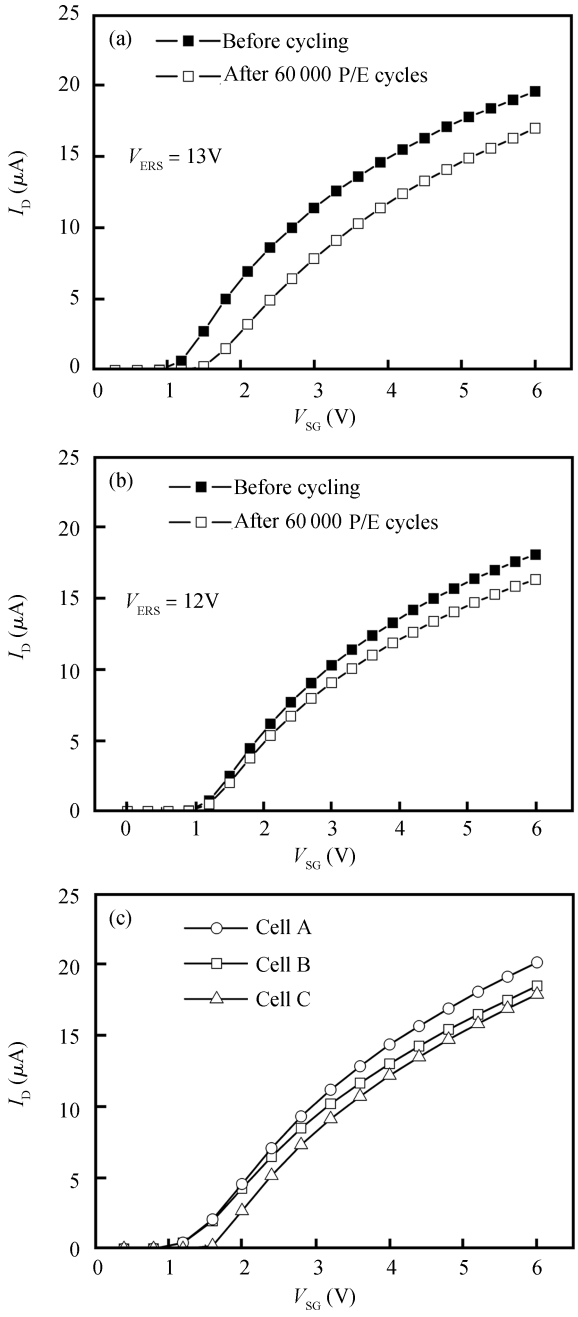

Fig. 4. I_D–V_{SG} curve comparison before and after 60 000 P/E cycles with different erase voltages. The drain is biased at 0.1 V. (a) 13 V erase voltage. (b) 12 V erase voltage. (c) Simulation I_D–V_{SG} curves with three different cell conditions. (Cell A: 2.0×10^{-15} C/μm charge in the FG; Cell B: 1.2×10^{-15} C/μm charge in the FG; Cell C: 1.2×10^{-15} C/μm charge in the FG, and 1×10^{12} cm^{-2} fixed electrons in the SG oxide/silicon interface.)

must be taken into consideration. A progressive erase voltage method is then suggested as a better balance. At the beginning of cycling, when there is no or very little tunnel oxide charge trapping, lower V_{ERS} is used to avoid over-stress on the SG oxide. As the tunnel oxide charge trapping accumulates with P/E cycling, V_{ERS} is increased dynamically to compensate the tunnelling efficiency drop and to maintain a stable FG potential. As demonstrated in Fig. 5, with an initial erase voltage of 11.5 V and voltage step of 0.1 V for every 50 000 P/E cycles, I_{r1}

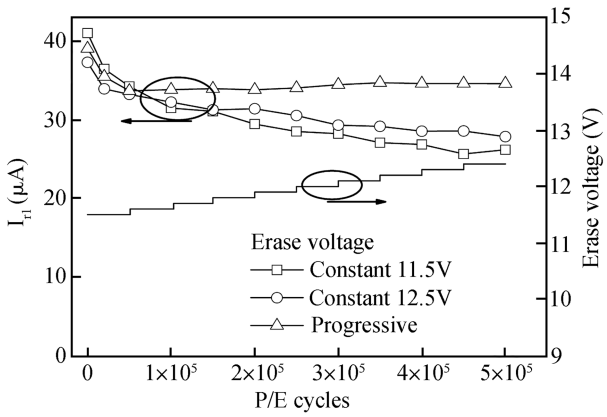

Fig. 5. I_{r1} degradation curve with the progressive erase voltage method. The erase voltage curve is also shown. The initial erase voltage is 11.5 V, and it increases by 0.1 V after every 50 000 P/E cycles.

only degrades about 10% (from 39.0 to 34.6 μA) after 500 000 P/E cycles. It is also demonstrated that this method is better than either constant 11.5 V V_{ERS} or constant 12.5 V V_{ERS}.

4. Conclusion

The erase voltage impact on the split-gate flash endurance is studied. Considering both the tunnel oxide charge trapping and SG oxide charge trapping, an optimized erase voltage is found to achieve the best endurance. A lower erase voltage causes more degradation by increasing the I_{r1} sensitivity to tunnel oxide charge trapping induced erase efficiency drop. A higher erase voltage will cause more I_{r1} degradation by introducing SG oxide charge trapping. Finally, a progressive erase voltage method is proposed and demonstrated to better balance the tunnel oxide and SG oxide charge trapping and improve the endurance performance.

References

[1] Naruke K, Yamada S, Obi E, et al. A new flash-erase EEPROM cell with a sidewall select-gate on its source side. IEDM Tech Digest, 1989: 603

[2] Houdt J V, Haspeslagh L, Wellekens D, et al. HIMOS-A high efficiency flash E^{2}PROM cell for embedded memory applications. IEEE Trans Electron Devices, 1993, 40**:** 2255

[3] Kamiya M, Kojima Y, Kato Y, et al. EPROM cell with high gate injection efficiency. IEDM Tech Dig, 1982: 741

[4] Houdt J V, Heremans P, Deferm L, et al. Analysis of the enhanced hot-electron injection in split-gate transistors useful for EEPROM applications. IEEE Trans Electron Devices, 1992, 39: 1150

[5] Cho C Y S, Chen M J, Chen C F, et al. A novel self-aligned highly reliable sidewall split-gate flash memory. IEEE Trans Electron Devices, 2006, 53: 465

[6] Shih H S, Fang S W, Kang A C, et al. High program efficiency of p-type floating gate in n-channel split-gate embedded flash memory. Appl Phys Lett, 2008, 93: 213503

[7] Wu D, Zhou F, Huang R, et al. A novel vertical channel self-aligned split-gate flash memory. Solid-State Electron, 2009, 53: 124

[8] Cao Z, Sun L, Lee E. Characterization of the triple-gate flash memory endurance degradation mechanism. Journal of Semicon-

ductors, 2009, 30: 014003
[9] Yeh B. Single transistor non-volatile electrically alterable semiconductor memory device. US Patent, No. 5029130, 1991
[10] Kianian S, Levi A, Lee D, et al. A novel 3 volts-only, small sector erase, high density flash E^2PROM. Symp VLSI Technol Digest Tech Papers, 1994, 6A(4): 71
[11] Mih R, Harrington J, Houlihan K, et al. 0.18 μm modular triple self-aligned embedded split-gate flash memory. Symp VLSI Technol Digest Tech Papers, 2000, 13(1): 120
[12] Chu W T, Lin H H, Hsieh C T, et al. Shrinkable triple self-aligned field-enhanced split-gate flash memory. IEEE Trans Electron Devices, 2004, 51: 1667
[13] Kotov A, Levi A, Tkachev Y, et al. Tunneling phenomenon in superflash cell. Proc NVM Tech Symp, 2002: 110
[14] Guan H, Lee D, Li G P. Analytical model for the programming of source side injection SST superflash split-gate cell using two-dimensional analysis. Solid-State Electron, 2004, 48: 2199
[15] Wang Y H, Wu M C, Lin C J, et al. An analytical programming model for the drain-coupling source-side injection split gate flash EEPROM. IEEE Trans Electron Devices, 2005, 52: 385
[16] Huang K C, Fang Y K, Yaung D N, et al. The impacts of control gate voltage on the cycling endurance of split gate flash memory. IEEE Electron Device Lett, 2000, 21: 359
[17] Huang K C, Fang Y K, Yaung D N, et al. Effect of substrate bias on the performance and reliability of the split-gate source-side injected flash memory. IEEE Electron Device Lett, 1999, 20: 412