A novel dual-functional MEMS sensor integrating both pressure and temperature units*

Chen Tao(陈涛), Zhang Zhaohua(张兆华), Ren Tianling(任天令)†, Miao Gujin(缪顾进), Zhou Changjian(周长见), Lin Huiwang(林惠旺), and Liu Litian(刘理天)

(National Laboratory for Information Science and Technology, Institute of Microelectronics, Tsinghua University, Beijing 100084, China)

Abstract: This paper proposes a novel miniature dual-functional sensor integrating both pressure and temperature sensitive units on a single chip. The device wafer of SOI is used as a pizeoresistive diaphragm which features excellent consistency in thickness. The conventional anisotropic wet etching has been abandoned, while ICP etching has been employed to etch out the reference cave to minimize the area of individual device in the way that the 57.4° slope has been eliminated. As a result, the average cost of the single chip is reduced. Two PN junctions with constant ratio of the areas of depletion regions have also been integrated on the same chip to serve as a temperature sensor, and each PN junction shows high linearity over −40 to 100 ℃ and low power consumption. The iron implanting process for PN junction is exactly compatible with the piezoresistor, with no additional expenditure. The pressure sensitivity is 86 mV/MPa, while temperature sensitivity is 1.43 mV/℃, both complying with the design objective.

Key words: SOI; MEMS; pressure sensor; temperature sensor
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1. Introduction

Since the discovery of pizeoresistive effect in semiconductors by Smith in the 1950s[1], this effect has been extensively used to detect physical signals, including pressure, acceleration, and strain signals, but initially in the form of stress gauges. With the development of IC technology, first pressure sensor made of bulk silicon appeared in 1971[2], and these types of sensors are called MEMS (micro-electro-mechanical system) sensors. Because of its easy batch fabrication, MEMS sensor has drawn great attention both in academic organizations and industry. For application in different circumstances, various improvements and innovations have been made to enhance the performance and reduce the volume of individual device[3, 4]. Of all these types of pressure sensors, the key processing step is the formation of the reference cave, which is usually sealed in vacuum to measure the absolute pressure. Generally, reference caves are etched by isotropic etching of bulk silicon in alkali solution. However, this technique makes the whole wafer vulnerable and unstable, because many bulk materials are removed. Another problem associated with wet etching is the resistive effect of ⟨111⟩ facet against wet etching would leave a slop of 57.4°, so the size of the mask window for etching is much larger than size of the membrane, which enlarges the average area of individual device. To overcome such problem, Wang[5] proposed a sensor whose reference cave was etched from the front side and sealed by SDB. This technique is commonly used in SOI preparation. SOI wafers are also used to manufacture pressure sensor, taking advantage of the charge insulation of the buried SiO_2 layer[6]; besides, oxide layer is also an ideal stopping layer against etching[7]. Diode has been used to detect temperature based on the proportionality of its forward voltage drop under constant current flow with the temperature. To minimize the intrinsic nonlinearity of PN junction, various solutions have been adopted[8]; one of the simplest ways is to utilize double PN junctions to cancel out the nonlinearity terms in the output voltage[9].

In some cases such as the TPMS system, both pressure and temperature data are needed, so it is necessary to design a sensor integrating both temperature and pressure sensitive units and minimize the area. ICP has been used to etch the backside of the SOI wafer. The schematic view of such a sensor is shown in Fig. 1. As can be seen, the device layer of the wafer is used as a diaphragm, which renders it possible to get highly consistent sensors over the same wafer and also among different wafers. The buried SiO_2 serves as a stop layer, and thanks to the high selection ratio between Si and SiO_2 during ICP etching, the process can be much more flexible and less demanding. Two PN junctions have also been integrated along with the piezoresistor.

2. Design theory

2.1. Pizeoresisor

The major theories related to the design involve mechanics of diaphragm, conductance of semiconductor materials, and the dependence on the temperature of the I–V characteristic of PN junction. The mechanics of diaphragm help determine of dimensions of the diaphragm under the dimensional constraint of the whole sensor. It is rather a complicated problem to calculate the displacement of square or rectangular diaphragms with edges clamped. Approximation of accurate so-

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† Corresponding author. Email: RenTL@tsinghua.edu.cn
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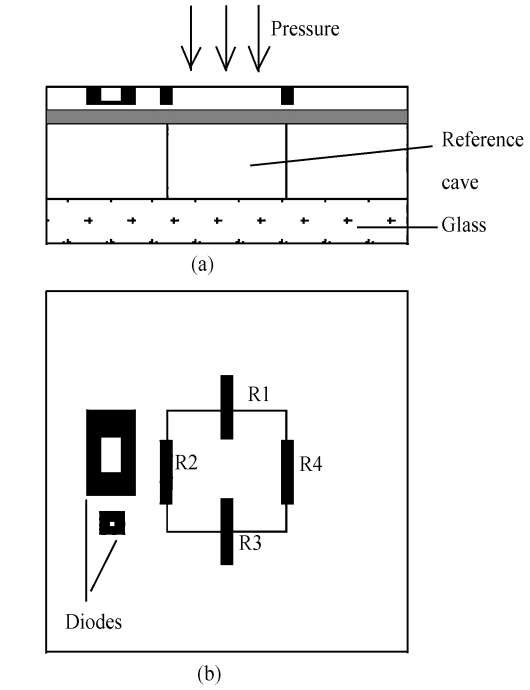

Fig. 1. Schematic view of the sensor. (a) Transverse view. (b) Top view.

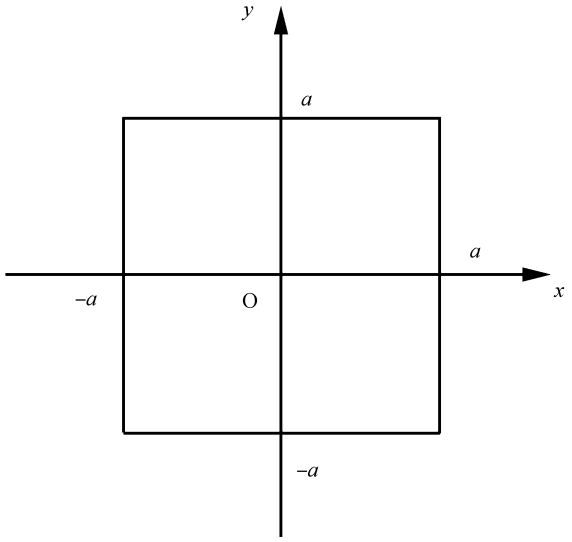

Fig. 2. A square diaphragm with edge length of a.

lutions can only be achieved by numerical analysis such as finite element method or finite differential method. There are also many approximate analytical expressions for the relations between pressure and displacement in square and rectangular diaphragms, which, however, can only express the stress far away from the clamping edges and give an qualitative intuition. For a square diaphragm shown in Fig. 2, whose edge length is a and thickness is h, the longitudinal and transverse stress over the surface are shown in Eqs. (1)–(3).

$$\sigma_{XX} = -0.51p\frac{a^2}{h^2}\left[\left(1-\tilde{y}^2\right)^2\left(1-3\tilde{x}^2\right) + \left(1-\tilde{x}^2\right)^2\left(1-3\tilde{y}^2\right)\right], \quad (1)$$

$$\sigma_{YY} = -0.51p\frac{a^2}{h^2}\left[\left(1-\tilde{x}^2\right)^2\left(1-3\tilde{y}^2\right) + \left(1-\tilde{y}^2\right)^2\left(1-3\tilde{x}^2\right)\right], \quad (2)$$

$$\sigma_{XY} = 2.045(1-v)p\frac{a^2}{h^2}\left(1-\tilde{x}^2\right)\left(1-\tilde{y}^2\right)\tilde{x}\tilde{y}. \quad (3)$$

To maximize the sensitivity and guarantee the robustness, it is expected that when imposed the full scale pressure, the maximum stress would be well below the yield stress of silicon. As the above model indicates, the largest stress locates in the central point of four edges, which is expressed in Eq. (4).

$$\sigma_{XX} = -0.51p\frac{a^2}{h^2}, \quad \sigma_{YY} = v\sigma_{XX}, \quad \sigma_{XY} = 0. \quad (4)$$

Generally, the junction depth of a piezoresistor formed by iron implanting is about 1 μm, while the thickness of diaphragm is 15–30 μm, much larger than junction depth, so it is convenient and reasonable to approximate the stress suffered by the piezoresistor as the stress expressed in the above equations.

Both the transverse and longitudinal stresses exert influences on the resistivity of a piezoresistor. As far as resistor in silicon wafer is concerned, the relative change of resistivity can be expressed as:

$$\frac{\Delta\rho}{\rho} = \pi_{\mathrm{l}}\sigma_{\mathrm{l}} + \pi_{\mathrm{t}}\sigma_{\mathrm{t}}, \quad (5)$$

$$\pi_{\mathrm{l}} = \pi_{11} + 2(\pi_{44} + \pi_{12} - \pi_{11})(l_1^2m_1^2 + l_1^2n_1^2 + m_1^2n_1^2), \quad (6)$$

$$\pi_{\mathrm{t}} = \pi_{12} + 2(\pi_{44} + \pi_{12} - \pi_{11})(l_1^2l_1^2 + m_1^2m_2^2 + n_1^2n_2^2). \quad (7)$$

In the case of P type silicon resistor which lies parallel with $\langle 100\rangle$ direction, the longitudinal and transverse are nearly the same, which render it possible to construct a fully differential Wheatstone bridge.

2.2. PN junction under different temperature conditions

PN junction is a fundamental device widely used in electronic circuit, and also used as temperature sensor. The current density J of PN junction under a bias voltage V can be expressed as:

$$J = J_{\mathrm{s}}\left(\exp\frac{qV}{k_0T} - 1\right), \quad (8)$$

$$J_{\mathrm{s}} = \frac{qD_{\mathrm{n}}n_{\mathrm{p0}}}{L_{\mathrm{n}}} + \frac{qD_{\mathrm{p}}n_{\mathrm{n0}}}{L_{\mathrm{p}}}. \quad (9)$$

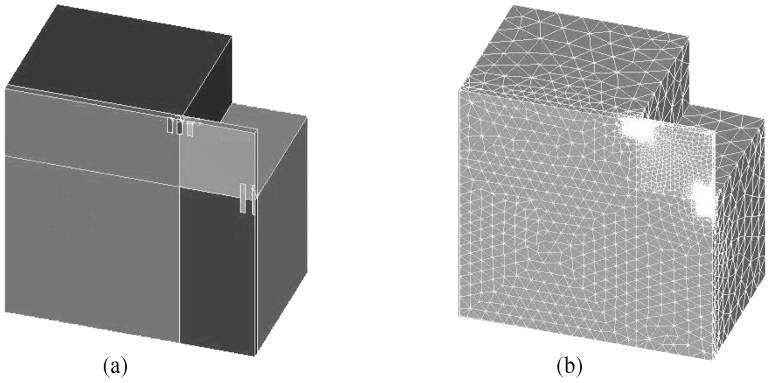

Fig. 3. (a) Quarter model of the sensor in ANSYS. (b) Meshing of the structure.

If taken into account of the temperature dependence of parameters in the J_s, then J is expressed as:

$$J = CT^{3+\gamma/2} \exp \frac{q(V - V_g)}{k_0 T}, \tag{10}$$

where C is a constant related to process, and γ also depends on process and usually takes the value between 0 and 1.

$$V_g = \frac{E_g}{q}. \tag{11}$$

Take the logarithm of Eq. (3) and do some transformation, we get:

$$V = T\frac{k_0}{q} \ln \frac{J}{C} + \left(3 + \frac{\gamma}{2}\right) \frac{k_0}{q} T \ln T + V_g. \tag{12}$$

As can be seen, the last two terms are non-linear terms, and the band voltage V_g also varies with temperature. In a small range of temperature of concern, the non-linear terms can usually be ignored. However, when large range of temperature detection is required, the non-linear effect will become very serious. To eliminate the non-linear term in output voltage, two PN junctions with different junction areas can be integrated under the same process condition. The difference of the two forward voltages under the same constant current bias is:

$$V_1 - V_2 = T\frac{k_0}{q} \ln \frac{J_1}{J_2}, \tag{13}$$

where V_1 and V_2 are the forward voltage drops of two diodes, and J_1 and J_2 are the current densities respectively. As can be seen, the non-linear terms vanish at the cost of some sensitivity.

3. Simulation

Two major parts of simulation in the design flow include the mechanical simulation and the electrical simulation. The purpose of mechanical simulation is to precisely estimate the stress distribution and optimize the parameters of structure, while the purpose of electrical simulation is to determine the dose of iron implantation. At the very beginning, certain constraints should be set up according to the design purpose. First constraint that should be complied with involves the dimensions of the sensor. To minimize the sensor so as to decrease the average cost, it is expected that the area of individual chip should be less than 1 mm. According to past experience, there should be left room for anodic bonding to seal the reference cave in vacuum. To start, we set the edge of diaphragm as 300 μm.

3.1. Finite elements analysis of sensitivity

The finite element analysis (FEM) has been employed to simulate the stress distribution in the buck sensor. The FEM model under analysis is shown in Fig. 3(a), which is a quarter model based on the symmetry of the sensor, and the whole bulk has been sectioned to enable adaptive mesh which contains minimum elements and provides enough simulation precision.

Figure 4(a) is the contour plot of stress distribution over sensor surface under full scare pressure load, which is 1 MPa. The largest stress intensity is approximately 8 MPa, 10 times smaller than the yield stress. Figure 4(b) shows the stress along the path the symmetrical axis on the surface. The result also shows that the most tensile point is at the center of diaphragm edge.

Because the piezoresistors cover a region with different stresses, to get the analytical formula of sensitivity is then impossible, and therefore can only be simulated with FEA tools. The variation of a piezoresistor can be expressed as[10]:

$$\frac{\Delta R}{R} = \frac{\pi_l \sum_{i=1}^{n} \sigma_{li} v_i + \pi_t \sum_{i=1}^{n} \sigma_{ti} v_i}{\sum_{i=1}^{n} v_i}, \tag{14}$$

where ΔR is the deviation of resistor, R is the zero-stress resistance, π_l and π_t are the longitudinal and transverse piezoresistance coefficient, v_i is the volume of the ith element, and σ_{li} and σ_{ti} are the longitudinal and transverse stress of the ith element respectively. The simulated parameters of R_1 and R_2 are listed in Table 1.

Assume that the process deviation is ignorable, and the two types of resistors are with a same resistance of R. With the above data, we are able to calculate the relative variation of the piezoresistors:

$$\Delta R_1 = -0.232R, \quad \Delta R_2 = 0.241R. \tag{15}$$

Then, the output voltage can be calculated with the following formula:

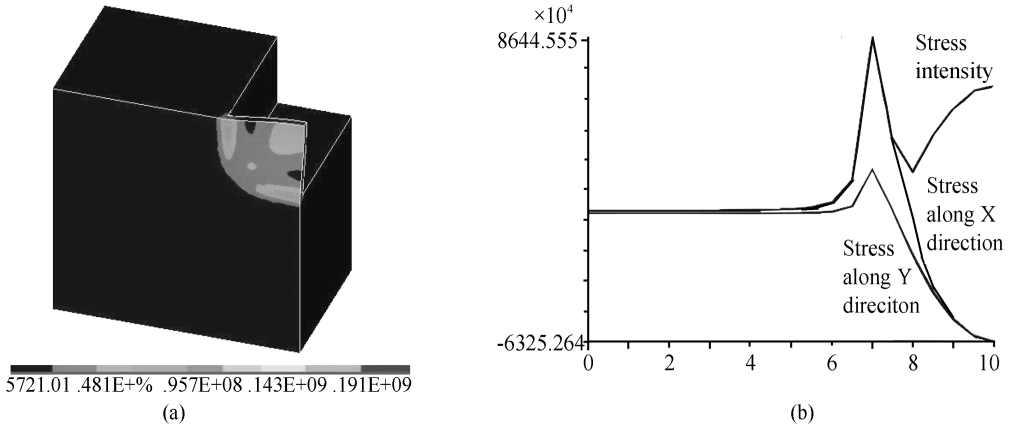

Fig. 4. Simulation results of the sensor under full scale pressure condition, 1 MPa. (a) Stress distribution over the surface. (b) Stress along the axis.

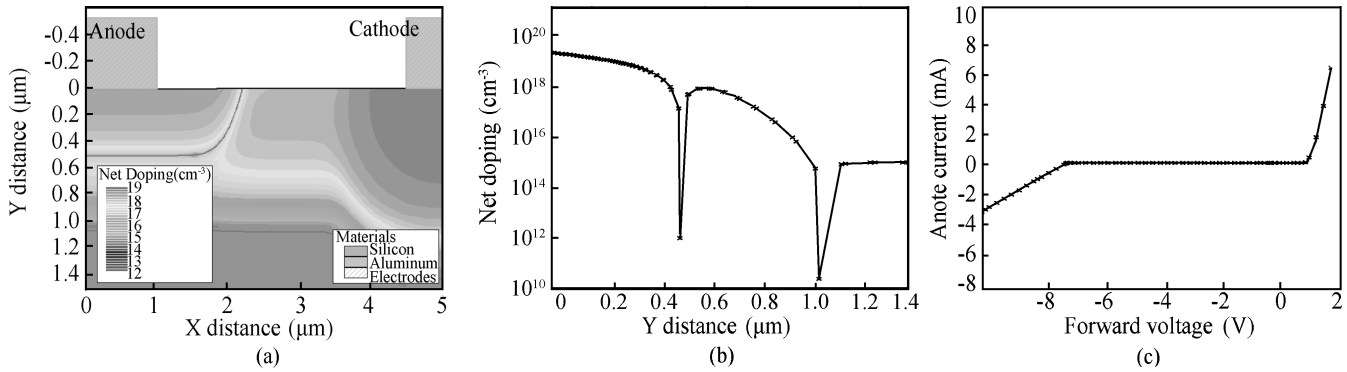

Fig. 5. (a) Athena model of the PN junction. (b) Net doping of iron along the depth direction. (c) Simulated I–V curve of the diode.

Table 1. Simulated results of the elements.

Resistor	$\sum_{i=1}^{n} \sigma_{li}\, \nu_i$	$\sum_{i=1}^{n} \sigma_{li}\, \nu_i$	$\sum_{i=1}^{n} \sigma_{li}\, \nu_i$
R_1	0.603958×10^{-7}	0.122862×10^{-7}	0.1344×10^{-14}
R_2	0.12207×10^{-7}	0.564431×10^{-7}	0.1344×10^{-14}

$$V_{\text{out}} = \frac{\Delta R_2 - \Delta R_1}{2R + \Delta R_1 + \Delta R_2} \times 3 = 0.071. \qquad (16)$$

3.2. Simulation of temperature sensor

To simplify the process flow and save cost, the PN junction is designed to be compatible with the process of piezoresistor which is p-type, so the ion concentration of p region has been confined. The only parameter remains to be determined is the dose of n-type implantation. This implantation also serves to form ohmic contact, which means that the surface concentration should surpass 10^{19} cm^{-3}.

Figure 5(a) shows the structure of the PN junction; the N^+ region is allowed to be adjusted in a range as long as a well contact is assured. Figure 5(b) is the net-doping along the cutline shown in Fig. 5(a). This figure indicates that the surface concentration is well beyond 10^{19} cm^{-3}, so ohmic contact between silicon and aluminum can be assured. It can also be seen that the junction depth of the PN junction is 0.5 μm which is less than the junction depth of P well as expected.

The I–V curve of this PN junction is shown in Fig. 5(c). From this figure, we know that the threshold voltage of diode is about 0.8 V, while the reverse break-though voltage is about –7 V.

Then the I–V curve of the PN junction was calculated with Silvaco under temperature from –40 to 120 ℃, and the data sets were fitted with nine-order polynomial for interpolation of the different forward voltage drops under the same current bias; these voltages are shown in Fig. 6(a) against temperature. Two PN junctions with different current densities were examined. The simulated results show that the temperature sensitivity is about 1.75 mV/℃. We can see that both the linearity is quite good, so we conclude that diminishing non-linearity by implementing two PN junctions would not be necessary anymore.

4. Fabrication

Figure 7 shows the fabrication processes of the sensor. As can be seen from Fig. 7(g), the wall of reference cave is nearly perpendicular to the surface, thus the area of each sensor can be reduced tremendously compared with conventional method.

The parameters of the SOI wafer include: handle wafer 400 μm, buried SiO_2 thickness 1 μm, and top Si layer 10 μm. The wafer had first been cleaned in boiling H_2SO_4+ H_2O_2 to diminish dirt and other organic contamination, and then, 5000 Å SiO_2 layer was grown to serve as a covering layer for iron implantation. Then two boron implanting processes were performed, one lightly doped, while the other heavily doped. The

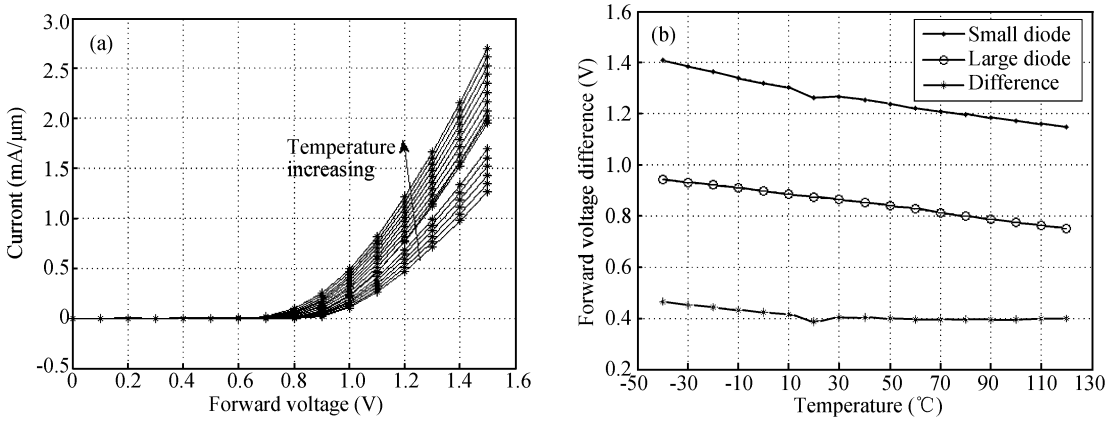

Fig. 6. Simulated temperature performance form −40 to 120 ℃. (a) I–V curve of the diode. (b) Forward voltage drop under constant current bias.

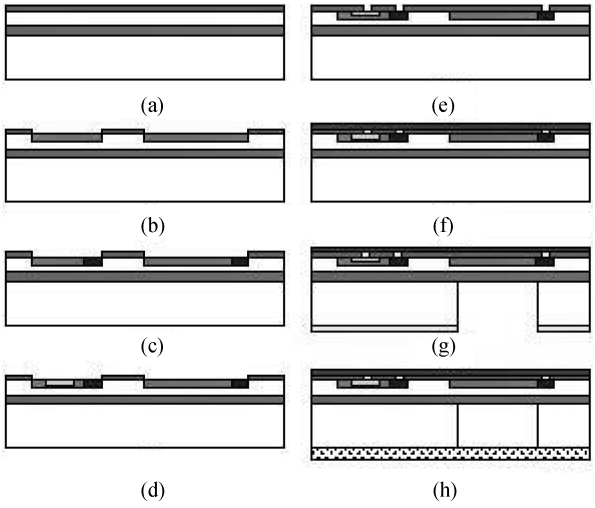

Fig. 7. Schematic view of the processing steps.

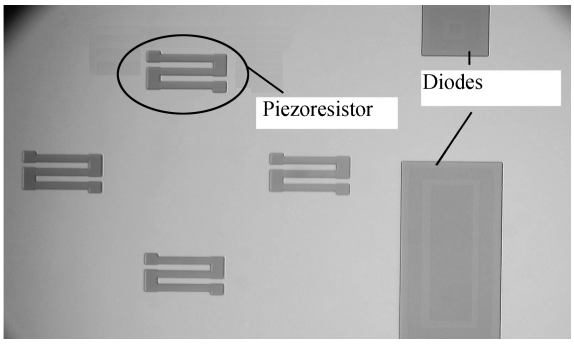

Fig. 8. Top view of the sensor after annealing after iron implantation.

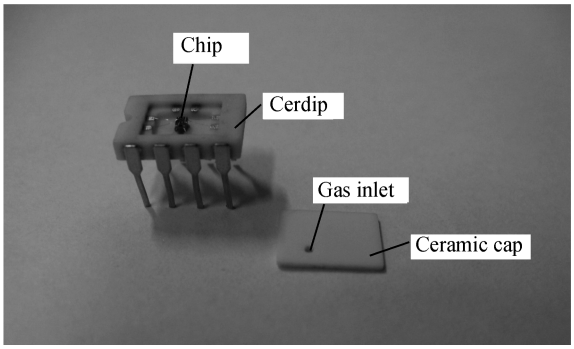

Fig. 9. Packaging of the sensor.

P doping can form the piezoresistor as well as P well of PN junction, while the P^+ doping is intended to realize a good ohmic contact with the aluminum layer. Then heavy implanting of phosphor was conducted. It should be noticed that the phosphor was implanted with a very low energy so as to get high concentration near the surface to decrease the contact resistance, and also not to penetrate the P well of temperature sensor to form an N region. The wafer was then annealed in nitrogen for 15 min, and in oxygen for 30 min to activate the doped iron. Figure 8 shows the top view photo of the wafer. Thereafter, another 5000 Å SiO_2 insulation layer was deposited by LPCVD. Prior to the deposition and etch of 1 μm aluminum which serves as the connecting wire, inverse sputtering was performed to clear the wafer surface in the via region to assure well contact. The last process on the front side was the deposition of 2000 Å Si_3N_4 passivation layer. After the processes on the front side were completed, an aluminum film was sputtered on the back side to serve as a cover layer against ICP etching, and then the pattern of diaphragm was transferred to aluminum layer by lithography and wet etching of aluminum. The buried SiO_2 proves to be a good stop layer, which plays an important role in improving the consistency among individual chips. The wafer was finally sealed by anodic bonding with Pyrex 7740 in vacuum.

The wafer was then diced, the chips were glued on a DIP-8 ceramic package, and the pads were bonded to the pins for test. The cap is also ceramic, and a hole with a diameter of 500 μm had been drilled near one corner to let gas in. The package is illustrated in Fig. 9.

5. Results and discussion

5.1. Basic electric characteristics

The resistor and diodes have first been tested with Agilen 4885 to identify some of the most important characteristics

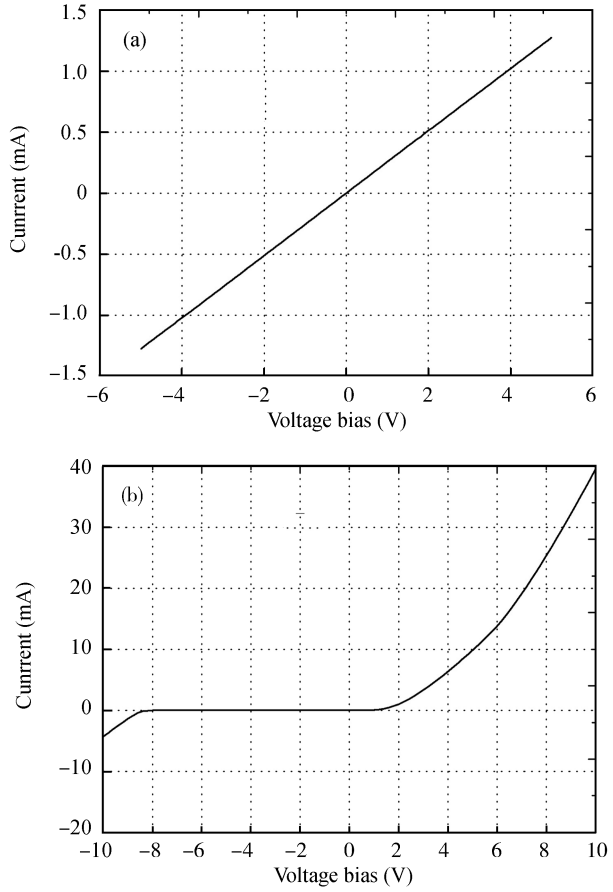

Fig. 10. Basic electric characteristics of the piezoresistor and diode. (a) I–V curve of the resistor. (b) I–V curve of the diode.

such as resistance, I–V curve, and leak current. Figure 10(a) shows the I–V curve of the resistor, from which the resistance is estimated to be 3.7 K. We can also draw a conclusion that ohmic contact has been fulfilled for the curve is almost linear, otherwise, there will be a bend near the zero-voltage point. Figure 10(b) shows the I–V curve of the diode; as can be seen, the reverse break though voltage is about –8.5 V, and the threshold voltage is about 0.85 V. The deviation from simulated results may origin from two aspects: one is the process variation, and the other is the simulation precision.

5.2. Functional performance

The instrument for test this sensor is specially designed. This equipment is mainly comprised of four parts, the high pressure nitrogen and vacuum pump make it possible to adjust the pressure in the sample chamber, while the liquid source together with filament in the chamber room are used to condition the temperature in the sample chamber. All the valves and electrical circuit are controlled by a PID controller to automatically set the temperature and pressure condition.

The sensors are placed in the sample chamber and then tested under pressure conditions from 0 to 1 MPa; the results are shown in Fig. 11. It is important to notice that the lines do not coincide with each other. They are just too close to be identified. To get a better understanding of the performance, some important parameters include full-scale output, nonlinearity, hysteresis, repeativity, and total precision are calculated

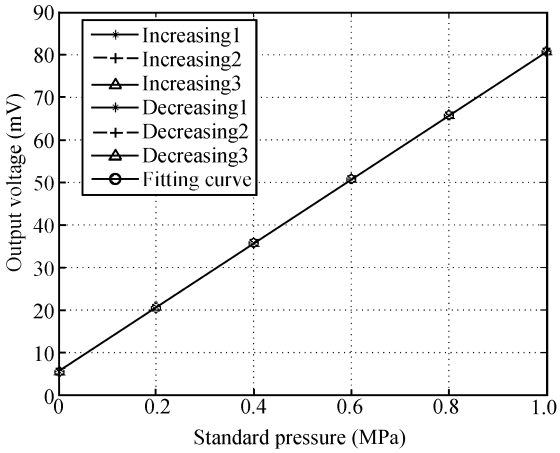

Fig. 11. Functional performance of the pressure sensor unit, tested from 0 to 1 MPa.

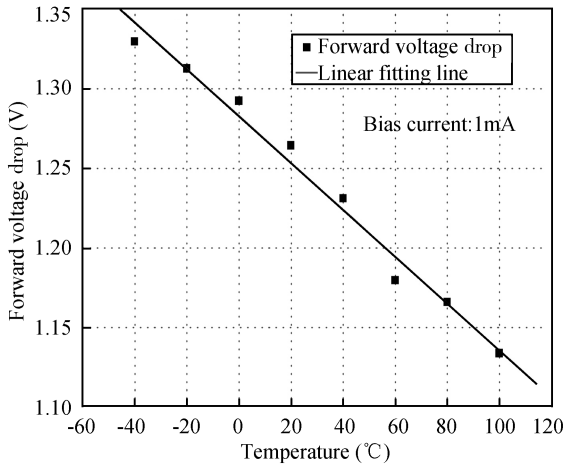

Fig. 12. Functional performance of the temperature sensor unit, tested from −40 to 100 ℃.

Table 2. Statistic specification of the pressure sensor unit.

Full scale output (mV)	Nonlinearity	Hysteresis	Repeativity	Total precision
75.1488	0.1968%	0.0472%	0.2%	0.2858%

and listed in Table 2.

The temperature sensitive unit is also tested from −40 to 100 °C; the sensitivity is about 1.43 mV/℃, less than the simulated results. As shown in Fig. 12, the points locate above or below the fitted line. This phenomenon can be explained as the system error of the characterization system. Unlike the pressure control unit, the temperature of the sample is so hard to stabilize that there is always a variation of up to 4°.The precise characterization has to be left to further work.

6. Conclusion

A pressure sensor unit and a temperature sensor unit have been integrated on a single chip; ICP etching is employed in the processing of pressure reference cave; such process proves to be efficient in reducing the average area of each sensor, which in turn decreases the cost. Test results show the following con-

ditions:

(1) ICP etch has less bulk silicon than conventional alkali etching does, and this step is arranged in the last steps of manufacturing, which allows the silicon wafer to be more robust in the flow, and has highly improved the yield of the sensor.

(2) Buried SiO_2 served as a good stopping layer against ICP etching, which left the process with more room to overcome the load effect of ICP etching which usually leads to the inconsistency of depth over the whole wafer. Because the devise layers of commercial SOI wafers are usually consistent, the thicknesses of diaphragms are nearly the same, so are the sensitivity of individual chips.

(3) The integration of the temperature of PN junction on the same chip with compatible process adds no cost and no chip area to the processing, and the performance of the single chip turns to be good. PN junctions prove to be unnecessary. The power can be controlled with the input current.

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References

[1] Smith C S. Piezoresistance effect in germanium and silicon. Phys Rev, 1954, 94: 42

[2] Samaun S, Wise K, Nielsen E, et al. An IC piezoresistive pressure sensor for biomedical instrumentation. IEEE Solid-State Circuits Conference, 1971, XIV: 104

[3] Jaeger R C, Suhling J C, Bradley A T, et al. Silicon piezoresistive stress sensors using MOS and bipolar transistors. Adv Electron Pack-ASME EEP-26-1, 1999: 219

[4] Singh R, Ngo L L, Seng H S, et al. A silicon piezoresistive pressure sensor. IEEE DELTA, 2002, 1: 181

[5] Wang Y, Zheng X, Liu L, et al. A novel structure of pressure sensors. IEEE Trans Electron Devices, 1991, 38: 1797

[6] French P J, Muro H, Shinohara T, et al. SOI pressure sensor. Digest Transducer, San Francisco, 1991: 181

[7] Tian Bian, Zhao Yulong, Jiang Zhuangde, et al. The analysis and structural design of micro SOI pressure sensors. Proc NEMS, Shenzhen, 2009: 55

[8] Takashima N, Kimura M. Proc IECON, Taipei, 2007: 2197

[9] Sze S M. Semiconductor sensors. John Wiley & Sons Inc, 1994: 140

[10] Krondorfer R, Kim Y K, Kim J, et al. Finite element simulation of package stress in transfer molded MEMS pressure sensors. Microelectron Reliab, 2004, 44: 1995