Two-dimensional threshold voltage analytical model of DMG strained-silicon-on-insulator MOSFETs*

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Abstract: For the first time, a simple and accurate two-dimensional analytical model for the surface potential variation along the channel in fully depleted dual-material gate strained-Si-on-insulator (DMG SSOI) MOSFETs is developed. We investigate the improved short channel effect (SCE), hot carrier effect (HCE), drain-induced barrier-lowering (DIBL) and carrier transport efficiency for the novel structure MOSFET. The analytical model takes into account the effects of different metal gate lengths, work functions, the drain bias and Ge mole fraction in the relaxed SiGe buffer. The surface potential in the channel region exhibits a step potential, which can suppress SCE, HCE and DIBL. Also, strained-Si and SOI structure can improve the carrier transport efficiency, with strained-Si being particularly effective. Further, the threshold voltage model correctly predicts a "rollup" in threshold voltage with decreasing channel length ratios or Ge mole fraction in the relaxed SiGe buffer. The validity of the two-dimensional analytical model is verified using numerical simulations.

Key words: SOI MOSFETs; strained-Si; dual-material gate; short channel effect; hot carrier effect; the drain-induced barrier-lowering; two-dimensional model

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1. Introduction

As technology advances, the feature sizes of MOSFETs are being continuously reduced to increase the packing density of very large-scale integration (VLSI) circuits. How to suppress the threshold voltage roll-off, short channel effect (SCE), hot carrier effect (HCE) and increase carrier transport efficiency has become a hot issue[1−4]. Strained-Si SOI MOSFETs can improve the carrier transport property[5−9]. However, they show considerable threshold voltage roll-off, SCE and HCE in the sub-100 nm regime. A dual-material gate (DMG) consisting of two metals with different work functions can suppress SCE, HCE and drain-induced barrier-lowering (DIBL) effectively[10−13]. In this paper, a novel SOI MOSFET structure with a strained-Si channel and dual-material gate is investigated. Analytical models for surface potential, surface electron field distribution and the threshold voltage are derived based on the two-dimensional Poisson's equation. The validity of the analytical model is verified using the numerical simulations.

2. Strained-Si-on-insulator MOSFET

2.1. Effect of strain on bandgap

In the presence of strain, silicon thin film experiences biaxial tension and changes its band structure[14−16]. The strain causes the electron affinity of silicon to increase; it also causes the bandgap and the effective mass of carriers to decrease. The above strain-related effects on the silicon band structure are modeled as follows[17, 18]:

$$(\Delta E_{\mathrm{C}})_{\text{s-Si}} = 0.57X, \tag{1}$$

$$(\Delta E_{\mathrm{g}})_{\text{s-Si}} = 0.4X, \tag{2}$$

$$V_{\mathrm{T}} \ln \frac{N_{\mathrm{V,Si}}}{N_{\text{s-Si}}} = V_{\mathrm{T}} \ln \left(\frac{m^*_{\mathrm{h,Si}}}{m^*_{\mathrm{h,s\text{-}Si}}} \right)^{3/2} = 0.075X, \tag{3}$$

where X is the strain in equivalent Ge mole fraction in the relaxed SiGe buffer layer; $(\Delta E_{\mathrm{C}})_{\text{s-Si}}$ is the increase in the electron affinity of silicon due to strain, $(\Delta E_{\mathrm{g}})_{\text{s-Si}}$ is the decrease in the bandgap of silicon due to strain, V_{T} is the thermal voltage. $N_{\mathrm{V,Si}}$ and $N_{\mathrm{V,s\text{-}Si}}$ are the density of states (DOS) in the valence band in normal and strained-silicon, respectively, and $m^*_{\mathrm{n,Si}}$ and $m^*_{\mathrm{n,s\text{-}Si}}$ are the effective masses of hole DOS in normal and strained-silicon, respectively.

2.2. Effect of strain on flatband voltage

The effect of strain on the front-channel flatband voltage of an FD-SOI MOSFET can be modeled as follows[17, 18]:

$$(V_{\mathrm{FB,f}})_{\text{s-Si}} = (V_{\mathrm{FB,f}})_{\mathrm{Si}} + \Delta V_{\mathrm{FB,f}}, \tag{4}$$

where

$$(V_{\mathrm{FB,f}})_{\mathrm{Si}} = \phi_{\mathrm{M}} - \phi_{\mathrm{Si}},$$

$$\Delta V_{\mathrm{FB,f}} = \frac{-(\Delta E_{\mathrm{C}})_{\text{s-Si}}}{q} + \frac{(\Delta E_{\mathrm{g}})_{\text{s-Si}}}{q} - V_{\mathrm{T}} \ln \frac{N_{\mathrm{V,Si}}}{N_{\mathrm{V,s\text{-}Si}}},$$

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$$\phi_{\mathrm{Si}} = \frac{\chi_{\mathrm{Si}}}{q} + \frac{E_{\mathrm{g,Si}}}{2q} + \phi_{\mathrm{f\text{-}Si}},$$

$$\phi_{\mathrm{f\text{-}Si}} = V_{\mathrm{T}} \ln(N_{\mathrm{A}}/n_{\mathrm{i,Si}}).$$

In the above relations, ϕ_{M} is the gate work function, ϕ_{Si} is the work function of unstrained-Si, $\phi_{\mathrm{f\text{-}Si}}$ is the Fermi potential of unstrained-Si, $E_{\mathrm{g\text{-}Si}}$ is the bandgap of unstrained-Si, q is the electronic charge, N_{A} is the body doping concentration, and $n_{\mathrm{i,Si}}$ is the intrinsic carrier concentration in unstrained-Si. In the same way, the effect of strain on the back-channel flatband voltage of an FD-SOI MOSFET is modeled as

$$(V_{\mathrm{FB,b}})_{\mathrm{s\text{-}Si}} = (V_{\mathrm{FB,b}})_{\mathrm{Si}} + \Delta V_{\mathrm{FB,b}}, \tag{5}$$

where

$$(V_{\mathrm{FB,b}})_{\mathrm{Si}} = \phi_{\mathrm{sub}} - \phi_{\mathrm{Si}},$$

$$\Delta V_{\mathrm{FB,b}} = \frac{-(\Delta E_{\mathrm{C}})_{\mathrm{s\text{-}Si}}}{q} + \frac{(\Delta E_{\mathrm{g}})_{\mathrm{s\text{-}Si}}}{q} - V_{\mathrm{T}} \ln \frac{N_{\mathrm{V,Si}}}{N_{\mathrm{V,s\text{-}Si}}}$$

$$\phi_{\mathrm{sub}} = \frac{\chi_{\mathrm{Si}}}{q} + \frac{E_{\mathrm{g,Si}}}{2q} + \phi_{\mathrm{f\text{-}sub}},$$

$$\phi_{\mathrm{f\text{-}sub}} = V_{\mathrm{T}} \ln \frac{N_{\mathrm{sub}}}{n_{\mathrm{i,Si}}},$$

where ϕ_{sub} is the work function of the silicon back-substrate under the buried oxide, $\phi_{\mathrm{f\text{-}sub}}$ is the Fermi potential in the silicon back-substrate, and N_{sub} is the doping concentration in the back-substrate.

It is also important to consider the effect of strain on the built-in voltage across the source-body and drain-body junctions in strained-Si thin film, which can be written as

$$V_{\mathrm{bi,s\text{-}Si}} = V_{\mathrm{bi,Si}} + (\Delta V_{\mathrm{bi}})_{\mathrm{s\text{-}Si}}, \tag{6}$$

where

$$V_{\mathrm{bi,Si}} = \frac{E_{\mathrm{g,Si}}}{2q} + \phi_{\mathrm{F,Si}},$$

$$(\Delta V_{\mathrm{bi}})_{\mathrm{s\text{-}Si}} = \frac{-(\Delta E_{\mathrm{g}})_{\mathrm{s\text{-}Si}}}{q} - V_{\mathrm{T}} \ln \frac{N_{\mathrm{V,Si}}}{N_{\mathrm{V,s\text{-}Si}}}.$$

3. Model formulation

3.1. Two-dimensional model for surface potential

The schematic structure of the novel DMG SSOI (dual-material gate strained-Si-on-insulator) MOSFET is shown in Fig. 1. L_1 and L_2 are the lengths of M1 and M2 respectively. The channel region is divided into two different zones since two kinds of gate material are used for the DMG SSOI MOSFET. Neglecting the effect of fixed oxide charges on the electrostatics of the channel, Poisson's equation of the potential distribution in the two strained-silicon film zones before the onset of strong inversion can be written as[19, 20]:

$$\frac{\partial^2 \phi_1(x,y)}{\partial x^2} + \frac{\partial^2 \phi_1(x,y)}{\partial y^2} = \frac{qN_{\mathrm{A}}}{\varepsilon_{\mathrm{Si}}}, \tag{7}$$

for $0 \leqslant x \leqslant L_1, 0 \leqslant y \leqslant t_{\mathrm{s\text{-}Si}}$,

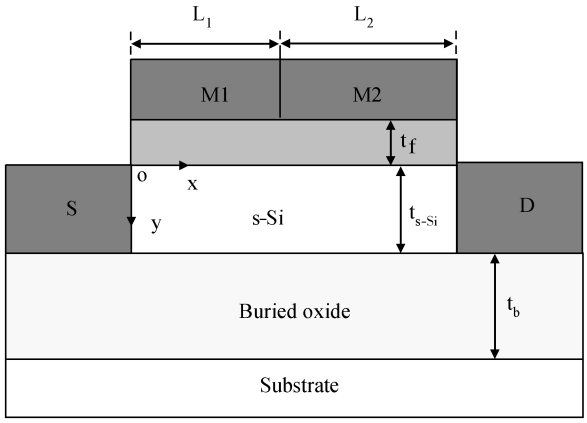

Fig. 1. Schematic structure of the DMG SSOI MOSFET.

$$\frac{\partial^2 \phi_2(x,y)}{\partial x^2} + \frac{\partial^2 \phi_2(x,y)}{\partial y^2} = \frac{qN_{\mathrm{A}}}{\varepsilon_{\mathrm{Si}}}, \tag{8}$$

for $L_1 \leqslant x \leqslant L_2, 0 \leqslant y \leqslant t_{\mathrm{s\text{-}Si}}$, where N_{A} is the doping concentration of the strained-Si film, $\varepsilon_{\mathrm{Si}}$ is the dielectric constant of strained-Si film, $t_{\mathrm{s\text{-}Si}}$ is the thickness of strained-Si film, the x axis is parallel to the channel, and the y axis is perpendicular to the channel. The potential profile in the vertical direction in the strained-Si film can be approximated by a parabolic function.

$$\phi_1(x,y) = \phi_{\mathrm{s1}}(x) + c_{11}(x)y + c_{12}(x)y^2, \tag{9}$$

for $0 \leqslant x \leqslant L_1, 0 \leqslant y \leqslant t_{\mathrm{s\text{-}Si}}$,

$$\phi_2(x,y) = \phi_{\mathrm{s2}}(x) + c_{21}(x)y + c_{22}(x)y^2, \tag{10}$$

for $L_1 \leqslant x \leqslant L_2, 0 \leqslant y \leqslant t_{\mathrm{s\text{-}Si}}$, where $\phi_{\mathrm{s1}}(x)$ and $\phi_{\mathrm{s2}}(x)$ is the front channel surface potential at the gate-oxide/strained-Si interface under M1, M2, respectively. The coefficients $c_{11}(x)$, $c_{12}(x)$, $c_{21}(x)$ and $c_{22}(x)$ are functions of x. Poisson's equation can be solved using the following boundary conditions.

(1) Electric flux (displacement) at the gate-oxide/strained-Si film interface is continuous, i.e.,

$$\left.\frac{\mathrm{d}\phi_1(x,y)}{\mathrm{d}y}\right|_{y=0} = \frac{\varepsilon_{\mathrm{ox}}}{\varepsilon_{\mathrm{Si}}} \frac{\phi_{\mathrm{S1}}(x) - V'_{\mathrm{GS1}}}{t_{\mathrm{f}}}, \tag{11}$$

$$\left.\frac{\mathrm{d}\phi_2(x,y)}{\mathrm{d}y}\right|_{y=0} = \frac{\varepsilon_{\mathrm{ox}}}{\varepsilon_{\mathrm{Si}}} \frac{\phi_{\mathrm{S2}}(x) - V'_{\mathrm{GS2}}}{t_{\mathrm{f}}}, \tag{12}$$

where $\varepsilon_{\mathrm{ox}}$ is the dielectric constant of the gate oxide, t_{f} is the gate oxide thickness, V_{GS} is the gate-to-source bias voltage, $V'_{\mathrm{GS1}} = V_{\mathrm{GS}} - (V_{\mathrm{FB1,f}})_{\mathrm{s\text{-}Si}} V'_{\mathrm{GS2}} = V_{\mathrm{GS}} - (V_{\mathrm{FB2,f}})_{\mathrm{s\text{-}Si}}$.

(2) Electric flux at the interface of the buried oxide and the back channel is continuous, i.e.,

$$\left.\frac{\mathrm{d}\phi_1(x,y)}{\mathrm{d}y}\right|_{y=t_{\mathrm{s\text{-}Si}}} = \frac{\varepsilon_{\mathrm{ox}}}{\varepsilon_{\mathrm{Si}}} \frac{V'_{\mathrm{SUB}} - \phi_{\mathrm{B}}(x)}{t_{\mathrm{b}}}, \tag{13}$$

$$\left.\frac{\mathrm{d}\phi_2(x,y)}{\mathrm{d}y}\right|_{y=t_{\mathrm{s\text{-}Si}}} = \frac{\varepsilon_{\mathrm{ox}}}{\varepsilon_{\mathrm{Si}}} \frac{V'_{\mathrm{SUB}} - \phi_{\mathrm{B}}(x)}{t_{\mathrm{b}}}, \tag{14}$$

where t_{b} is the buried-oxide thickness, $V'_{\mathrm{SUB}} = V_{\mathrm{SUB}} - (V_{\mathrm{FB,b}})_{\mathrm{s\text{-}Si}}$, V_{SUB} is the substrate bias, and $\phi_{\mathrm{B}}(x)$ is the back-channel potential at the strained-Si/buried oxide interface.

(3) Electric flux (displacement) and the electric potential at the M1/M2 interface is continuous, i.e.,

$$\left.\frac{\mathrm{d}\phi_1(x,y)}{\mathrm{d}x}\right|_{x=L_1} = \left.\frac{\mathrm{d}\phi_2(x,y)}{\mathrm{d}x}\right|_{x=L_1}, \tag{15}$$

$$\phi_1(L_1,0) = \phi_2(L_1,0). \tag{16}$$

(4) The surface potential at the source end is

$$\phi_1(0,0) = \phi_{S1}(0) = V_{\text{bi, s-Si}}. \tag{17}$$

(5) The surface potential at the drain end is

$$\phi_2(L_1+L_2,0) = \phi_{S2}(L_1+L_2) = V_{\text{bi, s-Si}} + V_{DS}, \tag{18}$$

where V_{DS} is the drain-to-source bias voltage.

Using the boundary conditions Eqs.(11)–(14), one can obtain the coefficients $c_{11}(x)$, $c_{12}(x)$, $c_{21}(x)$, $c_{22}(x)$ in Eqs. (9) and (10), and obtain the expressions for $\phi_1(x,y)$ and $\phi_2(x,y)$. Substituting $\phi_1(x,y)$ and $\phi_2(x,y)$ into Eqs. (7) and (8) respectively and substituting $y = 0$, one obtains

$$\frac{\mathrm{d}^2\phi_{S1}(x)}{dx^2} - \alpha^2\phi_{S1}(x) = \beta_1, \tag{19}$$

$$\frac{\mathrm{d}^2\phi_{S2}(x)}{dx^2} - \alpha^2\phi_{S2}(x) = \beta_2, \tag{20}$$

where

$$\alpha^2 = \frac{2(C_b C_{\text{s-Si}} + C_f C_{\text{s-Si}} + C_b C_f)}{t_{\text{s-Si}}^2 C_{\text{s-Si}}(2C_{\text{s-Si}} + C_b)},$$

$$\beta_1 = \frac{qN_A}{\varepsilon_{Si}} - 2V'_{gs1}\frac{C_f(C_{\text{s-Si}} + C_b)}{t_{\text{s-Si}}^2 C_{\text{s-Si}}(2C_{\text{s-Si}} + C_b)} - 2V'_{SUB}\frac{C_b}{t_{\text{s-Si}}^2(2C_{\text{s-Si}} + C_b)},$$

$$\beta_2 = \frac{qN_A}{\varepsilon_{Si}} - 2V'_{gs2}\frac{C_f(C_{\text{s-Si}} + C_b)}{t_{\text{s-Si}}^2 C_{\text{s-Si}}(2C_{\text{s-Si}} + C_b)} - 2V'_{SUB}\frac{C_b}{t_{\text{s-Si}}^2(2C_{\text{s-Si}} + C_b)}.$$

Here, $C_{\text{s-Si}} = \varepsilon_{Si}/t_{\text{s-Si}}$, $C_f = \varepsilon_f/t_f$ and $C_b = \varepsilon_{ox}/t_b$.

The solutions for Eqs. (19) and (20) are simple second-order non-homogeneous differential equations with constant coefficients, which can be written as

$$\phi_{S1}(x) = A\exp(\alpha x) + B\exp(-\alpha x) - \frac{\beta_1}{\alpha^2}, \tag{21}$$

$$\phi_{S2}(x) = C\exp[\alpha(x-L_1)] + D\exp[-\alpha(x-L_1)] - \frac{\beta_2}{\alpha^2}. \tag{22}$$

Now, using boundary conditions Eqs.(15)–(18) to solve for A, B, C and D, one obtains

$$B = \left\{\left(V_{\text{bi,s-Si}} + \frac{\beta_1}{\alpha^2}\right)[\exp(\alpha L) - 1] - V_{DS} - \frac{\beta_2 - \beta_1}{2\alpha^2} \times [2 - \exp(\alpha L_2) - \exp(-\alpha L_2)]\right\}[2\sinh(\alpha L)]^{-1}, \tag{23}$$

$$A = \left\{\frac{\beta_2 - \beta_1}{2\alpha^2}[2 - \exp(\alpha L_2) - \exp(-\alpha L_2)] + V_{DS} + B[1 - \exp(-\alpha L)]\right\}[\exp(\alpha L) - 1]^{-1}, \tag{24}$$

$$C = A\exp(\alpha L_1) + \frac{\beta_2 - \beta_1}{2\alpha^2}, \tag{25}$$

$$D = B\exp(-\alpha L_1) + \frac{\beta_2 - \beta_1}{2\alpha^2}. \tag{26}$$

The minimum potential of the front-channel can be calculated from Eq. (21) as

$$\phi_{s,\min} = 2\sqrt{AB} - \frac{\beta_1}{\alpha^2}. \tag{27}$$

The minimum occurs at

$$x_{\min} = \frac{1}{2\alpha}\ln\frac{B}{A}. \tag{28}$$

The electric field pattern along the channel determines the electron transport velocity through the channel. The electric field horizontal components under the metal gates M1 and M2 are given as

$$E_1(x) = A\alpha\exp(\alpha x) - B\alpha\exp(-\alpha x), \tag{29}$$

$$E_2(x) = C\alpha\exp[\alpha(x-L_1)] - D\alpha\exp[-\alpha(x-L_1)]. \tag{30}$$

3.2. Two-dimensional model for threshold voltage

The threshold voltage V_{TH} is the value of the gate voltage V_{GS} at which a conducting channel of the SOI MOSFET is induced. In a fully depleted thin film SOI, it is desirable that the front channel turns on before the back channel. Therefore, the threshold voltage is taken to be that value of gate source voltage for which $\phi_{s,\min} = 2\phi_{F,Si}$, where $\phi_{F,Si}$ is the difference between the extrinsic Fermi level in the bulk region and the intrinsic Fermi level. For the strained-Si SOI MOSFET, the threshold condition under the front gate is modified as[19, 20]

$$\phi_{s,\min} = 2\phi_{F,Si} + \Delta\phi_{\text{s-Si}} = \phi_{th}, \tag{31}$$

where

$$\Delta\phi_{\text{s-Si}} = -\frac{(\Delta E_g)_{\text{s-Si}}}{q} = V_T\ln\frac{N_{V,Si}}{N_{V,\text{s-Si}}}.$$

ϕ_{th} is the value of surface potential at which the volumetric inversion electron charge density in the strained-Si device is the same as that in the unstrained-Si at threshold, i.e., equal to the body doping.

In the case of the DMG structure, due to the coexistence of the different metal M1 and M2, the minimum surface potential is solely determined by the metal gate with the higher work function. So the threshold voltage is defined as the value of V_{GS} at which the minimum surface potential $\phi_{s,\min}$ equals ϕ_{th}. Hence, one can determine the value of threshold voltage as the value of V_{GS} by solving Eq. (27).

When $C_b \ll C_f$ and $C_b \ll C_{Si}$, the threshold voltage can be expressed as follows:

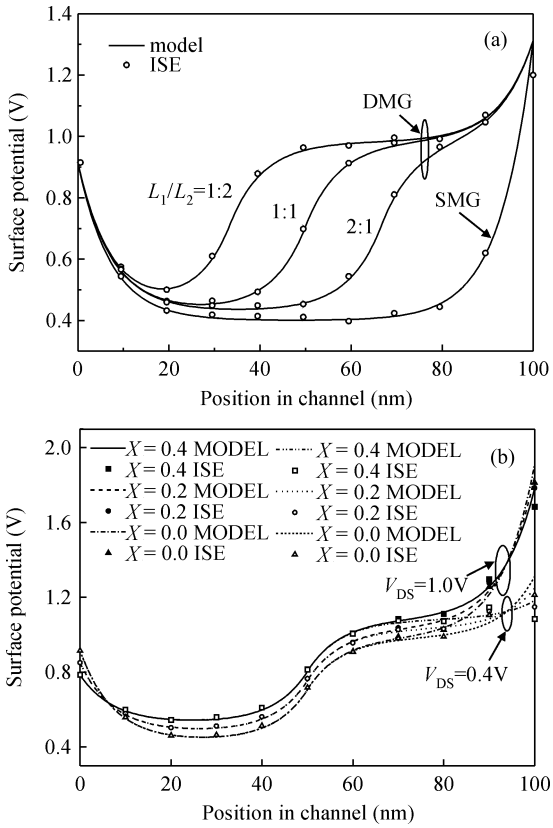

Fig. 2. (a) DMG MOSFET surface potential for different gate length ratios (L_1/L_2 = 2 : 1, 1 : 1, 1 : 2) and SMG MOSFET surface potential against the horizontal distance x in the channel. (b) Variation of surface potential of the FD DMG SSOI MOSFET for different V_{DS} (V_{GS} = 0.15 V, L_1/L_2 = 1 : 1, L = 100 nm).

$$V_{TH} = \frac{-\eta + \sqrt{\eta^2 - 4\sigma\xi}}{2\sigma}, \tag{32}$$

where

$$\gamma = \exp(-\alpha L),$$

$$\sigma = \frac{1}{\gamma} - \sinh^2(\alpha L) - 2 + \gamma,$$

$$\eta = V_{bi1}\left(1 - \frac{1}{\gamma}\right) + \sinh^2(\alpha L)\cdot(2\phi_{th} - 2u) - V_{bi2}(1-\gamma),$$

$$\xi = V_{bi1}V_{bi2} - \sinh^2(\alpha L)\cdot(\phi_{th} - u)^2,$$

$$V_{bi1} = V_{bi,\,s\text{-}Si}(1-\gamma) + V_{DS} - (u-v)\cosh(\alpha L_2) - v + u\gamma,$$

$$V_{bi2} = V_{bi,\,s\text{-}Si}\left(\frac{1}{\gamma} - 1\right) - V_{DS} + (u-v)\cosh(\alpha L_2) + v - \frac{u}{\gamma},$$

$$u = \frac{C_b}{C_f}V'_{SUB} - \frac{qN_A t_{Si}}{C_f} - (V_{FB1})_{s\text{-}Si},$$

$$v = \frac{C_b}{C_f}V'_{SUB} - \frac{qN_A t_{Si}}{C_f} - (V_{FB2})_{s\text{-}Si}.$$

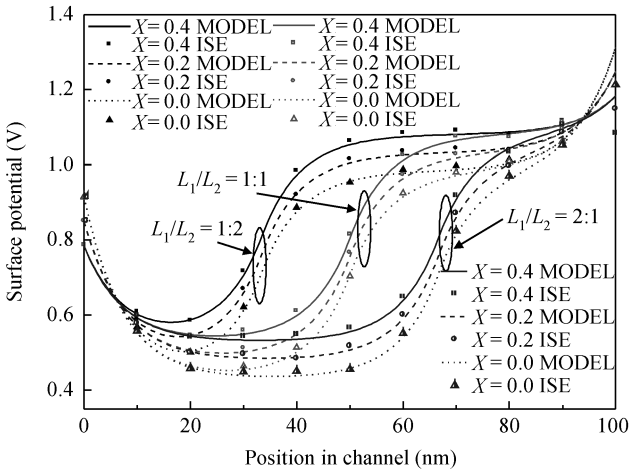

Fig. 3. Variation of surface potential of FD DMG SSOI MOSFET for different gate length ratios (V_{GS} = 0.15 V, V_{DS} = 0.4 V, L =100 nm).

4. Results and discussion

To verify the proposed analytical model, the FD n-channel DMG SSOI structure shown in Fig. 1 was used. Typical values of work function for gate metals M1 and M2 were chosen as 4.77 eV and 4.10 eV, respectively. t_f = 3 nm, t_b = 100 nm, $t_{s\text{-}Si}$ = 6 nm, V_{SUB} = 0 V, $N_A = 1\times 10^{17}$ cm^{-3}, $N_{SUB} = 1\times 10^{16}$ cm^{-3}.

Figure 2(a) shows the curve of the DMG MOSFET surface potential for different gate length ratios (L_1/L_2 = 2 : 1, 1 : 1, 1 : 2) and the SMG MOSFET surface potential against the horizontal distance x in the channel. From the comparison, there is a step change of the potential along the channel at the interface of M1 and M2 for the DMG MOSFET. Figure 2(b) shows the curve of surface potential against the horizontal distance x in the channel at different drain voltages. Due to the presence of DMG, there is no significant change in the potential under the gate M1 with increasing drain bias. Hence, the channel region under M1 is "screened" because of the changes in the drain potential, i.e., the drain voltage is not absorbed under M1 though it is absorbed under M2. As a consequence, V_{DS} has only a little influence on the drain current after saturation. The drain conductance is reduced. It is evident from the figure that the shift in position of the minimum potential is almost zero irrespective of the applied drain bias. This is a clear indication that the DIBL effect is considerably reduced for the DMG SSOI MOSFET. Also, it can be seen that the surface potential under gates M1 and M2 increases with increasing strain$X$.

Figure 3 shows the variation of surface potential along the normalized channel portion for different gate length ratios (L_1/L_2 = 2 : 1, 1 : 1, 1 : 2). The gate length L is 100 nm under conditions of different values of effective Ge mole fraction in the relaxed SiGe buffer (X = 0, X = 0.2 and X = 0.4). The surface potential changes greatly at the interface of M1 and M2 for the DMG SSOI MOSFET, which can suppress SCE due to the screening effect. As the gate length ratio is reduced, the abrupt change of the potential moves toward the source side. The surface potential increases with increasing strain X.

Figure 4 shows the variation of horizontal electric field of the FD DMG SSOI MOSFET for different gate length ratios. The point of maximum barrier lies at the interface of the two

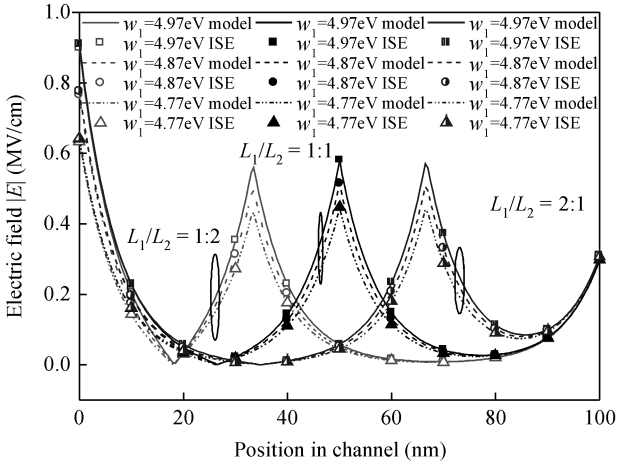

Fig. 4. Variation of electric field of the FD DMG SSOI MOSFET for different gate length ratios and work functions of gate metal M1. X = 0.2, V_{GS} = 0.15 V, V_{DS} = 0.4 V.

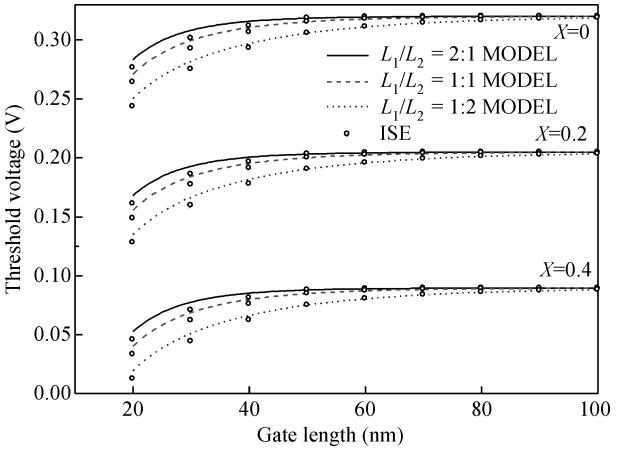

Fig. 5. Variation of threshold voltage of FD DMG SSOI MOSFET for different Ge mole fractions and gate length ratios. V_{DS} = 0.4 V.

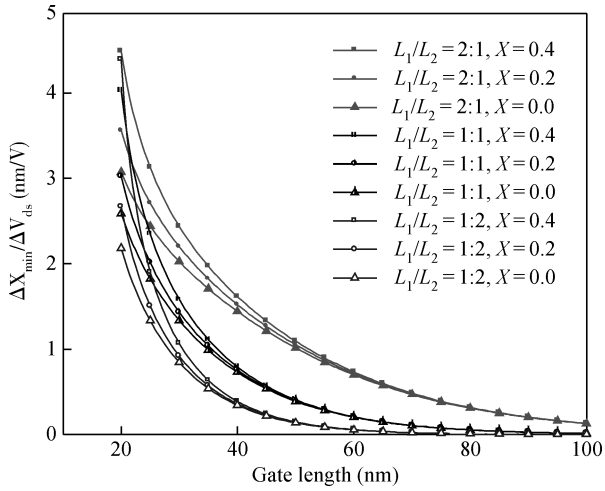

Fig. 6. Variation of change in minimum surface potential $\Delta x_{min}/\Delta V_{DS}$ with gate length for different L_1/L_2 ratios at different values of effective Ge mole fraction in relaxed SiGe.

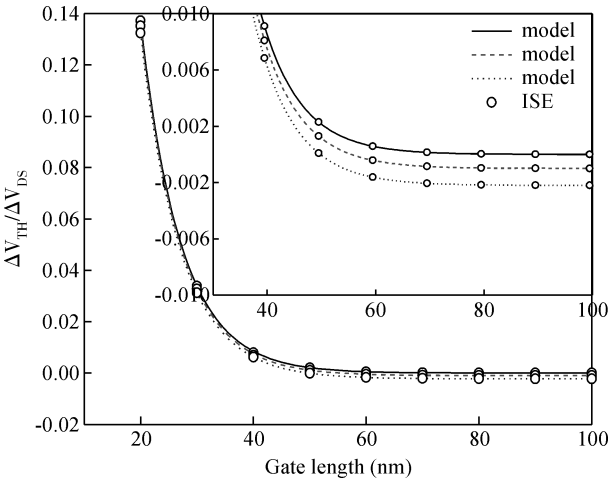

Fig. 7. $\Delta V_{th}/\Delta V_{DS}$ variation with different gate lengths (x = 0).

metal gates. As L_1 decreases or the L_1/L_2 ratio decreases, the point of peak electric field at the interface shifts toward the source end. This causes more uniformity of the electric field in the channel, resulting in a higher carrier drift velocity and device speed. The carrier transport efficiency increases with decreasing L_1, which causes HCE to reduce and DIBL to improve. The peak electric field increases with the increasing work function of metal gate M1.

Figure 5 shows the variation of threshold voltage with the gate length for different Ge mole fractions and gate length ratios. It is observed that SCE become serious on decreasing the channel length ratios. It is also observed that the threshold voltage is lower for higher strain in the silicon film for a given channel length. The change with increasing Ge content X is due to a decrease in the flatband voltage, a decrease in the built-in potential barrier, and an earlier onset of inversion due to a decrease in ϕ_{th}.

The effect of DIBL can be explained by two methods: (1) a change in the position of the minimum surface potential Δx_{min} ($\Delta x_{min} = x_{min}|_{V_{DS}=0\,V} - x_{min}|_{V_{DS}=2\,V}$) with V_{DS}, i.e., $\Delta x_{min}/\Delta V_{DS}$; (2) a change in the threshold voltage (ΔV_{th}) with V_{DS}, i.e. , $\Delta V_{th}/\Delta V_{DS}$. Figure 6 shows the $\Delta x_{min}/\Delta V_{DS}$ variation with gate length for different L_1/L_2 ratios and Ge mole fractions. When L_1/L_2 = 1 : 2 and X = 0, $\Delta x_{min}/\Delta V_{DS}$ is the minimum. This validates the DIBL reduction with increasing screen gate length (L_2). It also validates the DIBL reduction with decreasing X.

Figure 7 shows the $\Delta V_{th}/\Delta V_{DS}$ variation with different gate lengths, for different gate length ratios. It may be seen that $\Delta V_{th}/\Delta V_{DS}$ is the lowest for the DMG SSOI MOSFET when L_1/L_2 = 1 : 2 and X = 0.

5. Conclusion

By developing a 2-D analytical model for surface potential and threshold voltage, the paper has examined the effectiveness of DMG structure in fully depleted SSOI MOSFETs to suppress SCE. The results unambiguously show that the introduction of the novel device leads to the suppression of SCE due to a step-function in the channel potential profile. The shift in surface channel potential minimum position is negligible with increasing drain bias. The electric field in the channel at the

drain end is reduced, which improves HCE. Further, it is clearly seen that the DMG SSOI MOSFET gives rise to a desirable threshold voltage roll-off with decreasing channel length and improves the carrier transport efficiency. The derived analytical models are in good agreement with the results of the two-dimensional device simulator ISE.

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