A low-spurious fast-hopping MB-OFDM UWB synthesizer*

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Abstract: A frequency synthesizer for the ultra-wide band (UWB) group #1 is proposed. The synthesizer uses a phase-locked loop (PLL) and single-sideband (SSB) mixers to generate the three center frequencies of the first band group by mixing 4224 MHz with ±264 MHz and 792 MHz, respectively. A novel multi-QSSB mixer is designed to combine the function of frequency selection and frequency conversion for low power and high linearity. The synthesizer is fabricated in Jazz 0.18-μm RF CMOS technology. The measured reference spur is as low as –69 dBc and the maximum spur is the LO leakage of –32 dBc. A low phase noise of –110 dBc/Hz @ 1 MHz offset and an integrated phase noise of 1.86° are achieved. The hopping time between different bands is less than 1.8 ns. The synthesizer consumes 30 mA from a 1.8 V supply.

Key words: frequency synthesizer; SSB mixer; VCO; PLL
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1. Introduction

Ultra-wide band (UWB) is a short-range high data-rate wireless technology for which FCC allows use of the frequency band from 3.1 to 10.6 GHz[1]. The multi-band OFDM alliance (MBOA) proposal divides the spectrum into 14 sub-bands with a channel spacing of 528 MHz. The center frequencies for the band group #1 are 3432 MHz, 3960 MHz and 4488 MHz. The MBOA proposal assumes frequency hopping over the bands per OFDM symbol with a switching time about 9.5 ns. This fast switching is practically infeasible with respect to a classical phase-locked-loop (PLL) programmable synthesizer architecture.

Several methods have been reported to conquer the switching problem. In Ref. [2], the synthesizer has three fixed-modulus PLLs, one for each of the three frequencies in band group #1. In Ref. [3], a DLL-based frequency multiplier is used to generate the three frequencies by switching the feedback clock from one delay cell to another. However, both References [2] and [3] are difficult to be further extended to cover more bands for power and area consideration. Most of the state-of-the-art solutions[4,5] make extensive use of single side-band (SSB) frequency mixing in order to meet the frequency hopping time requirements. In Ref. [4], two PLLs are used, resulting in large chip size and much power consumption. In Ref. [5], divide-by-8.5 and divide-by-17 dividers as well as a VCO oscillating at 8976 MHz are needed to generate the mandatory three frequencies. They consume a lot of power and increase the design complexity.

In this design, a synthesizer (see Fig. 1) adopts one ideal PLL and two quadrature SSB (QSSB) mixers, one of which is a novel multi-QSSB mixer. In SSB-mixer based synthesizers, the spurious performance is the most troublesome issue. The proposed multi-QSSB mixer combines the function of frequency conversion and frequency selection for a better linearity and a cleaner output spectrum than the conventional SSB mixer and frequency multiplexer. Divide-by-2 dividers are effectively used to generate quadrature outputs. Two high frequency dividers are reused in the PLL and in generating the essential frequencies for mixing for power reduction.

2. Architecture

A block diagram of the proposed synthesizer architecture is shown in Fig. 1. It is composed of a PLL and two QSSB mixers. The three frequencies in UWB band group #1 are generated by the following equations.

$$3432\,\text{MHz} = 4224\,\text{MHz} - 792\,\text{MHz}, \quad (1)$$

$$3960\,\text{MHz} = 4224\,\text{MHz} - 264\,\text{MHz}, \quad (2)$$

$$4488\,\text{MHz} = 4224\,\text{MHz} + 264\,\text{MHz}. \quad (3)$$

The PLL generates the quadrature signals of 4224 MHz, and the QSSB mixers execute the up/down frequency conversion.

In the PLL, an LC-QVCO is used to oscillate at 4224 MHz. The reference clock is 24 MHz. Three divide-by-2 dividers (Div2) and a digital divide-by-22 divider are used in the divider-chain. Div2s can generate quadrature outputs in its nature. A dummy Div2 is added to the in-phase path to provide a balanced load for the QVCO's in-phase and quadrature-phase (IQ) outputs, as seen in Fig. 1.

Two Div2s are added to the 1056 MHz obtained in the divider-chain to generate the essential IQ signal of 264 MHz. A QSSB mixer, whose RF and LO inputs are 264 MHz and 1056 MHz respectively, is used to generate the frequency of 792 MHz. A multi-QSSB mixer executes the last-stage frequency conversion. It combines the function of frequency mixing and frequency selection. The output frequency is controlled by the selecting signal. Poly-phase filters are added before each QSSB mixer to filter out the unwanted input sideband signals.

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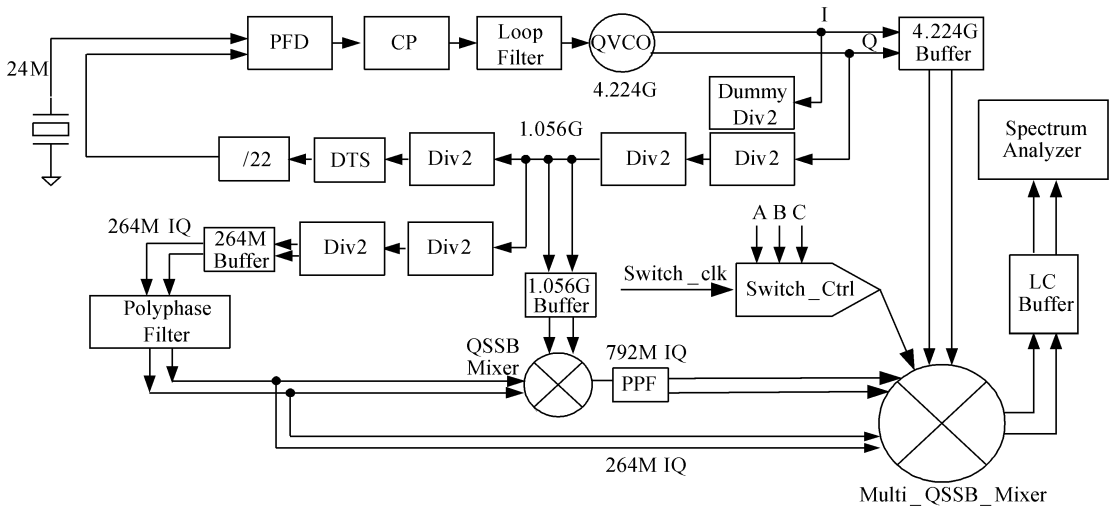

Fig. 1. Proposed synthesizer architecture.

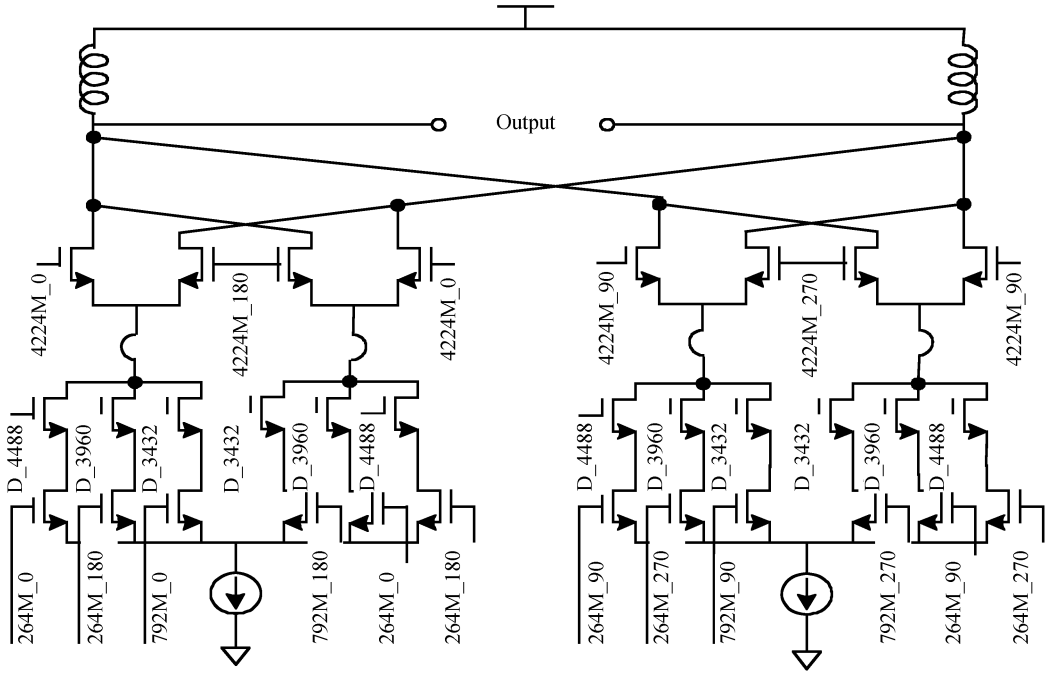

Fig. 2. Schematic of the proposed multi-QSSB mixer.

3. Circuit design

3.1. Multi-QSSB mixer

Generally, QSSB mixers realize the up/down frequency conversion in the synthesizer. They generate quadrature outputs and require quadrature inputs. Their performance determines the output spectrum, i.e. the spur of the synthesizer. In order to get a clean output spectrum, a good linearity of the QSSB mixers is needed, as well as a pure and balanced input of the QSSB mixers.

In this design, a novel multi-QSSB mixer is proposed. It combines the function of frequency conversion and frequency selection. The circuit of the proposed multi-QSSB mixer is shown in Fig. 2. The LO frequency is fixed at 4224 MHz. The RF signal could be selected from three different frequencies and phases, i.e. –264 MHz, +264 MHz and –792 MHz, according to the control signals D_3960, D_4488 and D_3432. The switches are cascode to the corresponding input RF transistors. They are on the top of the RF transistors for a better RF-to-output isolation. Only one set of the switches controlled by the same signal is on at one time. Frequency hopping could be easily realized by changing the effect control signal.

The proposed multi-QSSB mixer avoids using a separated frequency selector, which would consume more power. Besides that, the unbalance and non-linearity caused by a selector is avoided. This helps to achieve a better spurious performance.

3.2. Quadrature VCO

To generate quadrature signals, two cross-coupled LC VCOs as shown in Fig. 3 are implemented. As Leeson's fa-

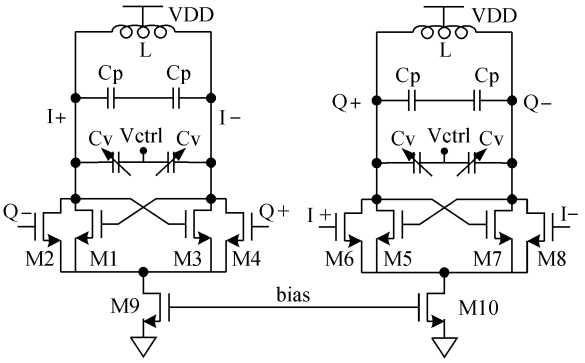

Fig. 3. Quadrature VCO.

mous model predicts[6], the phase noise of an LC VCO could be described as Eq. (4), wherein $\omega_{\rm osc}$ is the oscillating frequency of the VCO, $\Delta\omega$ is the frequency offset to the oscillating frequency, k is the Boltzmann constant, T is the Kelvin temperature, F is the noise factor of the circuit, $P_{\rm sig}$ is the power of the oscillating signal, and $Q_{\rm eff}$ is the effective quality factor of the tank:

$$L(\Delta\omega) = 10\lg\left\{\frac{2kTF}{P_{\rm sig}}\left(\frac{\omega_{\rm osc}}{2Q_{\rm eff}\Delta\omega}\right)^2\right\}. \quad (4)$$

To a quadrature VCO (QVCO), $P_{\rm sig}$, $Q_{\rm eff}$, and F are all related to the coupling coefficient m, which is equal to the current ratio of M2 to M1 , i.e. $m = I_2/I_1$. However, m has little effect on F, for F is dominated by the tail current. With careful analysis, Equation (5) could be derived[7], wherein Q is the quality factor of the tank, R is the equivalent parallel resistance of the tank, and $I_{\rm tail}$ is the tail current. Together with Eq. (4), this indicates that a larger m causes a worsened phase noise of the QVCO. However, a smaller m will induce more phase error between the in-phase and quadrature-phase outputs[8]. $m = 1/3$ is chosen as a tradeoff in this design:

$$P_{\rm sig}Q_{\rm eff}^2 = \frac{Q}{(1+m)^2}\left(\frac{4}{\pi}I_{\rm tail}\right)^2 R. \quad (5)$$

The required QVCO oscillating frequency is 4224 MHz. 5-bit switched-capacitor arrays in parallel with the MOS varactors are used here to widen the QVCO's tuning range for PVT robustness.

3.3. Charge pump

The charge pump is a key module which determines the reference spur of the synthesizer's output. A good design of the charge pump should eliminate the mismatch of the charge/discharge current and other nonideal factors such as current-sharing. The schematic of the charge pump in this work is shown in Fig. 4. Two rail-to-rail operation-amplifiers (OP) are used.

OP1 makes the voltage of node n1 equal to $V_{\rm out}$, hence the voltages of nodes n2 and n3 remain the same when the switches' state (UP, DONW, UP_BAR, DOWN_BAR) changes. Thus the unwanted current-sharing can be eliminated when the switches turn on and off.

OP2 is used in another negative feedback to achieve good current matching. It makes the voltage of node n4 be equal to

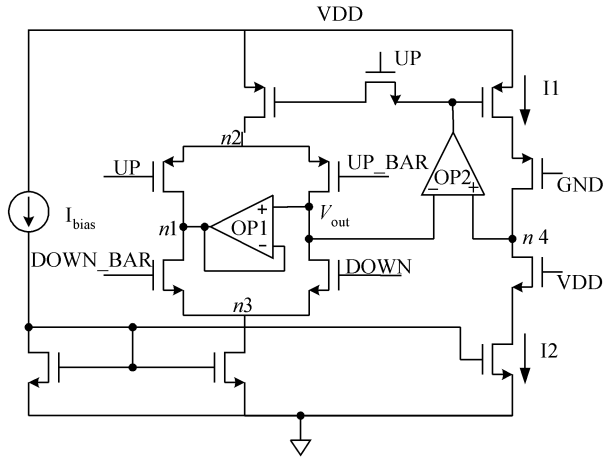

Fig. 4. Schematic of the charge pump.

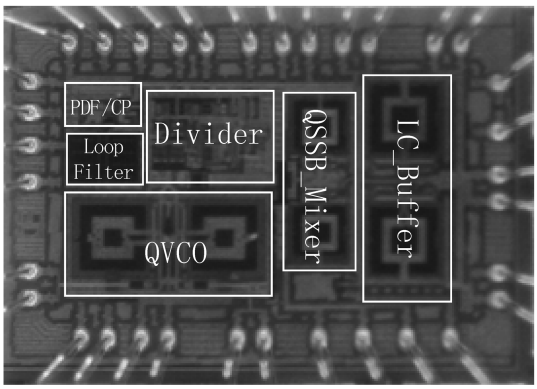

Fig. 5. Die photo.

$V_{\rm out}$. The current of I_1 and I_2 are equal because no other path exists. I_1 and I_2 will be exactly replicated to the charging and discharging current sources when the switches turn on (UP = 1, DOWN = 1), ensuring good current matching.

4. Measurement

The proposed frequency synthesizer for UWB band group #1 is implemented in Jazz 0.18-μm RF CMOS technology. A die photo of it is shown in Fig. 5. The total area occupies 2.3 × 1.5 mm^2. The synthesizer draws 30 mA current from a 1.8 V supply without the LC test buffer.

Figure 6 is the measured phase noise of the output frequency at 3432 MHz. It achieves –110 dBc/Hz @ 1 MHz which is sufficient for the MB-OFDM UWB system. The RMS phase error is 1.86°, obtained from an appropriate design of the QVCO and a low phase noise in band. The bandwidth of the PLL is designed to be 200 kHz. In UWB systems, the RMS phase error may be more important than the spot phase noise because it is the dominant factor in EVM degradation while the spot phase noise of the LO is determined by the receiver's adjacent channel selectivity and the intermodulation characteristic performance.

Figures 7(a) and 7(b) show the output spectrum of 3960 MHz. Figure 7(a) shows a small spectrum span of 100 MHz. The reference spur is as low as –69.6 dBc, because the refer-

Table 1. Comparison of the proposed PLL with previous work.

Parameter	Ref. [5]	Ref. [9]	Ref. [10]	This work
Number of bands	3 Bands	3 Bands	9 Bands	3 Bands
Sideband suppression (dBc)	> 34	> 30	> 22	> 32
Phase noise @ 1 MHz (dBc/Hz)	–108	–90	–104	–110
Integrated phase noise (°)	N.A.	N.A.	4.43	1.86
Switching time (ns)	< 1.5	< 7	< 1	< 1.8
Technology	0.18-μm CMOS	0.18-μm CMOS	0.18-μm CMOS	0.18-μm CMOS
Supply voltage (V)	1.8	1.8	1.5	1.8
Power consumption (mW)	124	70	88	54

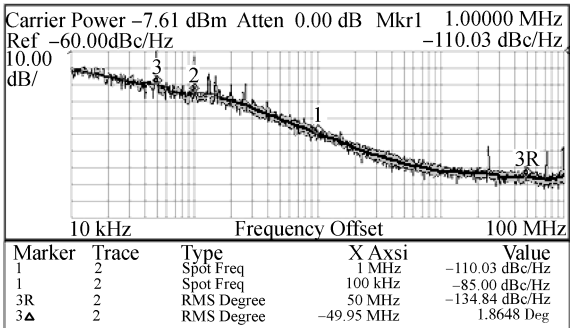

Fig. 6. Phase noise of the output at 3432 MHz.

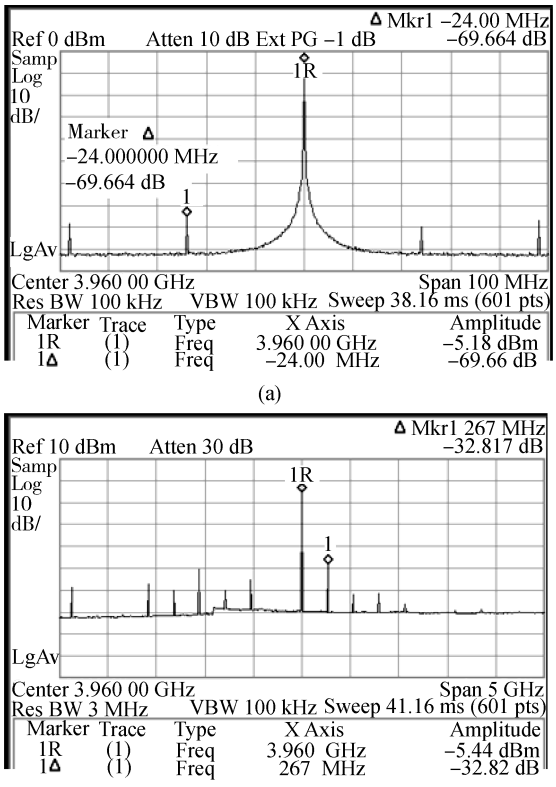

Fig. 7. (a) Frequency spectrum of 3960 MHz. (b) Frequency spectrum of 3960 MHz.

ence clock is 24 MHz. This indicates the good design of the charge pump as well as the phase-locked loop. Figure 7(b) shows a large spectrum span of 5 GHz. The spectrum is very clean. Most spurs are below –50 dBc. The maximum spur is –32.8 dBc at 4224 MHz, which is caused mainly by the substrate coupling from QVCO due to the low substrate resistivity of 3 Ω·cm. A lower leakage spur would be expected with better isolation of the QVCO output in the layout and PCB. The spurs caused by mixing are troublesome issues in SSB-mixer based frequency synthesizers. In this design, they are very low as seen in Fig. 7(b). The image spur at 4488 MHz is about –50 dBc. All these indicate that the multi-QSSB mixer and its former stages work quite well.

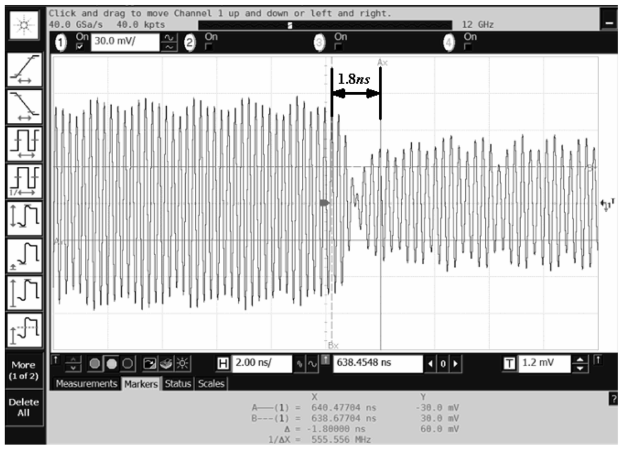

Fig. 8. Transient switching from 4488 to 3432 MHz.

The fast switching property of the frequency synthesizer is shown in Fig. 8. A clock generator was used to trigger the control of the multi-QSSB mixer. From Fig. 8 it is clearly seen that the switching time from 4488 to 3432 MHz is less than 1.8 ns.

Finally, the key performance parameters of the proposed frequency synthesizer are summarized in Table 1 along with the characteristics of other existing implementations.

5. Conclusions

This paper presents a low-spurious fast-hopping frequency synthesizer for an MB-OFDM UWB system in 0.18 μm RF CMOS technology. The proposed synthesizer consists of a single PLL and two QSSB mixers, one of which is a novel multi-QSSB mixer for power reduction and spurious rejection. It exhibits a frequency transition time of less than 1.8 ns and sideband rejection of 32 dBc. The measured phase noise is –110 dBc/Hz at 1 MHz offset frequency. The total power consumption of the frequency synthesizer is 54 mW from a 1.8 V supply voltage.

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