Analysis and design of power efficient semi-passive RFID tag*

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Abstract: The analysis and design of a semi-passive radio frequency identification (RFID) tag is presented. By studying the power transmission link of the backscatter RFID system and exploiting a power conversion efficiency model for a multi-stage AC–DC charge pump, the calculation method for semi-passive tag's read range is proposed. According to different read range limitation factors, an intuitive way to define the specifications of tag's power budget and backscatter modulation index is given. A test chip is implemented in SMIC 0.18 μm standard CMOS technology under the guidance of theoretical analysis. The main building blocks are the threshold compensated charge pump and low power wake-up circuit using the power triggering wake-up mode. The proposed semi-passive tag is fully compatible to EPC C1G2 standard. It has a compact chip size of 0.54 mm^2, and is adaptable to batteries with a 1.2 to 2.4 V output voltage.

Key words: RFID; semi-passive tag; power conversion efficiency; AC–DC charge pump; wake-up circuit
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1. Introduction

Radio frequency identification (RFID) is a rapidly developing automatic identification technology. As defined by EPC_{global}, semi-passive tags are a higher class of RFID tags compared to the well known class of passive tags[1] which have been widely used in logistics and warehouse management[2, 3]. The term "semi-passive" means batteries are employed to supply the functional circuits for signal processing and data storage, but the tags still operate in a passive manner in that they use "reader talk first" mode and backscatter mechanism for uplink (tag to reader) communication[4]. Thanks to the battery, semi-passive tags are less dependent on receiving power strength than passive tags and thus have better readability and read range performances[5−7]. These qualities make them highly expected in applications like post management, dangerous cargo surveillance and cold chain logistics[8, 9]. On the other hand, since semi-passive tags do not use the method of power amplification to transmit signals, cheap thin film batteries with small power capacity can be employed to make them commercially competitive in price[10].

Though technologies of UHF RFID tags have been studied for years, the design of semi-passive tag IC still remains an emerging area and relative reports are few. A semi-passive tag composed by on-board discrete devices was reported in Ref. [5]. Kim *et al.*[6] proposed a fully integrated passive/semi-passive tag which has an on-chip temperature sensor. A study on battery powered RFID tags with complicated circuit structure was provided in Ref. [7]. However, the design criterion for semi-passive tag's power budget and optimization method for backscatter modulation index are still lacking in literature. Besides, the conventional calculation method for read range only takes tag power consumption as a critical factor, without considering the impact of reader performance.

By studying the transmission link of the backscatter RFID system, this paper reveals the joint effect of tag power consumption and reader sensitivity on read range in a mathematical way. The analysis also gives a design instruction for semi-passive tag's power issues. The theoretical analysis is verified by the design and measurements of a compact semi-passive tag chip implemented in SMIC 0.18 μm standard CMOS technology.

2. Transmission link analysis

Figure 1 illustrates the power transmission link of backscatter RFID system. It is composed by reader, air channel (denoted by the arcs), tag's rectifier (usually an AC–DC charge pump) and tag's processing circuit. Definitions of the variables are listed in Table 1. Total available power for tag $P_{\rm av}$ is to be distributed between $P_{\rm in}$ and $P_{\rm sc}$. According to the free space transmission assumption, the total available power $P_{\rm av}$ for tag is determined by the distance between reader and tag, in another word, the read range:

$$P_{\rm av} = P_{\rm tx} - 10\lg(4\pi d/\lambda)^2 + G_{\rm t}, \tag{1}$$

where d is the read range, λ is the wavelength, and $G_{\rm t}$ is the gain of tag antenna.

In order to establish communications between reader and tag, two requirements need to be met: for the downlink, $P_{\rm load}$

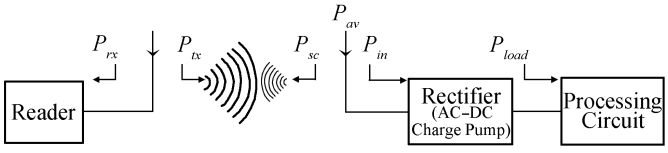

Fig. 1. Transmission link of a UHF RFID system.

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Table 1. Variable definition.

Variable	Definition
P_{rx}	Signal power reader receives
P_{tx}	Signal power reader transmits
P_{av}	Total available power for tag
P_{sc}	The power tag scatters
P_{in}	The power tag chip obtains
P_{load}	Load power of the rectifier

should be greater than the minimum power demand of the tag processing circuit $P_{tag,min}$; for the uplink, P_{rx} should be greater than the reader sensitivity $P_{reader,min}$.

$$P_{load} \geqslant P_{tag,min}, \tag{2}$$

$$P_{rx} \geqslant P_{reader,min}. \tag{3}$$

Considering the PCE of the rectifier and the downlink path loss, Equations (2) and (3) can be expressed as:

$$P_{load} = P_{in} + 10\lg\eta \geqslant P_{tag,min}, \tag{4}$$

$$P_{rx} = P_{sc} - 10\lg(4\pi d/\lambda)^2 + G_r \geqslant P_{reader,min}, \tag{5}$$

where η is the PCE and G_r is the gain of reader antenna.

In a UHF RFID system, backscatter modulation is usually a combination of ASK and PSK[11]. The input and scattered power of the tag are related to the total available power P_{av} by a modulation index m[12]:

$$P_{in} = P_{av}\left(1 - m^2\right), \tag{6}$$

$$P_{sc} = P_{av}\left(m^2/L_a\right), \tag{7}$$

where L_a is the antenna loss factor. Since the maximum transmit power of reader is defined by radio regulation: $P_{tx,max} = P_{EIRP}$. From Eqs. (1) and (4)–(7), read range's dependence on reader sensitivity and tag power consumption can be expressed in a complete form:

$$\begin{aligned} P_{load} &= P_{EIRP} - 201\lg(4\pi d/\lambda) + 10\lg(1-m^2) \\ &\quad + 10\lg\eta + G_t \\ &\geqslant P_{tag,min}, \end{aligned} \tag{8}$$

$$\begin{aligned} P_{rx} &= P_{EIRP} - 401\lg(4\pi d/\lambda) + 10\lg(m^2/L_a) \\ &\quad + G_t + G_r \\ &\geqslant P_{reader,min}. \end{aligned} \tag{9}$$

Equations (8) and (9) explain the reason why smaller values of $P_{tag,min}$ and $P_{reader,min}$ produce a longer read range. Besides, high gain antennas with small loss factor are also desired. The modulation index $m \in (0, 1)$ is the key factor for proper power distribution. Since the gain and loss factor of antennas are independent of the circuit parameters, once the rectifier's PCE is known, the read range for given values of $P_{tag,min}$ and $P_{reader,min}$ can be calculated along with the optimized modulation index. However, PCE of an AC–DC charge pump is strongly dependent on its load conditions. The relationship between PCE and the load power needs to be analyzed.

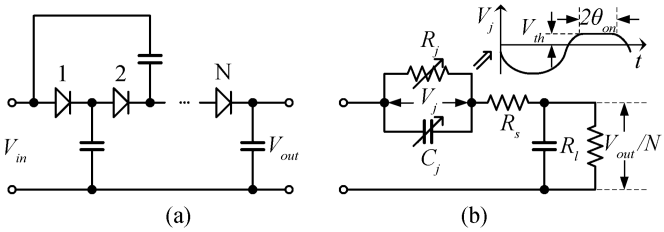

Fig. 2. An N-stage Dickson charge pump. (a) Circuit topology. (b) Equivalent circuit model of one stage.

3. Multi-stage charge pump model

For all types of RFID tags, rectifier is an essential component. The remotely powered characteristic of RFID tag requires the rectifier to be operated with limited input RF signal amplitude, which is often at the level of several hundred mV. Therefore, AC–DC charge pump circuits are often employed as rectifiers for voltage boosting. Though prevalent designs of AC–DC charge pumps have experienced great changes like threshold compensation and differential drive techniques, their fundamental principles are still based on the conventional design of Dickson's charge pump[13−15].

A typical Dickson charge pump circuit is shown in Fig. 2(a), where each pair of diode and capacitor composes a charge pump stage[16]. Figure 2(b) shows the equivalent circuit model of a single stage. The transient waveform of the junction voltage V_j is illustrated aside. PCE of a diode has been studied in Refs. [17, 18]. However, tag's charge pump circuit often has more than one stage. Therefore, a multi-stage charge pump circuit model is derived and expanded to calculate PCE for different load power and different stage numbers.

PCE of the charge pump is defined as the ratio between output DC power and the incident RF power:

$$\eta = P_{dc}/P_{in} = P_{dc}/(P_{dc} + P_{loss}). \tag{10}$$

Three parts compose the power loss P_{loss} of the charge pump circuit; they are: $P_{loss,\,Rs,\,on}$, power loss on the series resistor when the diode turns on; $P_{loss,\,Rs,\,off}$, power loss on the series resistor when the diode turns off; and $P_{loss,\,dio}$, power loss on the diode. By substituting these three parts into Eq. (10), PCE of the charge pump circuit can be deduced and thus given by Eqs. (11)–(14). Detailed deduction of the equations can be referred to Ref. [19].

$$\begin{aligned} \eta &= \frac{1}{1 + \dfrac{P_{loss,Rs,on}}{P_{dc}} + \dfrac{P_{loss,Rs,off}}{P_{dc}} + \dfrac{P_{loss,dio}}{P_{dc}}} \\ &= \frac{1}{1 + \eta_1 + \eta_2 + \eta_3}, \end{aligned} \tag{11}$$

$$\eta_1 = \frac{NR_l}{2\pi R_s}\left(\frac{1}{N} + \frac{V_{th}}{V_{out}}\right)\left[\theta_{on}\left(2 + \frac{1}{\cos^2\theta_{on}}\right) - 3\tan\theta_{on}\right], \tag{12}$$

$$\eta_2 = \frac{NR_sR_lC_j^2\omega^2}{2\pi}\left(\frac{1}{N} + \frac{V_{th}}{V_{out}}\right)^2\left(\frac{\pi - \theta_{on}}{\cos^2\theta_{on}} + \tan\theta_{on}\right), \tag{13}$$

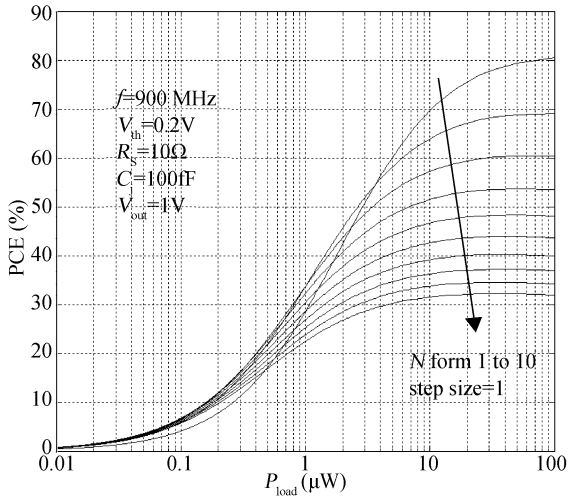

Fig. 3. PCE versus P_{load} for different stage numbers.

$$\eta_3 = \frac{NR_{\text{l}}V_{\text{th}}}{\pi R_{\text{s}}V_{\text{out}}}\left(\frac{1}{N}+\frac{V_{\text{th}}}{V_{\text{out}}}\right)(\tan\theta_{\text{on}}-\theta_{\text{on}}), \qquad (14)$$

where N is the stage number, R_{l} is the load resistance, R_{s} is the series resistance of the diode, C_{j} is the junction capacitance, V_{th} is the turn-on voltage of the diode (or the threshold voltage of a diode connected MOS transistor), V_{out} is the output DC voltage, and θ_{on} is the forward bias turn-on angle. Among these variables, V_{th}, R_{s}, and C_{j} are process variant, R_{l} and V_{out} are dependent on load conditions, N is a circuit parameter, and θ_{on} is determined by all the aforementioned parameters:

$$\tan\theta_{\text{on}}-\theta_{\text{on}} = \frac{\pi R_{\text{s}}}{R_{\text{l}}\,(1/N+V_{\text{th}}/V_{\text{out}})}. \qquad (15)$$

Figure 3 shows the relationship between PCE and the load power, where $P_{\text{load}} = V_{\text{out}}^2 / R_{\text{l}}$. A set of parameters is chosen according to the state of the art designs and is listed in too. PCE increases with the load power when P_{load} is varying from 10 nW to 100 μW. Since power loss on each stage is same for a constant load current, PCE decreases with the stage number, which is also shown in Fig. 3 for curves of $N \geqslant 3$.

4. Power analysis summary

Power distribution in the transmission link and PCE of the AC–DC charge pump are studied separately in the foregoing sections. A brief summary of power issue analysis is drawn by combining the deductions of the two sections together.

By substituting the calculated PCE of Eqs. (11–15) into read range restriction equations (8, 9), the relationship among read range, modulation index, reader sensitivity and tag power consumption is figured out in a mathematical way. For each combination of reader sensitivity and tag power consumption, there is one optimum modulation index m_{opt} to get the maximized read range d_{max}. In order to have an insight into the joint effect of reader sensitivity and tag power consumption, contour maps for d_{max} and m_{opt} are depicted by varying $P_{\text{reader,min}}$ from -50 to -110 dBm and $P_{\text{tag,min}}$ from 0.01 to 100 μW, as shown in Fig. 4. We note that Fig. 4 is acquired by assuming $P_{\text{EIRP}} =$ 36 dBm and choosing the PCE curve of $N = 5$ from Fig. 3, which is a typical stage number for charge pump design in low voltage low power tag[20]. Similar results can be obtained by alternating the value of N. Figure 4 is an evolution from the conventional calculation methods for read range[15]. It gives an intuitive way to evaluate how performance improvement of reader and tag might contribute to the read range performance for all RFID systems using backscatter mechanism. Besides, it also gives a reference for design specifications of semi-passive tag's RF power budget and modulation index. Summary of the analytical results are given on three aspects.

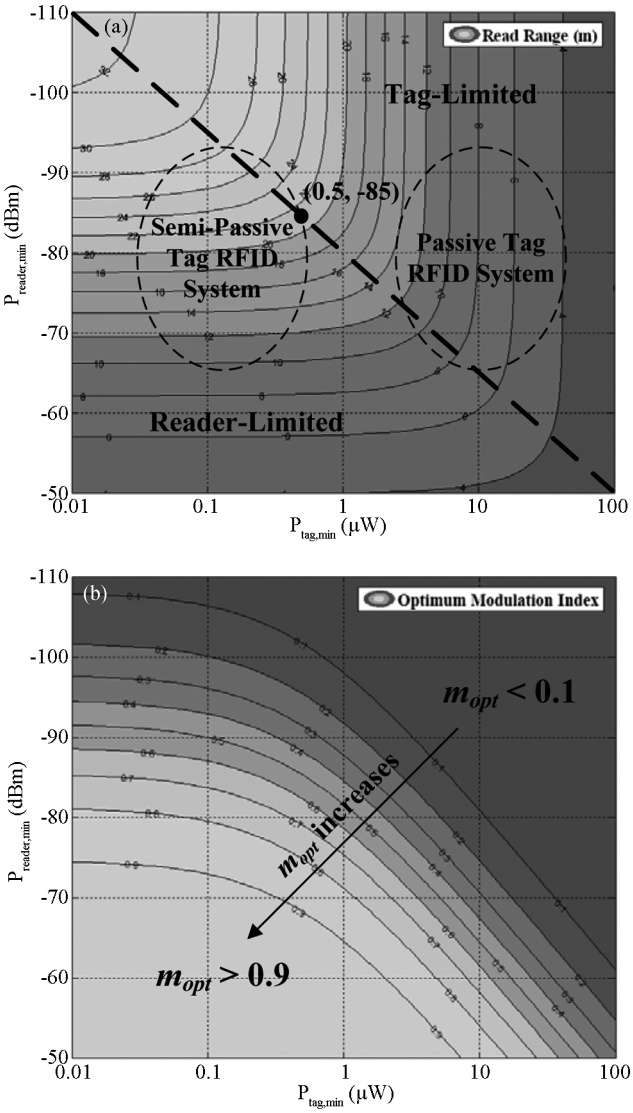

Fig. 4. Calculated d_{max} and m_{opt} versus $P_{\text{tag,min}}$ and $P_{\text{reader,min}}$. (a) Maximized read range. (b) Optimum modulation index.

4.1. Limiting factor for read range

The whole plane of Fig. 4(a) is divided into two parts by the diagonal. According to the limiting factors for read range, the two parts are named reader-limited area and tag-limited area respectively. In the tag-limited area, the results show good accordance with the conventional calculation method, which only regards tag power consumption as a limiting factor for read

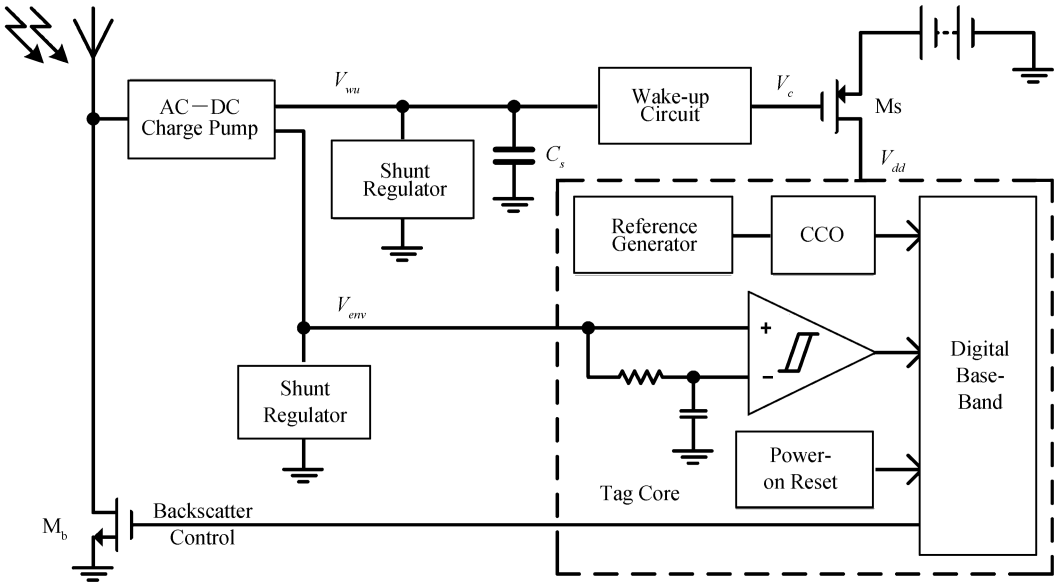

Fig. 5. Circuit architecture.

range. On the other hand, read range is determined by reader sensitivity in the reader-limited area, decreasing tag power consumption contributes little to the read range. The reader-limited area is a good supplement to the conventional method and proves that in future design of low power passive tag and semi-passive tag systems, sensitivity of reader will become an important factor.

4.2. RF power budget

For the state of the art UHF RFID design, power consumption of a passive tag is on the order of 10 μW[2], and sensitivity of a reader is about to be below –85 dBm[21–24]. It is easily found that these two power factors set passive tag system into the tag-limited area. Therefore, challenges for today's passive tag design are power consumption reduction and rectifier PCE enhancement. On the other hand, in designing a semi-passive tag, it is required for the system to be located in reader-limited area for the sake of read range performance. This requirement gives the budget for RF load power of a semi-passive tag. As an example, by using a –85 dBm reader, load power of the tag's rectifier needs to be below 0.5 μW.

4.3. Backscatter modulation

Figure 4(b) shows that the optimum modulation index also depends on the joint effect of reader sensitivity and power consumption. Compared Fig. 4(b) with Fig. 4(a), it is found that passive tag operating in the tag-limited area needs a small $m_{\rm opt}$ to maximize the forward link power transmission, and semi-passive tag operating in the reader-limited area needs to scatter back almost all the power back to meet the needs of signal detection on the reader end.

5. Circuit description

The analytical results give a reference for semi-passive chip design. A test chip is designed under the guidance of power budget and modulation index calculation. The test chip is designed to be compact to keep the chip size small. The prevalent EPC C1G2 standard for UHF RFID systems is employed.

5.1. Circuit architecture

Figure 5 shows the system architecture of the proposed semi-passive tag. Two power sources supply the circuits. They are the rectified dc energy from the antenna, and the battery. In the system, a wake-up circuit and two regulators are powered by the rectifier; the rest functional blocks for signal detection and protocol processing are supplied by the battery. Different requirements are proposed for the load of the two power source. For the rectifier, its load power needs to be minimized for read range consideration. For the battery, its static power consumption needs to be zero when the tag is standing by. However, sporadic large power of the battery is allowed when the tag goes into the interrogating field and all the tag circuits are fully functional. The upper limit for the operating power is the battery's output driving ability.

In Fig. 5, an AC–DC charge pump serves as a rectifier and an envelope extractor. It generates a DC voltage $V_{\rm wu}$ for wake-up detection, and extracts the envelope of the carrier $V_{\rm env}$ for demodulation purpose. Two shunt regulators protect the circuit in case of large interrogating power. As the downlink signal of an EPC C1G2 RFID system is ASK modulated, input energy of the tag varies a lot. In order to keep the wakeup voltage $V_{\rm wu}$ a constant value, a storage capacitor $C_{\rm s} = 100$ pF is connected between $V_{\rm wu}$ and ground. A low power wake-up circuit controls the power switch Ms by detecting the voltage level of $V_{\rm wu}$. Circuits in the dotted-line frame compose the tag core. It derives power supply from the battery when Ms is turned on. In the tag core, a reference generator is employed to provide voltage and current reference[25]. Clock signal for the digital baseband is obtained by using a current controlled oscillator (CCO). The demodulator is composed by a hysteresis comparator and an RC filter. It detects the envelope signal $V_{\rm env}$ and extracts the modulated PIE code. Power-on reset signal is generated when $V_{\rm dd}$ is turned high[26]. Uplink signal is modulated onto the carrier by directly connect the input RF port to ground. When the modulation transistor M_b is off, impedance matching is carried out to maximize the forward power transmission. On the other hand, when M_b is turned on, short circuit behavior of RF in-

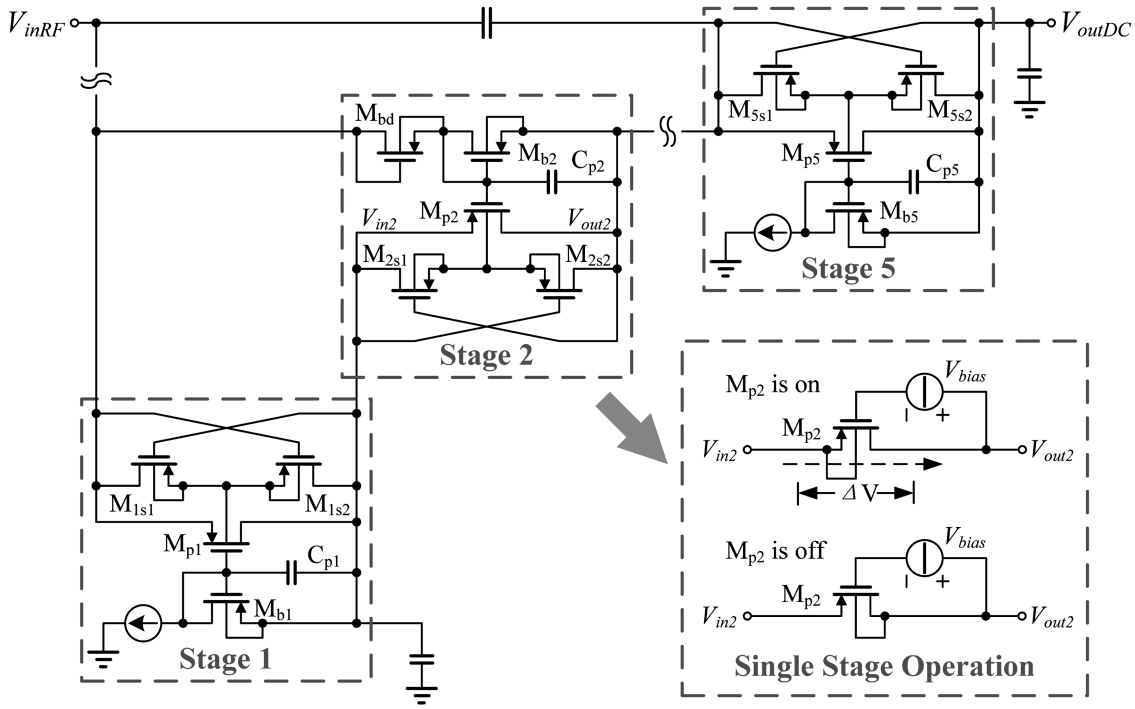

Fig. 6. AC-DC charge pump.

put and ground sets the backscatter modulation index to 1, as indicated by Fig. 4(b).

5.2. Threshold compensated charge pump

A 5-stage charge pump with high PCE is designed. Because for semi-passive tags, the receiving RF signal amplitude can be as small as 200–300 mV[27], devices with small turn-on voltage are required in the charge pump circuit. Since the test chip is implemented in standard CMOS technology, threshold compensation technique for MOS transistors is employed[20]. Figure 6 shows the charge pump circuit. Output of the 3rd and 5th stages are used as the extracted envelope $V_{\rm env}$, and wakeup triggering signal $V_{\rm wu}$ respectively. By regarding each stage (framed by the dotted line) as a diode, the circuit is similar to the traditional Dickson charge pump shown in Fig. 2. Operation of the circuit is explained by illustrating the second stage as an example. Two auxiliary MOS transistors M_{2s1} and M_{2s2}, as switch transistors, are introduced to update the body voltage of the pass transistor M_{p2}, for the purpose of reducing the body effect in substrate. M_{b2} is introduced to provide bias voltage $V_{\rm bias}$. If $V_{\rm in2}$ is higher than $V_{\rm out2}$, M_{p2} is on and $V_{\rm bias}$ is used to compensate the threshold voltage of M_{p2}. When M_{p2} is on, $V_{\rm bias}$ is optimized to be close to $V_{\rm GS,p2}$ according to the equivalent load and input magnitude. PCE of the circuit can be optimized by choosing a proper voltage drop ΔV to set the forward bias turn-on angle $\theta_{\rm on}$ as illustrated in section 2. Bias voltages for odd and even stages are generated in different ways. For odd stages, bias is provided by constant current sources, and for even stages, it is provided by bias resistances (diode connected $M_{\rm bd2,4}$). The UHF application requires careful layout design to minimize the interference of the parasitics, especially on the nodes connecting the RF input to the ground.

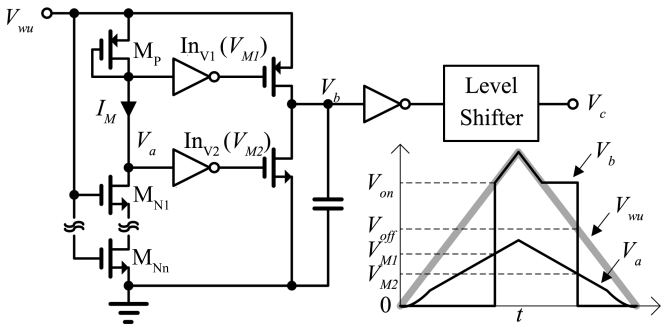

Fig. 7. Wake-up circuit.

5.3. Low power wake-up circuit

As defined by the EPC C1G2 standard, tag needs to be power-on once it is located in the reader's interrogating field. Wake-up mode for the EPC C1G2 compatible tag is power triggered. According to the power issue analysis results depicted in Fig. 4, power consumption of the wake-up circuit needs to be strictly controlled. Therefore, a low power voltage sensing circuit is proposed for wake-up detection.

The circuit architecture is shown in Fig. 7 along with the transient voltages of critical nodes. The serially connected NMOS transistors are set into linear region. The current $I_{\rm M}$ needs to be kept small by reducing the W/L ratio of $M_{{\rm N1}-n}$. Two inverters ($\rm Inv_1$ and $\rm Inv_2$) play the role of voltage comparison. Conversion voltage $V_{\rm M1}$ is set to be higher than $V_{\rm M2}$. When $V_{\rm a} > V_{\rm M1}$, $V_{\rm b} = V_{\rm wu}$; when $V_{\rm a} < V_{\rm M2}$, $V_{\rm b} = 0$; when $V_{\rm a} \in (V_{\rm M1}, V_{\rm M2})$, $V_{\rm b}$ remains unchanged. A level shifter converts the signal level to be the same as the battery. By applying Kirchhoff's law to the circuit, turn-on voltage $V_{\rm on}$ is determined by Eqs. (16, 17).

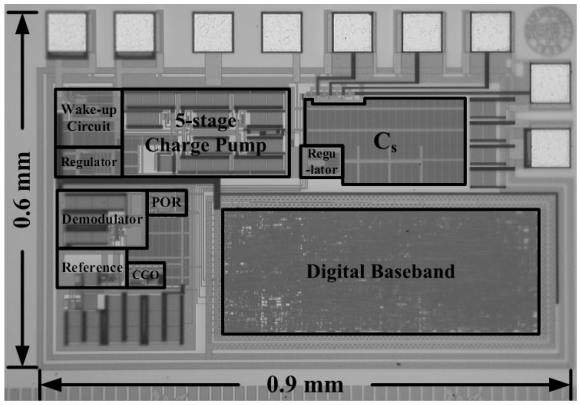

Fig. 8. Chip micrograph.

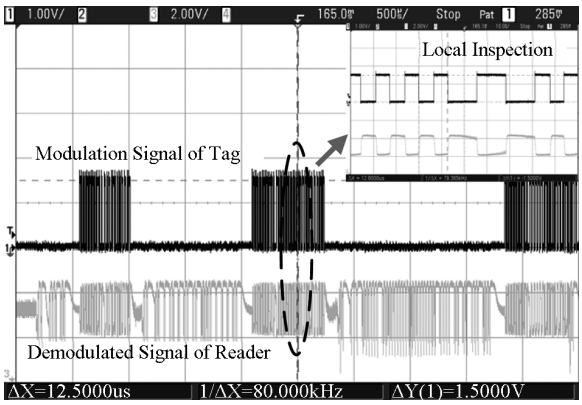

Fig. 10. Waveforms of uplink communication.

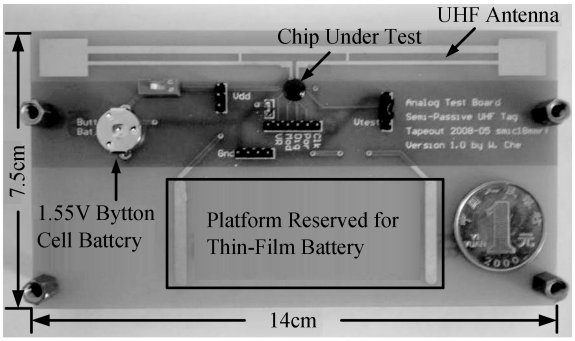

Fig. 9. Test board photograph.

$$V_{\rm on} - V_{\rm GS,P} = V_{\rm M1} = (r_1/1 + r_1)\, V_{\rm on}, \tag{16}$$

$$V_{\rm on} = (1 + r_1)\, V_{\rm GS,P}, \tag{17}$$

where r_1 is the conversion voltage coefficient of $\rm Inv_1$. The serially connected NMOS transistors $\rm M_{N1-\mathit{n}}$ can be regarded as one transistor MN with large channel length. Gate to source voltage of $\rm M_P$ is determined by the I–V relationships of $\rm M_P$ and $\rm M_N$:

$$I_{\rm M} = k_{\rm P}\,(W/L)_{\rm P}\,(V_{\rm GS,P} - V_{\rm TH,P})^2\,, \tag{18}$$

$$I_{\rm M} = 2k_{\rm N}\,(W/L)_{\rm N}\,(V_{\rm on} - V_{\rm TN})\,V_{\rm M1}. \tag{19}$$

Turn-off voltage $V_{\rm off}$ can be obtained in a similar way. The hysteresis behavior of turn-on and turn-off voltages is employed to withstand noise and voltage ripple on $V_{\rm wu}$.

6. Experimental results

The semi-passive tag is implemented in SMIC 0.18 μm standard CMOS technology. Figure 8 shows the chip micrograph. The chip size is 0.54 $\rm mm^2$including the test pads. Test of the chip includes: (1) communication with reader under EPC C1G2 protocol; (2) battery voltage adaptability; (3) wakeup function; (4) power consumption. Figure 9 shows the test board. An alkaline button cell battery with 1.55 V output voltage is employed as the battery power source. The power source can also be replaced by DC voltage source or other batteries using the on-board switch. A platform for thin-film battery deposition is also designed on the board for future adaptation of printable thin-film batteries.

A common EPC C1G2 reader is employed for communication function test. The reader is same with that used in passive RFID systems, no extra adaptation is made. Figure 10 shows the waveform of the uplink transmitted and received data. Test results show that the tag supports 840 to 960 MHz carrier frequency with downlink data rates from 40 to 160 kb/s. Similar communication function tests were carried out by using different battery sources. The tag chip shows good compatibility to battery output voltage ranging from 1.2 to 2.4 V.

Test of the wake-up function is carried out by observing the system control signal $V_{\rm c}$ and the corresponding current driven from the battery. According to the voltage curves of Fig. 7, measured turn-on voltage $V_{\rm on}$ = 0.8 V, $V_{\rm off}$ = 0.6 V. Current consumption of the battery is too small to be measurable when the rectified voltage $V_{\rm wu}$ is less than 0.6 V. But after $V_{\rm wu}$ reached 0.8 V, current consumption increases dramatically. Since current consumption of the tag core varies a lot for different EPC C1G2 commands, overall current consumed by the semi-passive tag chip is not a constant value. Measured average current value during the wakeup state is about 10 μA. Load power of the rectifier is 230 nW. It meets the requirement of being set to the reader-limited area shown in Fig. 4.

Measured sensitivity of the tag is –18 dBm at 915 MHz. At this power level, the input impedance is 22 – j680. For a –85 dBm reader, theoretical read range can be 13 m. The measured sensitivity and the corresponding read range is somehow worse than the theoretical results given by the mathematical analysis. This is because of the relatively high Q input impedance, which makes the impedance matching difficult during chip test. Moreover, the unavoidable bounding parasitics also degrades the tag's sensitivity performance to some extent.

A summary of the experimental results is listed in Table 2 with comparison to some of the recent works. The proposed tag chip distinguishes itself with performances of low power consumption and compact chip size.

7. Conclusion

We present the analysis and design of a power efficient semi-passive tag. The transmission link of a backscatter RFID system is studied to optimize power distribution. To assess how the performance improvement of the reader and tag might impact the read range, concepts of reader-limited and tag-limited RFID systems are introduced. It is proven that the read range of

Table 2. Result comparison.

	Protocol	Wake-up mode	Process	Chip size (mm^2)	Rectifier load power (nW)	Compatible battery voltage (V)	Sensitivity (dBm)
Kim[6]	EPC C1G2	Power triggered	0.25 μm 2P4M CMOS with FeRAM and Schottky diodes	1	NA	2.0	NA
Pillai[7]	ISO 18000-4B	Power triggered	1 μm dual poly standard CMOS	5	600	NA	–19
This work	EPC C1G2	Power triggered	0.18 μm 1P6M standard CMOS	0.54	230	1.2–2.4	–18

a semi-passive tag can be reader-limited by cutting down its RF load power to be below 0.5 μW. Under the instructions of the theoretical analysis, a test chip compatible to EPC C1G2 standard is implemented in SMIC 0.18 μm standard CMOS technology. The proposed tag has a small chip size of 0.54 mm^2 and is adaptable for a wide range of batteries. This work serves as a meaningful attempt to help the design of low cost higher class RFID tags in the future.

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