An ultra-high-speed direct digital frequency synthesizer implemented in GaAs HBT technology*

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Abstract: This paper presents a 10-GHz 8-bit direct digital synthesizer (DDS) microwave monolithic integrated circuit implemented in 1 μm GaAs HBT technology. The DDS takes a double-edge-trigger (DET) 8-stage pipeline accumulator with sine-weighted DAC-based ROM-less architecture, which can maximize the utilization ratio of the GaAs HBT's high-speed potential. With an output frequency up to 5 GHz, the DDS gives an average spurious free dynamic range of 23.24 dBc through the first Nyquist band, and consumes 2.4 W of DC power from a single –4.6 V DC supply. Using 1651 GaAs HBT transistors, the total area of the DDS chip is 2.4×2.0 mm^2.

Key words: DDS; double-edge-trigger; CML; ECL; GaAs HBT; sine-weighted DAC
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1. Introduction

Compared with other frequency synthesizing techniques such as VCO and PLL, direct digital synthersizer (DDS) gives much higher frequency resolution, faster frequency channel switching with continuous phase, a wider tuning range of frequency and more flexible versatile modulation capability. So DDS can be widely used in various communication systems, radars and test-measurement instruments. However, the output frequency of DDS is generally much lower than its competitors due to its conventional ROM-based operating mechanism.

With the recent improvement of some advanced semiconductor technologies such as SiGe BiCMOS and InP HBT, several ultra-high-speed DDS integrated circuits with clock frequencies from 8 to 32 GHz have been reported. The design reported in Ref. [1] uses a traditional DDS architecture with ROM-based phase to amplitude conversion, while the DDS in Ref. [2] utilizes a ROM-less architecture with bipolar differential pairs in saturation to perform triangle to sine wave conversion in the analog domain. Similar to the designs in Refs. [3–6], this proposed DDS employs a ROM-less structure with a sine-weighted DAC combining the sine mapping block and the digital to analog amplitude conversion block together. There are also some designs using the CORDIC algorithm to perform the conversion[7]. Besides using advanced technologies such as InP and SiGe, designing new circuit architectures is another way to improve the speed of DDS. Noting that the speed of ROM-less DDS is often limited by the speed of the phase accumulator[4], we developed a double-edge-trigger (DET) technique for the 8-stage pipeline accumulator that can finish two accumulating operations in a single clock cycle, thus significantly improving the speed of the DDS by 2 times. So, even implemented in the relatively backward GaAs HBT technology, this proposed DDS can achieve a comparable speed to InP or SiGe technology-based DDSs. It should be noted that the DTE technique proposed here is not exclusive to GaAs HBT technology and can be transplanted conveniently to InP or SiGe-based designs to achieve even higher performance.

Implemented in 1 μm GaAs HBT technology, of which the unit short-circuit current gain frequency (f_t) is about 60 GHz, the DDS IC presented here achieves a maximum clock frequency of more than 10 GHz, showing the highest semiconductor technology's high-speed potential utilization ratio FOM of 16.67% compared to other reported designs.

2. DDS architecture

Typically a traditional ROM-based DDS consists of an accumulator, a ROM for phase to amplitude conversion and a digital-to-analog converter (DAC). Generally the ROM is the bottleneck of the DDS's high-speed performance, so some ROM-less DDS architectures are used to improve the DDS's clock frequency[2–6].

The top-level architecture of the proposed DDS is shown in Fig. 1. Similar to the DDS architecture in Ref. [3], this proposed DDS mainly consists of an 8-bit pipeline phase accumulator, a 2-bit XOR complementer, a 3-bit thermometer coder, a sine-weighted DAC and a Gilbert cell. The three LSBs of the accumulator's output are truncated to reduce the size and power consumption of the chip with little spurious penalty. Because of this 3-bit truncation, the amplitude resolution of the sine-weighted DAC is 5-bit. The 1st-MSB output of the accumulator's output is used as one input of the Gilbert cell to provide the proper mirroring of the sine waveform about the π phase point. The 2nd-MSB of the accumulator's output is used to complement the remaining 3-bit output for the second and fourth quadrants of the sine waveform prior to the thermometer coder. The 7-bit thermometer outputs drive the switches of the sine-weighted tap current sources of the DAC. All the currents are added together and then are converted to a voltage signal as the second input of the Gilbert cell. The output of the Gilbert cell forms the DDS output.

What is different from the DDS architecture in Ref. [3] is that we designed a DET 8-stage pipeline accumulator: in each

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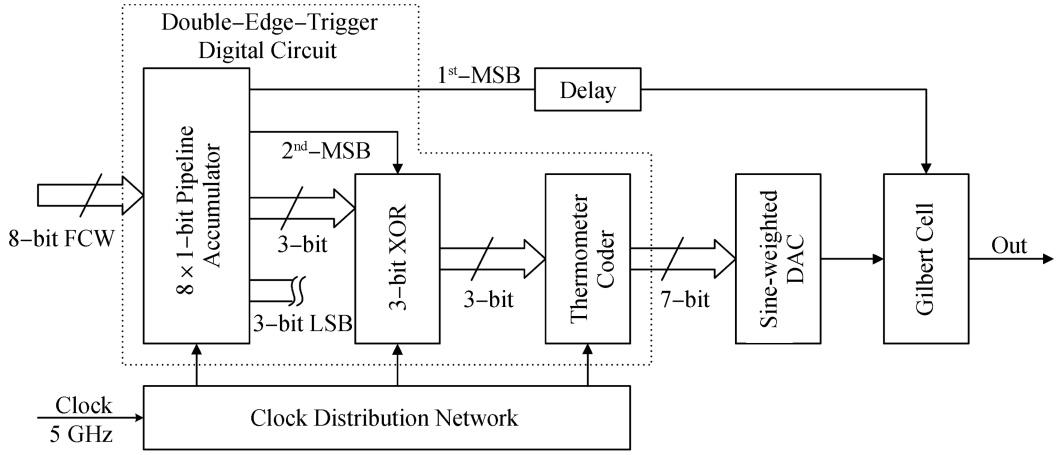

Fig. 1. Block diagram of the 10 GHz 8-bit ROM-less DDS.

stage there is a 1-bit accumulator, rather than a single-edge-trigger 4-stage pipeline accumulator in Ref. [3]. By this novel accumulator design, we can improve the speed by at least 2 times.

3. Circuit implementation

To pursue the highest speed, all of the digital circuits make use of current-mode-logic (CML) or emitter-coupled-logic (ECL) which is popular in ultra-high-speed bipolar digital designs.

3.1. 8-bit DET Pipeline Accumulator

Figure 2 shows a block diagram of the DET 8-bit pipeline accumulator and the 1-bit accumulator unit ACC1. Each of the eight ACC1's includes two 1-bit adder Sum's and two 1-bit carrier Carry's. One Su–Carry pair is triggered at the rising edge of the clock signal while the other pair is triggered at the sequent clock falling edge. The two corresponding sum results S_p and S_n are fed back into the falling-edge-triggered and rising-edge-triggered Sum–Carry pairs respectively inside the ACC1 for accumulating operation. Meanwhile the two corresponding carry results Cout_p and Cout_n are passed out to the next stage ACC1. Thus the pipeline accumulator operates at the speed of ACC1, generating two accumulating results in a single clock cycle. There is one Latch in the Sum block following the sum logic gate, as well as in the Carry block. So the critical path propagation delay of the ACC1 for each accumulating operation is $T_1 = \tau_{\text{gate}} + \tau_{\text{latch}}$, where τ_{gate} is the larger of the propagation delays of the sum and carry logic gates, and τ_{latch} is the propagation delay of the Latch. Compared to the critical path propagation delays of $T_2 = 2\tau_{\text{gate}} + 2\tau_{\text{latch}}$ in the designs of Refs. [1, 2] and $T_3 = \tau_{\text{gate}} + 2\tau_{\text{latch}}$ in the designs of Refs. [3, 4], the DET accumulator can achieve a higher maximum operating frequency. The latches at the output of each ACC1 facilitate data alignment for the following operations of the complementer and thermometer coder which also use DET structure.

3.2. MUX

For each bit of the 7-bit width thermometer coder output, a MUX circuit shown in Fig. 2 is used to merge the two data streams that are generated at the rising and falling edges of the clock respectively. The same as the other digital blocks in the DDS, the MUX is based on full differential ECL topology, which is well suited for GaAs HBT devices. Two different signal pairs (IN_1, $\overline{\text{IN}_1}$) and (IN_2, $\overline{\text{IN}_2}$), representing the two data streams, are gated by the differential clock signal (CLK,$\overline{\text{CLK}}$) to form one data stream, the data rate of which is doubled. After two stage amplifications, the data stream is buffered out by an emitter follower to drive the switches of the sine-weighted DAC.

3.3. Sine-weighted DAC

A block diagram of the proposed sine-weighted DAC and a schematic of the Gilbert cell are shown in Fig. 3. The table in Fig. 3 illustrates how the [3 5 5 4 4 3 2 1] tap weighting scheme of the DAC is calculated out. The switches of the current sources in the DAC are controlled by the 7-bit width thermometer-code, thus the weights sum successively to generate a quarter-wave sine output. In order to ensure that the current summing junction has non-zero outputs for all possible states, the first tap weight 3 is always enabled[3]. The summing current is then converted to a voltage signal simply by a pull-up resistor. This differential voltage signal (DAC, $\overline{\text{DAC}}$) is multiplied by the properly delayed 1st-MSB (MSB, $\overline{\text{MSB}}$) of the accumulator output in the Gilbert cell, resulting in a full-wave sine output. Linearity of the Gilbert cell is important for the quality of the DDS output since nonlinearities reduce the SFDR. There is a resistor between the emitters of the input transistor pair, to improve the linearity of the Gilbert cell by introducing a negative feedback. Two 50 Ω pull-up resistors are used at the output port to perform a wideband impedance match to the measurement system.

4. Experiment results

A microphotograph of the fabricated DDS is shown in Fig. 4. The fabricated DDS is implemented in the 1 μm GaAs HBT process with an f_t of 60 GHz, and has 1651 transistors in a die area of 2.4 × 2 mm^2. The DDS is tested on-wafer using GSG single-ended microwave probes. With the Nyquist output, the DDS achieves a maximum internal effective clock frequency of more than 10 GHz when consuming 528 mA current from

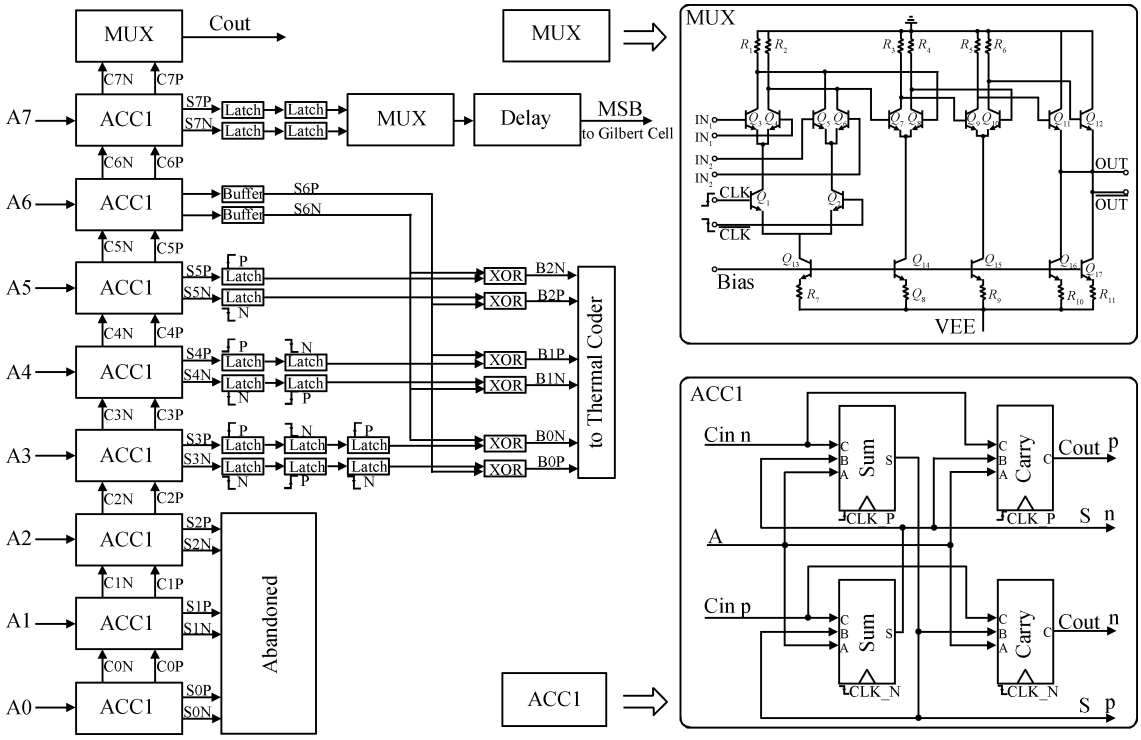

Fig. 2. Block diagram of the DET 8-stage pipeline accumulator and the 1-bit accumulator unit, and the schematic of MUX.

Angle	Difference	Normalized
$\theta_1 = \pi/32$	$b_1 = \sin\theta_1 - 0$	$a_1 = b_1/b_8 \rightarrow 3$
$\theta_2 = 3\pi/32$	$b_2 = \sin\theta_2 - \sin\theta_1$	$a_2 = b_2/b_8 \rightarrow 5$
$\theta_3 = 5\pi/32$	$b_3 = \sin\theta_3 - \sin\theta_2$	$a_3 = b_3/b_8 \rightarrow 5$
$\theta_4 = 7\pi/32$	$b_4 = \sin\theta_4 - \sin\theta_3$	$a_4 = b_4/b_8 \rightarrow 4$
$\theta_5 = 9\pi/32$	$b_5 = \sin\theta_5 - \sin\theta_4$	$a_5 = b_5/b_8 \rightarrow 4$
$\theta_6 = 11\pi/32$	$b_6 = \sin\theta_6 - \sin\theta_5$	$a_6 = b_6/b_8 \rightarrow 3$
$\theta_7 = 13\pi/32$	$b_7 = \sin\theta_7 - \sin\theta_6$	$a_7 = b_7/b_8 \rightarrow 2$
$\theta_8 = 15\pi/32$	$b_8 = \sin\theta_8 - \sin\theta_7$	$a_8 = b_8/b_8 \rightarrow 1$

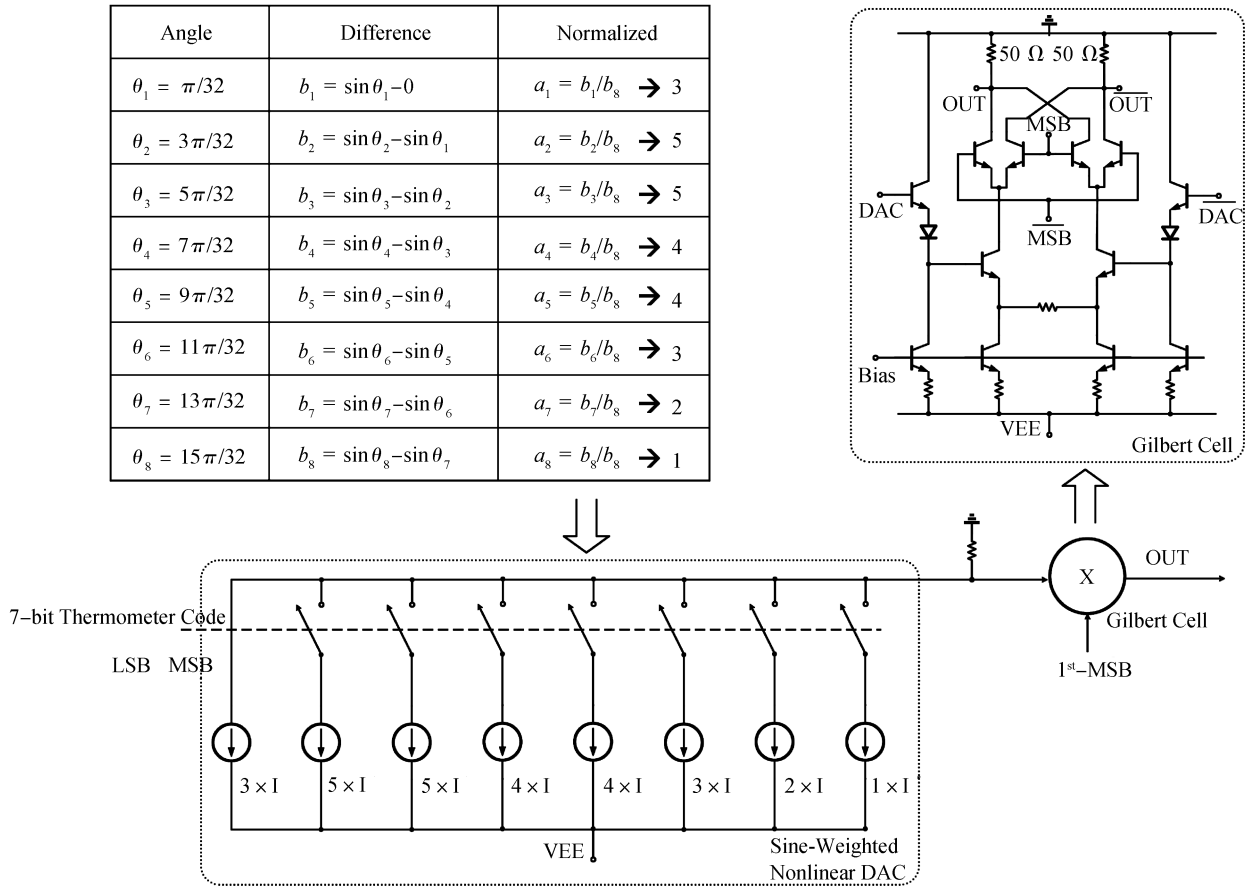

Fig. 3. The sine-weighted nonlinear DAC and Gilbert cell.

Table 1. Experimental performance and comparison with recently reported designs.

Technology f_t (GHz)	InP 370[1]	SiGe 170[2]	InP 300[3]	SiGe 120[4]	SiGe 200[5]	GaAs 60[This work]
Max clock f_{clk} (GHz)	24	15	32	12	5	10
Phase resolution B (bit)	12	8	8	9	24	8
Amplitude resolution A (bit)	7.5	6	5	8	10	5
Worst case DDS SFDR (dBc)	30.7	21	21.56	22	38	19.3
Die area (mm^2)	5.0 × 3.3	1.1 × 1.0	2.7 × 1.5	2.5 × 0.7	3.7 × 3.0	2.4 × 2.0
Power consumption P (W)	19.8	0.366	9.45	1.9	4.7	2.4
FOM1 = $f_{clk} \times B \times$ SFDR/P	447	6885	584	1251	970	643
FOM2 = $f_{clk}/f_t \times 100\%$	6.49%	8.82%	10.67%	10.0%	2.50%	16.67%
FOM3 = $f_{clk} \times A \times B \times$ SFDR/($P \times f_t$)	9.08	243	9.75	83.44	48.5	53.61

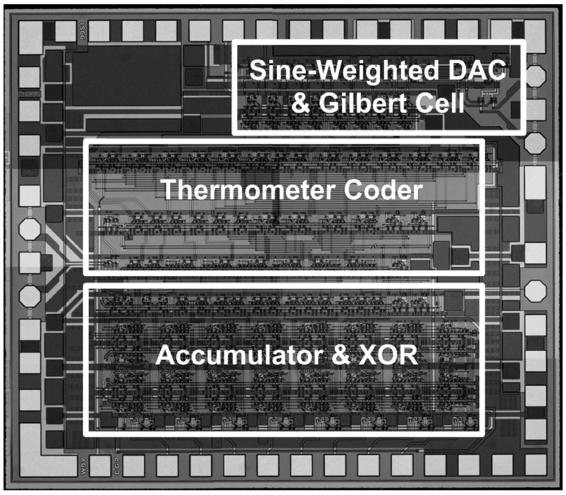

Fig. 4. Die photo of the DDS chip.

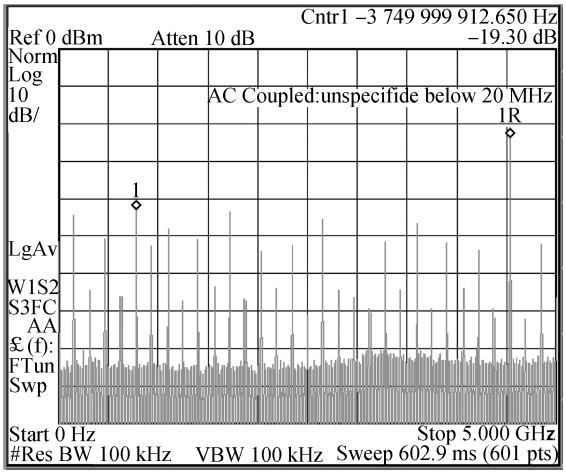

Fig. 6. DDS output spectrum of the worst case SFDR of 19.3 dBc at FCW = 16. The output frequency is 4.531 GHz with an external clock of 5 GHz.

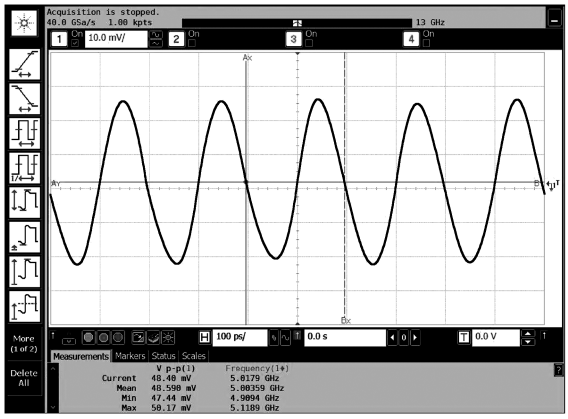

Fig. 5. DDS output waveform of 5 GHz (FCW = 128) with a 5 GHz external clock.

a single –4.6 V power supply. Figure 5 shows the measured DDS output waveform of 5 GHz with 5 GHz external clock when the frequency control word (FCW) is set to be 128. The measured SFDR of the DDS through the whole Nyquist band is 23.24 dBc on average, with the worst case SFDR of 19.3 dBc at an FCW of 116, as shown in Fig. 6. It should be noted that the SFDR performance can be better if measured under differential driven conditions.

Table 1 summarizes the experimental performance of the proposed DDS, along with five recently reported ultra-high-speed designs. Three figures of merit (FOM) are calculated for all of the 6 designs for comparison. Due to the designed DTE architecture, this work shows the best utilization ratio of the technology's f_t (FOM2) of 16.67% which is 1.56 times that in second place. It also demonstrates a good FOM3 which includes more information on the metrics that are important for DDS performance.

5. Conclusion

This paper presented a 10 GHz 8-bit DDS implemented in a 1 μm GaAs HBT process with an f_t of 60 GHz. Due to the proposed DET accumulator, this DDS gives the best f_{clk}/f_t ratio compared with the other reported designs.

There are some limitations in this DDS. Future work will improve the linearity of the Gilbert cell and extend the bit width of FCW to 32-bit, and reduce the power consumption.

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