An 8-b 300MS/s folding and interpolating ADC for embedded applications*

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Abstract: A 1.4-V 8-bit 300-MS/s folding and interpolating analog-to-digital converter (ADC) is proposed. Fabricated in the 0.13-μm CMOS process and occupying only 0.6-mm^2 active area, the ADC is especially suitable for embedded applications. The system is optimized for a low-power purpose. Pipelining sampling switches help to cut down the extra power needed for complete settling. An averaging resistor array is placed between two folding stages for power-saving considerations. The converter achieves 43.4-dB signal-to-noise and distortion ratio and 53.3-dB spurious-free dynamic range at 1-MHz input and 42.1-dB and 49.5-dB for Nyquist input. Measured results show a power dissipation of 34 mW and a figure of merit of 1.14 pJ/convstep at 250-MHz sampling rate at 1.4-V supply.

Key words: analog-to-digital convertor; low-power; low-voltage; embedded; folding and interpolating
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1. Introduction

Ultra-wideband (UWB) is a new technology which is proposed to ease the short-range wireless communication for domestic use. According to the Chinese UWB standard, two high-speed analog-to-digital Converter (ADC) operating at a 264-MHz sample rate are needed in the I/Q channels to process signals down-mixed from the front-end receiver. To ensure the precision of the signal, the resolution of the ADCs should be as many as 8 bits. Since the ADC is to be integrated into the UWB system, extra requirements are necessary to reach as an embedded IP design to fit the whole system. Power dissipation is of the most important issues in the UWB system design. That is to say, the ADCs are highly desirable to work under a low supply voltage and consume as less power as possible.

Folding and interpolating structured ADCs well balance speed and resolution, offering a wide-range application for high-speed and middle-resolution circumstances. They perform the speed as fast as that of flash ADCs but consume what the pipelined ADCs can reach. Therefore, folding and interpolating structured ADCs are extremely suitable for the UWB system.

In this paper, an 8-bit 300-MHz folding and interpolating ADC is presented. It is fabricated in 0.13-μm CMOS process. Measured results are also illustrated.

2. Architecture design

The block diagram of the overall converter is shown in Fig. 1. It employs a single track-and-hold (T/H) block to isolate the input signal from the input capacitors of the preamplifier array, which adds up to a comparable value to the sampling capacitor. A resistor ladder between two reference voltages generates 35 tap voltages dividing the whole quantified range into 34 sections for the preamplifier array which is composed by 36 overall differential amplifiers including dummies. One dummy for each side are added to reduce the mismatch introduced from the process. Followed by is a 2-stage cascaded folder with folding factor 3× for each stage. A pipelining sampling switch and an averaging resistor array are inserted between the two stages. Due to the low supply voltage, folded signals with 35 zero-crossings are interpolated by 2× for three times after passing through a 3-stage cascaded active interpolating block in order to reach substantial gain. 5-bit cycle thermometer codes are generated after the signals are fed into 35 comparators that accomplish the task like the fine quantizer does in the traditional fine part. Coarse quantizer is removed in this work for the power consideration, since the higher 3-bit MSBs can be generated by the in-between signals produced by the fine part and a signal produced by preamplifier stage. All of the cycle thermometer codes are merged together and translated into binary codes by an encoder in the digital part.

Non-ideal factors of the ADC are reduced through some structural methods. The offset voltages of each cascaded stage can be divided by the cascaded voltage gain gathered by the former ones, thus can add up to an equivalent offset of the first input stage. Since the gain is high, equivalent offset can be lowered to be less than 1 LSB which will not lead to wrong judgments. Averaging resistor network also contributes to the mismatch reduction. Offsets of the pre-amplifier array as well as those of the first stage folding array can be averaged through the joint resistors.

3. System low-power optimization

Current-saving is one of the critical directions in a low-power design. As Figure 1 has demonstrated, 6 of 8 stages from preamplifier array to 3rd interpolating array are driven by tail currents. Currents enable these stages to have voltage gain so that the cascaded gain can reach certain value. The initial 1LSB analog input is amplified by the high cascaded gain to reach decades of millivolts before it is fed into comparator. Therefore, the demands for small input mismatch of the comparator

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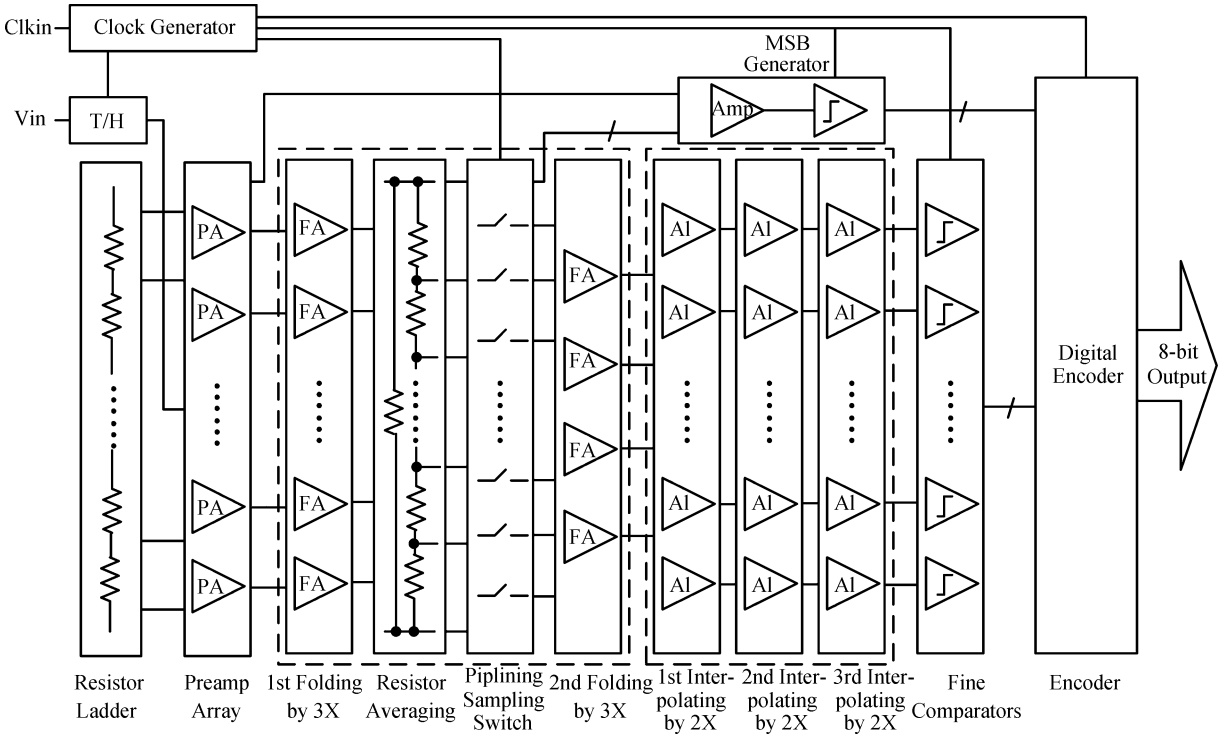

Fig. 1. Block diagram of the folding and interpolating ADC.

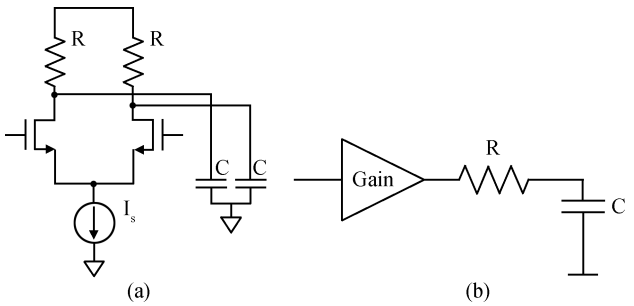

Fig. 2. (a) Simple differential amplifying structure. (b) Equivalent model of the amplifying structure (single-end).

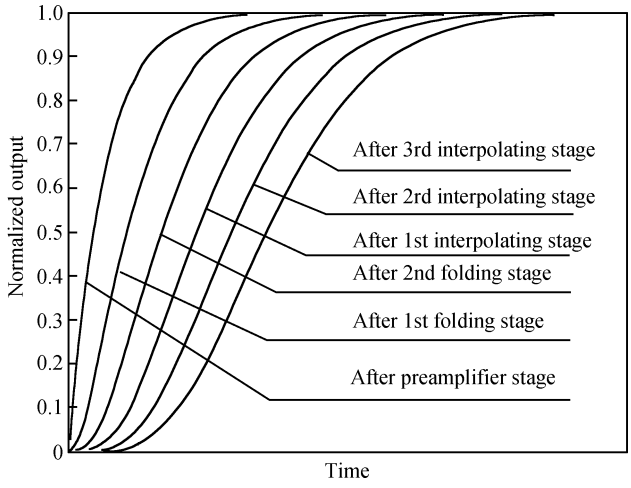

Fig. 3. Step response diagram of the cascaded structure for each stage.

itself can be lowered, which in return, can reduce the currents needed by the comparators.

Not only the preamplifier stage but the folding stages and interpolating stages share a simple differential amplifying structure as Figure 2(a) shows. The voltage gain of each stage is $g_m R$, also can be shown as $I_S R/V_{eff}$, in which I_S is the tail current of the differential pair and V_{eff} is the overdrive voltage of the input MOSFET. If the overdrive voltage and the voltage gain are sustained, the resistor loads have to be increased if we lower the currents. The single-end equivalent model of Fig. 2(a) is presented in Fig. 2(b). The capacitor load is the input capacitor of the following stage. If we unitize the gain and suppose each stage has the same RC product, a cascaded structure will have a step response shown in Fig. 3. The signal settling time has been extended due to the cascaded RC delay. In order to sample the stable signal that precision demands for, small resistor values are chosen. This consequently leads to the rise of the currents if voltage gain is wished to be maintained to overcome the mismatch problem mentioned above.

Pipelining sampling switches[1] are inserted between first and second folding stages to add an extra half clock cycle. Both of the two parts before and after the switches can promise the signals to be settled in sufficient time since total cascading delays are largely reduced. In this way, the combination of larger resistors and smaller currents becomes feasible for preamplifier array and first-stage folding array. Power cuts down markedly at these stages that have numerous current sources.

Averaging resistor array is also optimized for a low-power consideration. Commonly averaging resistors are placed after the preamplifier array like Fig. 4(a). In a physical design, preamplifiers are arranged in sequence to make the connection of the averaging resistors easier. But the subsequent folders pick up the outputs of the preamplifier array every other twelve

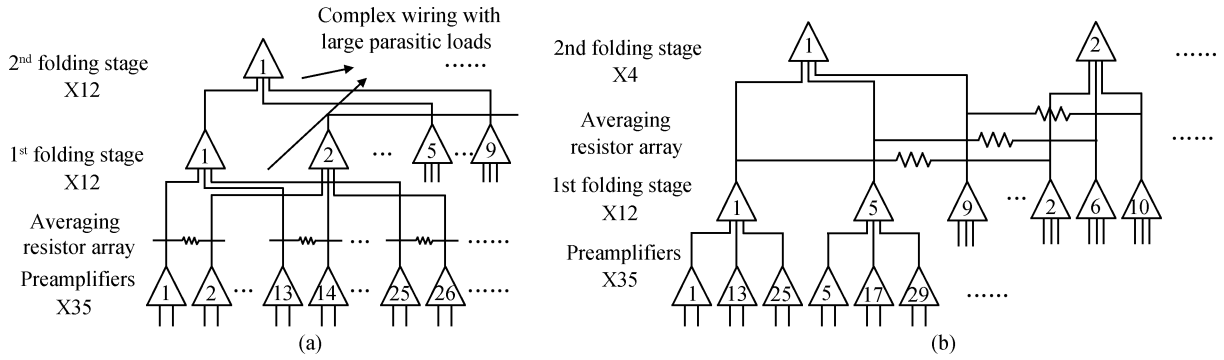

Fig. 4. (a) Physical arrangement in sequence has large parasitic loads. (b) Optimized arrangements decrease wiring complexity.

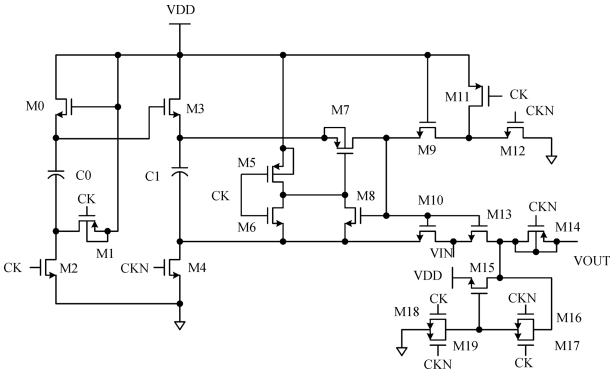

Fig. 5. Improved bootstrapped switch circuit.

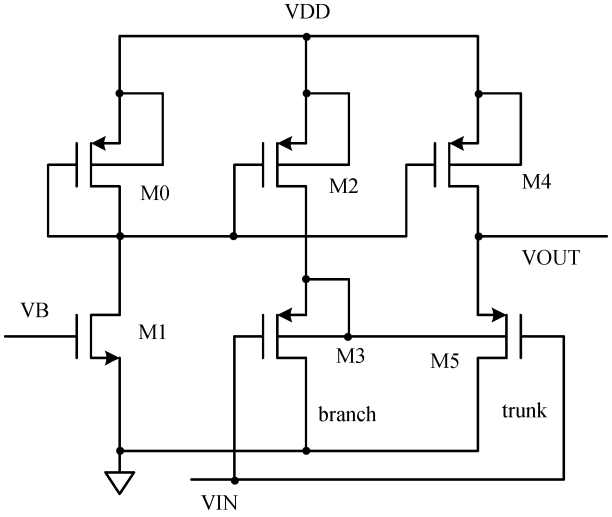

Fig. 6. Improved source-follower buffer.

in our design. Connecting wires go across several hundred micro-meters which will introduce an asymmetry and large parasitic loads as well. Parasitic loads should be paid much attention to in a high-speed design because they narrow the bandwidth of each stage. Extra powers are needed to deal with it.

In Fig. 4(b), we adjust the sequences of the preamplifier array and folding stages to simplify the connection between two stages. Averaging resistor array is moved to follow the first folding stage. This can decrease connecting complexity tremendously since there are only12 units comparing to the 35 of the preamplifier array. Accordingly, the parasitic loads are controlled and bandwidth requirement is allowed to be relaxed in exchange with a power reduction. Moreover, the averaging array not only balances the outputs of the preamplifier array but also the outputs of the first folding stage.

4. Circuit implementation

4.1. Singal front-end T/H circuit

The T/H circuit includes a revised bootstrapped switch[2], sampling capacitor and a source-follower structured buffer. The bootstrapped switch shown in Fig. 5 introduces several MOSFETs to overcome the effect of clock through and to reduce the signal dependant charge injection. The size of M13 and M15 are chosen to be equal so that the two MOSFETs have identical overlapped capacitors. Without the compensation MOSFETs, the voltage error caused by clock through is

$$\Delta V = (V_{\mathrm{DD}} + V_{\mathrm{in}}) \frac{W C_{\mathrm{OV}}}{W C_{\mathrm{OV}} + C_{\mathrm{S}}}, \qquad (1)$$

which depends on input signal. In the revised circuit, M13 and M15 cancel the second part of ΔV, leaving the remaining part unchangeable. M14 is a dummy MOSFET used for charge injection cancellation. The size of M14 should be selected according to simulation result.

Source follower structured buffer usually has a problem of nonlinearity. Connecting substrate to source in the PMOS design may overcome the body effect but still the introduced changeable substrate capacitor becomes a load of the output and will affect the linearity in another aspect. An improved source-follower[3] is illustrated in Fig. 6. A duplicated branch is also connected to the input but the sizes of M2 and M3 are chosen to be rather smaller comparing to M4 and M5 in the trunk. By connecting the substrate of the M5 to that of M3 can the output be clean and immune from the nonlinearity problem.

4.2. Folding circuit

Folding circuit is shown in Fig. 7. Two-stage cascaded structure[4] is used to guarantee the high voltage gain which is beneficial to reducing the mismatch of comparator input pairs. Moreover, each stage of the cascaded folder contains three folding units achieving cascaded folding factor of 9, generating less capacitive load at the outputs. Therefore, the bandwidth and dynamic performance of the folder can be largely improved. Stage1 needs 12 folding blocks to cover total 36

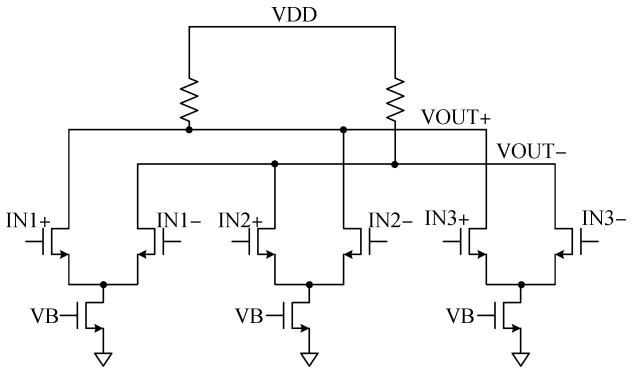

Fig. 7. Folding circuit for a single stage.

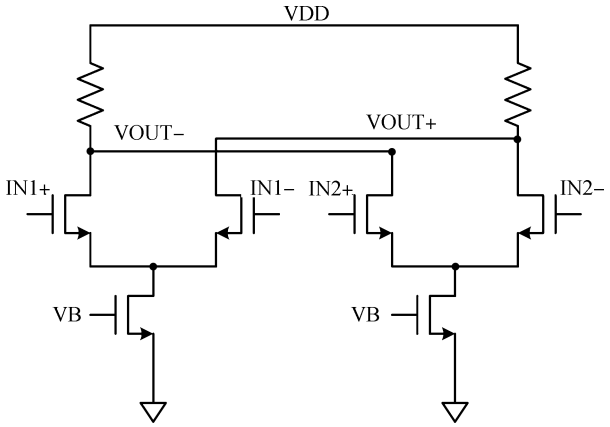

Fig. 8. Active interpolating circuit for a single stage.

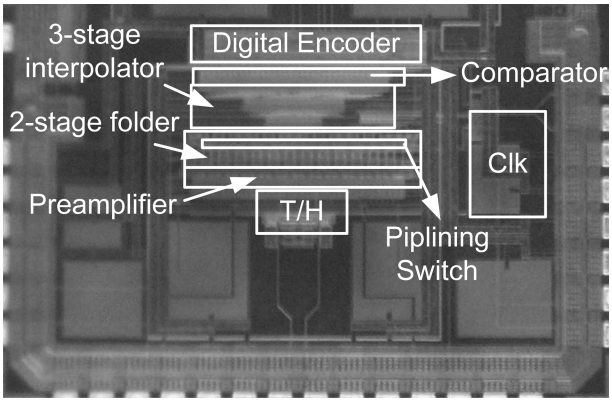

Fig. 9. Prototype of the proposed ADC.

Table 1. Measured performance of the ADC.

Parameter	Value
Technology	0.13 μm CMOS
Resolution/ENOB	8 bit/6.9 bit
Sampling rate	300 MS/s (250MS/s for measurement)
SNDR @ f_{in} = 1 MHz	43.4 dB
@ f_{in} = 125 MHz	42.1 dB
SFDR @ f_{in} = 1 MHz	53.5 dB
@ f_{in} = 125 MHz	49.5 dB
DNL	+0.75/−0.68 LSB
INL	+1.4/−2.4 LSB
Power supply	1.4 V
Power consumption	34 mW @ 1.4 V
Active area	0.6 mm^2

zero-crossings produced by preamplifiers while stage2 contains only four as Figure 1 shows.

Resistor averaging network is inserted between the two folding stages. Equivalent resistor now can be derived as

$$R_{\rm eq} = \frac{R_1 + \sqrt{R_1(R_1 + 4R_0)}}{2}, \qquad (2)$$

in which R_1 stands for the averaging resistor and R_0 is the load of the amplifier[5]. The equivalent resistor is lowered when R_0/R_1 reaches a certain value. Therefore, the gain of the amplifier stage is lowered. Meanwhile, the ratio of R_0 and R_1 should be chosen as large as possible to achieve a better ECF (error correction factor) according to the concept of spatial filtering[6]. To balance the gain reduction and the averaging effect, a ratio of R_0/R_1 = 3 is selected according to simulation results.

4.3. Interpolating circuit

Active interpolation as shown in Fig. 8 is adopted in the interpolating block instead of choosing the resistor interpolation as normally used. In one hand, resistor interpolation requires a source-follower to drive the resistors but the shifted level is hard to match the common mode voltage of the former or later circuits when the supply is as low as 1.2 V. In the other hand, active interpolation realizes one additional zero-crossing between every two, so a 3-stage cascaded structure[7] can easily achieve 8×. Furthermore, active interpolation has an advantage of having certain gain that helps to amplify the signal before it is compared.

5. Experimental results

The ADC is fabricated in a 0.13-μm mixed-signal 1P8M CMOS technology. A die microphotography is shown in Fig. 9. The ADC occupies a core area of 1000 × 630 μm^2 = 0.63 mm^2.

The analog input signal produced by a vector signal generator passes through a bandpass filter before it is fed into a splitter, by which the single-end signal can be divided into two differential signals. The clock signal is generated in a similar way. Low-voltage differential signaling (LVDS) PADs are taken into use when the chip is designed for a better performance at high frequencies. Hence, an on-board level converter MAX9173 is adopted to convert the differential outputs into single-end signals to allow the logic analyzer to collect them. MAX9173 can process a clock signal no faster than 250 MHz. Therefore, highest sampling frequency of 250 MHz is set in the testing period. Finally, the data are saved and sent to PC to start a MATLAB analysis.

The peak differential nonlinearity (DNL) and integral nonlinearity (INL) of +0.75/–0.68 LSB and +1.4/–2.4 LSB are shown in Fig. 10. Figure 11 shows that the SNDR and SFDR are 43.4 dB and 53.3 dB at 1-MHz input-signal frequency at a supply of 1.4 V. When input frequency rises to Nyquist-frequency, the SNDR and SFDR remain 42.1 dB and 49.5 dB. FFT result is illustrated in Fig. 12. As a Nyquist ADC,

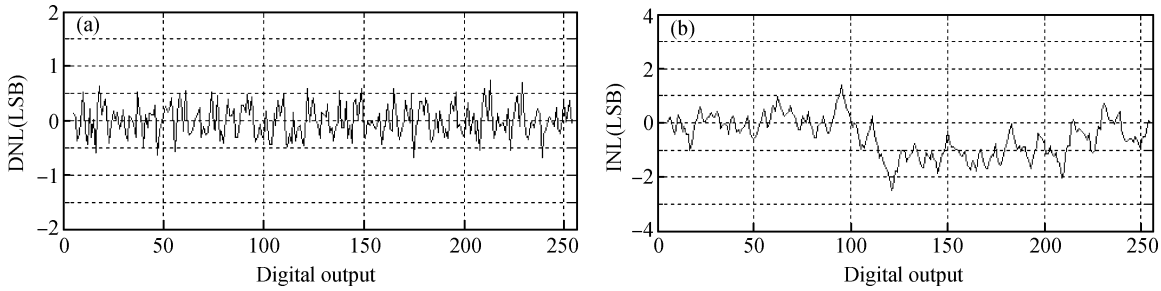

Fig. 10. (a) DNL. (b) INL.

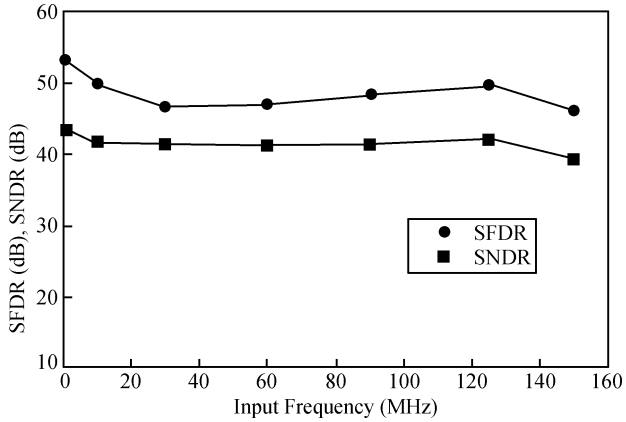

Fig. 11. Measured SFDR and SNDR versus input frequency (F_s = 250 MHz, 1.4-V supply).

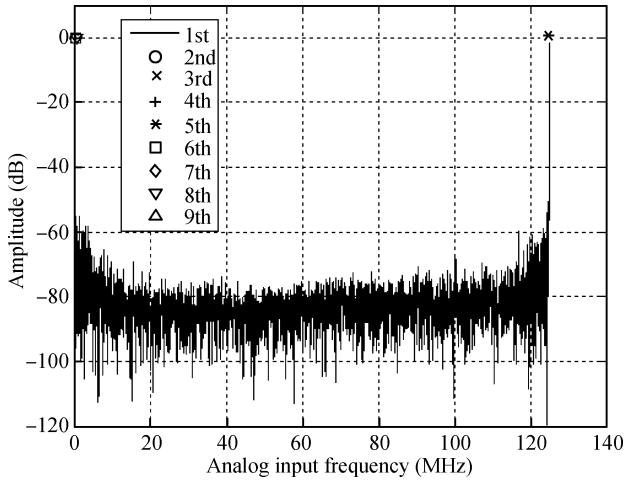

Fig. 12. FFT results of Nyquist-frequency input at f_s = 250 MHz, f_{in} = 125 MHz.

the SNDR degrades only 1.3-dB ranging from low-frequency to Nyquist-frequency which shows a wide-range of bandwidth. That is to say, the dynamic performance of the ADC is not limited to the bandwidth. However, performances at low-frequencies do not show much progress than those at high-frequencies. INL may be a possible reason since DC performance is more related to INL instead of bandwidth. If INL is improved in the future versions, the flat line in Fig. 11 may have an overall rise.

INL appears to be not so good, as can be seen from the measurement results. It is probably caused by the limited effect of the averaging network. As mentioned above, the averaging network is removed from the traditional position so that more power can be saved. From another aspect, the averaging network after the pr-amplifier array will badly affect the gain which in return will cause non-linearity. Therefore, this is a compromise between power-saving and high-linearity. In this design, linearity is sacrificed to some extent in exchange for the low power dissipation.

The measured performance is summarized in Table 1. Power of the ADC is only 34 mW at 1.4-V supply. Figure of merit (FoM) is defined as Power/($2^{ENOB}\times F_S$) for Nyquist converters and Power/($2^{ENOB}\times 2 \times$ ERBW) for non-Nyquist converters[8]. ERBW stands for Effective Resolution Bandwidth. In comparison with the reported results listed in Table 2, the proposed ADC achieves relatively low FoM among the state-of-the-art high-speed ADCs with similar resolution requirements.

6. Conclusion

This paper presents a 1.4-V 8-bit 300-MS/s folding and interpolating structured ADC. A cascaded stages structure is used both in folding and interpolating blocks that is beneficial to low-voltage design and can accumulate high cascaded gain to overcome input mismatch. Low-power optimization is conducted by inserting pipelining sampling switches to cut down the extra power needed for complete settling. The averaging resistor array is moved to the middle of two folding stages for a power-saving consideration. The ADC is fabricated in 0.13-μm process with an active area of 0.6 mm^2. It consumes only 34 mW and is well-designed for embedded use.

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Table 2. Performance comparison.

Publication	Process (μm)	Resolution (Bits)	Sample (MHz)	Power (mW)	Area (mm^2)	FoM (pJ/convstep)
JSSC, 2003[9]	0.35	7	300	200	1.2	8.2
JSSC, 2004[10]	0.13	8	125	21	0.09	0.54
JSSC, 2005[11]	0.18	8	150	71	1.8	2.65
AICSP, 2006[12]	0.18	8	200	177	0.25	7.3
VLSI, 2006[13]	0.09	7	800	120	0.32	2.2
CICC, 2007[14]	0.18	8	500	348	1.22	5.4
TCAS, 2008[15]	0.18	8	600	207	0.5	6.25
This work	0.13	8	300	34	0.6	1.14

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