An 8-bit 100-MS/s pipelined ADC without dedicated sample-and-hold amplifier*

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Abstract: An 8-b 100-MS/s pipelined analog-to-digital converter (ADC) is presented. Without the dedicated sample-and-hold amplifier (SHA), it achieves figure-of-merit and area 21% and 12% less than the conventional ADC with the dedicated SHA, respectively. The closed-loop bandwidth of op amps in multiplying DAC is modeled, providing guidelines for power optimization. The theory is well supported by transistor level simulations. A 0.18-μm 1P6M CMOS process was used to integrate the ADCs, and the measured results show that the effective number of bits is 7.43 bit and 6.94 bit for 1-MHz and 80-MHz input signal, respectively, at 100 MS/s. The power dissipation is 23.4 mW including voltage/current reference at 1.8-V supply, and FoM is 0.85 pJ/step. The ADC core area is 0.53 mm^2. INL is -0.99 to 0.76 LSB, and DNL is -0.49 to 0.56 LSB.

Key words: analog-to-digital converter; pipelined; removing dedicated SHA; close-bandwidth; figure-of-merit
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1. Introduction

The development of digital signal processing techniques in different domains, such as wireless communication, audio and video, has driven the developments of ADCs and DACs to lower power dissipation and higher performance. In the applications for portable devices, the power dissipation is the main concern. The power dissipation of digital circuits is reduced directly by device scaling down while that of analog circuits mainly depends on the development of new topology and structure techniques and system level optimization[1].

An 8-b 100-MS/s pipelined ADC is presented in this paper. The pipelined ADC is preferred because it guarantees high linearity by employing high DC gain amplifiers in a closed-loop configuration with moderate power dissipation. To further reduce the power dissipation and area, the dedicated sample-and-hold amplifier (SHA) is often removed[2, 3]. In our work, two ADCs are presented. The 1st ADC (ADC1) has the dedicated SHA removed and the sample-and-hold is embedded in the 1st stage[4]. The 2nd ADC (ADC2) is a conventional ADC which is implemented in the same die for comparison. The closed-loop bandwidth (BW_{close}) of op amps in multiplying DAC (MDAC) is modeled considering short-channel effect providing guidelines for power optimization. Transistor level simulations are performed to verify the theory. In Section 2, ADC architectures are presented. In Section 3, circuits design is described including the operating principle and BW_{close} modeling. The comparison results are given in detail in Section 4. This paper will be concluded in Section 5.

2. ADC architectures

Both ADC1 and ADC2 architectures are 1.5 bit/stage as shown in Figs. 1 (a) and 1(b), respectively. The analog signal is quantized by six pipelined stages followed by flash-2bit-ADC and digital outputs of each stage are corrected by digital error correction (DEC). The op amps are shared between two consecutive stages and the capacitances used in the following stages are scaled down to reduce the power dissipation. Clock generator and current/voltage reference blocks are also included in the design. The only difference between two ADCs lies in SHA and the 1st stage. In ADC1, the SHA is removed and sample-and-hold function is embedded in the 1st stage which will be addressed in detail in the next section.

3. Circuit design

3.1. 1st stage with embedded sample-and-hold

SHA is widely used in pipelined ADCs in order to reduce the aperture error caused by sample timing mismatch between the MDAC and the sub-ADC. But it is not a necessary block because it makes no contribution to the final digital output and adds noise and distortion to the analog input signal. Furthermore, it occupies large die area and consumes large power dissipation.

Therefore, SHA can be removed if the aperture error can be minimized within the tolerance which can be corrected by DEC. Various methods to eliminate a dedicated SHA have been published[2, 3]. In Ref. [2], two sample paths need to match by carefully setting their RC time constants equal in the layout design. However, the matching strongly depends on design, layout and process variations, and therefore, it may not be suitable to high speed applications. In Ref. [3], an additional sampling capacitor is required. In this work[4], sample-and-hold is embedded in the 1st stage, while no carefully matching is needed, as shown in Fig. 2(a). This architecture is used in ADC1 and the operation is described as below: there are three operating

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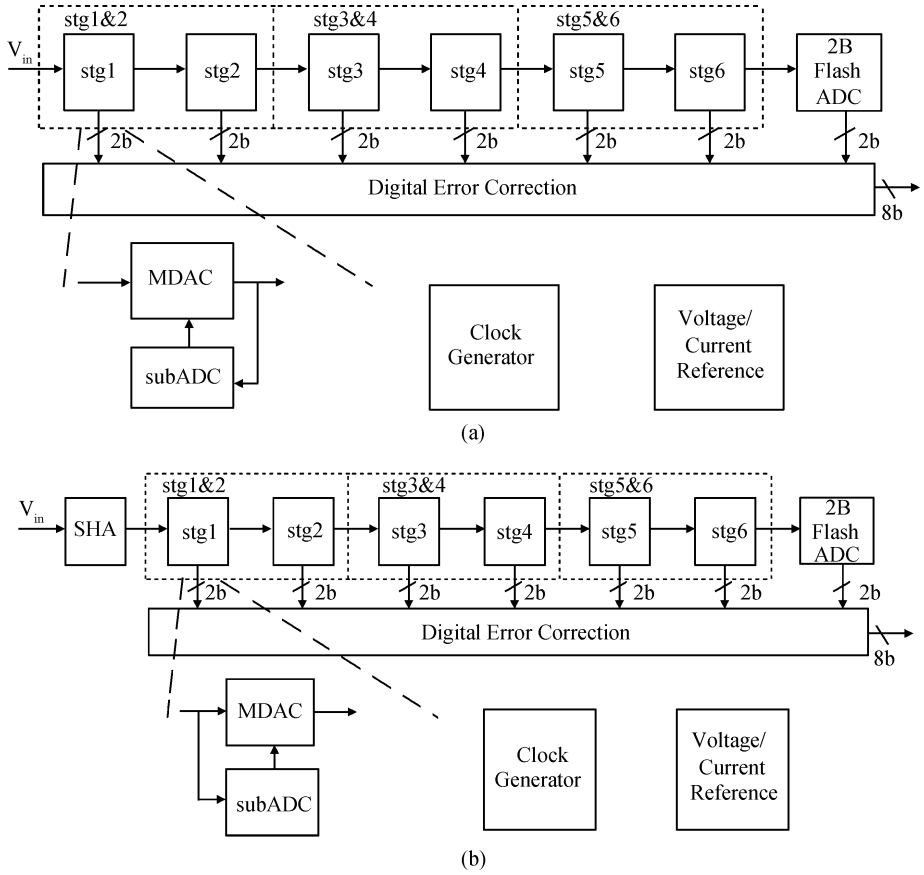

Fig. 1. ADCs architecture. (a) Without dedicated SHA. (b) Conventional.

phases, i.e., sampling, comparing and settling, which correspond to t_1, t_2, t_3, respectively, in Fig. 2(b). During the sampling phase as shown in Fig. 2(c), the input signal V_{in} is sampled by C_S and C_F at the end of CK1. During the comparing phase, as shown in Fig. 2(d), C_F becomes feedback capacitor in phase CK2A. The high gain of op amp makes the node X a virtual ground while the charge in C_F will remain constant. Then, the MDAC functions as a unit-gain flip-around sample/hold amplifier. So, the voltage of node V_{out} will be equal to V_{in} after t_2. The comparator begins to work and the result is latched at rising edge of CK2D as shown in Fig. 2(d). Then, the 1st stage goes into the settling phase at shown in Fig. 2(e). According to the output D_{n-1} of sub-ADC, the bottom plate of C_S is connected to one of the voltage references V_{refp}, V_{cmo} and V_{refn}. And t_2 is decided by how much error the DEC can correct.

As the mention above, the only difference between this 1st stage and conventional 1st stage is t_2 delay of comparing phase. So more power dissipation of op amp in 1st stage is needed but much less than the power dissipation which is saved by removing dedicated SHA. Now let us calculate the increasing power dissipation of the 1st stage. From Ref. [4], we can get the ratio of maximum delay t_2 to the minimum settling time t_3 which is shown in Eq. (1). The effective settling time of the 1st stage to conventional settling time is $1/(1+R_t)$. So the required unity gain bandwidth (GBW) is $1 + R_t$ times of conventional counterpart and the power dissipation is $R_p = (1 + R_t)^2$ times of its counterpart. Given the parameters used in this work, such as $B_1 = 2$, N = 8, $R_t = 0.1875$, $R_p = 1.41$. And the maximum increasing of op amp power dissipation in the 1st stage is 41% which is approximately 12% of the ADC2 supposing that op amp occupies most of the pipelined stage power dissipations. This is much smaller than SHA consumption which is about 40% in ADC2 which will be proved by measurement in Section 4.

$$R_t = \frac{t_{2,\max}}{t_{3,\min}} = \frac{B_1 + 1}{(N - B_1 + 2)2^{B_1 - 1}}. \quad (1)$$

In order to reduce the power in comparing phase, we can open switch S_0. Therefore the loading capacitance is reduced to 2/5 of Ref. [4]. So the additional power is reduced from 12% to 5%. Thanks to the loose settling requirement of comparing phase and relative high non-dominant pole of telescopic OTA, the lower phase margin of OTA caused by small loading capacitance will not influence the ADC. And the proposal is verified by simulations.

3.2. Modeling of close-loop bandwidth of MDAC for power optimization

In pipelined ADC, the sampling rate is mainly determined by BW_{close} of op amps in MDACs. For the ideal op amps with constant feedback factor (f), GBW, along with the BW_{close}, increases with transconductor (g_m). However, for non-ideal op amp, considering the non-ideal factors such as parasitic capacitance which leads to a non-constant feedback factor, BW_{close} does not increase monotonically with g_m[5] and will reach its maximum which corresponds to the maximum sampling rate and the modeling is based on Shockley's MOSFET model[6].

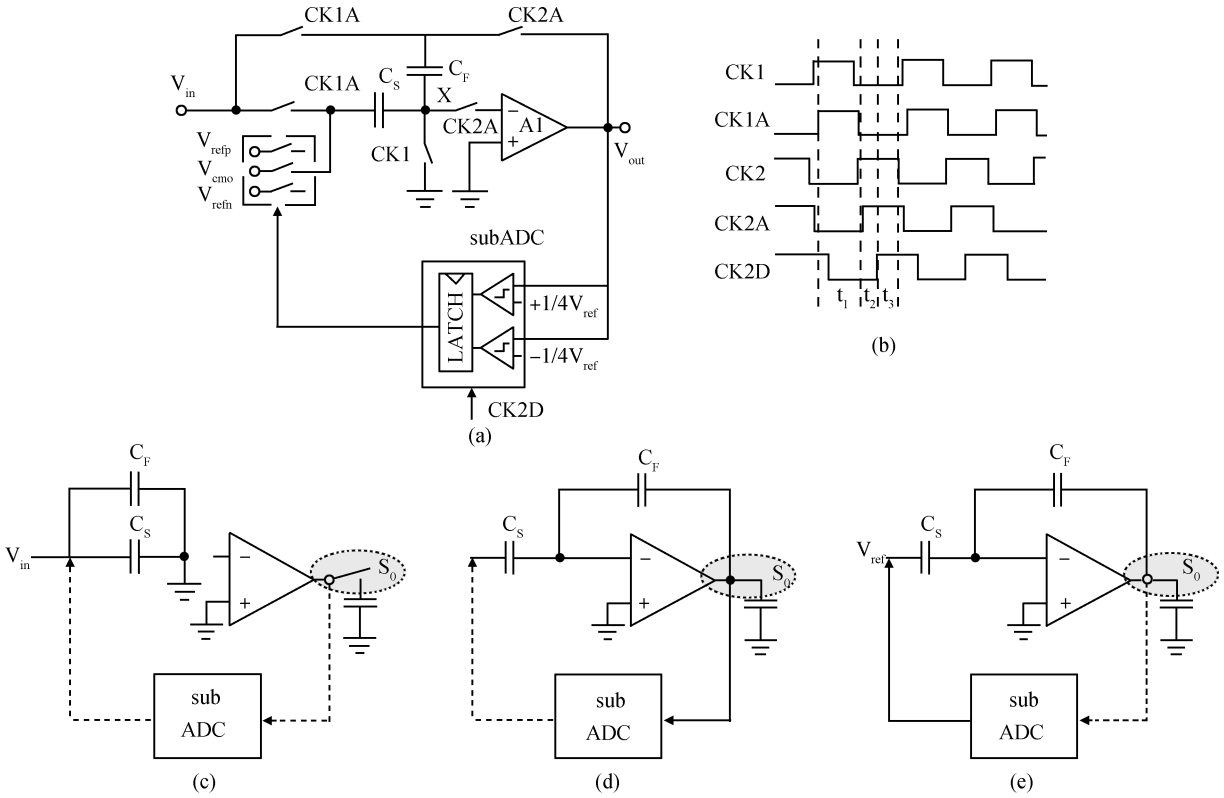

Fig. 2. Working principal of the 1st stage in ADC1. (a) The 1st stage circuit. (b) Its timing. (c) Sampling phase. (d) Comparing phase. (e) Settling phase.

However, the Shockley model can not reproduce the voltage-current characteristics of the short-channel MOSFET's, such as mobility degradation with vertical field, channel-length modulation. In the following analysis, a new model is proposed by considering short-channel effects and verified by transistor level simulations. Figure 3(a) is the MDAC circuit in the settling phase, and Figure 3(b) the equivalent small signal model of the circuit using an NMOS transistor instead of the amplifier. Supposing that the over-drive voltage ($V_{\rm dsat}$) and the length (L) of the input transistors are both constant. Therefore, the current density ($\rho = I/W$, where I is current and W is the width of input transistors) is also constant and the $g_{\rm m}$ is proportional to W, so as to I. The relationship between $V_{\rm dsat}$ and I is described as:

$$I = \frac{1}{2}\frac{\mu_{\rm n}C_{\rm ox}}{1+\theta V_{\rm dsat}}\frac{W}{L}V_{\rm dsat}^2(1+\lambda V_{\rm DS}). \tag{2}$$

From Eq. (2),

$$V_{\rm sat} = \frac{2\theta t + \sqrt{(2\theta t)^2 + 8t}}{2} = \theta t + \sqrt{\theta^2 t^2 + 2t}, \tag{3}$$

where

$$t = \frac{\rho L}{\mu_{\rm n}C_{\rm ox}(1+\lambda V_{\rm DS})}. \tag{4}$$

In Eq. (2), $V_{\rm dsat}$ is considered as a fixed value for the given current density, and θ is also fitting parameter. From Eq. (2), we get $g_{\rm m}$ as

$$g_{\rm m} = \frac{\mu_{\rm n}C_{\rm ox}(1+\lambda V_{\rm DS})}{2L}\frac{\theta V_{\rm dsat}^2 + 2V_{\rm dsat}}{(1+\theta V_{\rm dsat})^2}W. \tag{5}$$

The $\rm BW_{close}$ is

$$\rm BW_{close} = \frac{1}{\tau} = \frac{g_{\rm m}}{C_{\rm load,total}}f, \tag{6}$$

where

$$f = \frac{C_{\rm F}}{C_{\rm F}+C_{\rm S}+C_{\rm GS}}, \tag{7}$$

$$C_{\rm load,\,total} = C_{\rm L} + C_{\rm OP} + \frac{C_{\rm F}(C_{\rm S}+C_{\rm GS})}{C_{\rm F}+C_{\rm S}+C_{\rm GS}}, \tag{8}$$

in which, f is feedback factor of the settling phase MDAC, $C_{\rm load,\,total}$ is the capacitance looking into the output node of op amp, $C_{\rm GS}$ is the input parasitic capacitance, approximately equals to $\frac{2}{3}WLC_{\rm ox}$, and $C_{\rm OP}$ is the parasitic capacitance of the output node with the value of $\alpha WLC_{\rm ox}$. Therefore, both $C_{\rm GS}$ and $C_{\rm OP}$ are proportional to W, which is the same as the $g_{\rm m}$. In addition, $C_{\rm F}$ is the feedback capacitor, and $C_{\rm S}$ is the sample capacitor which is equal to $(2^{B-1}-1)C_{\rm F}$, where B is the resolution of this stage. $C_{\rm L}$ is the sample capacitor of the next stage.

Take Eqs. (5), (7), (8) into Eq. (6),

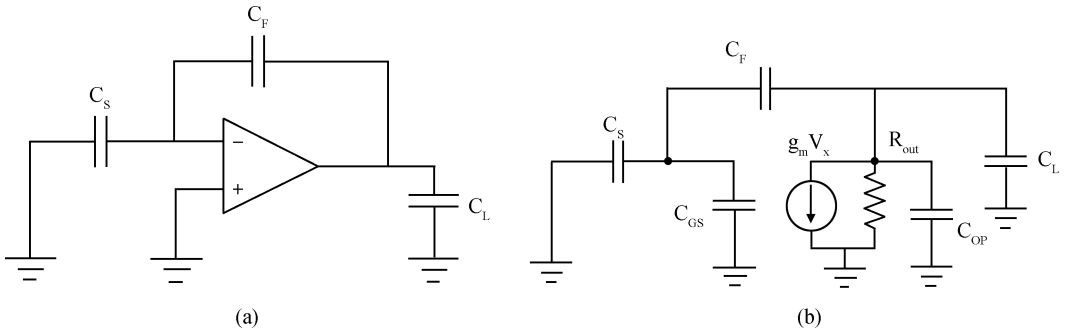

Fig. 3. (a) Settling phase of the MDAC circuit. (b) Equivalent small signal model of (a).

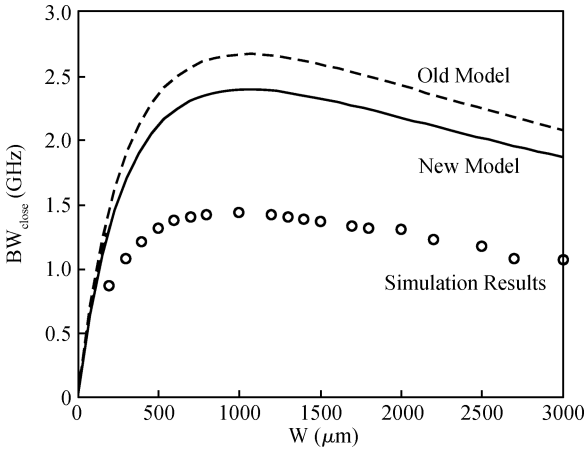

Fig. 4. BW_{close} versus the width of input transistors for the given current density. Suppose $\alpha = 1$, $B = 1$, $C_F = 0.7$ pF, $C_L = 1$ pF, $L = 0.18$ μm, $\rho = 10$ μA/μm, $\mu_n = 340$ cm^2/(V·s), $C_{ox} = 8.91$ fF/μm^2.

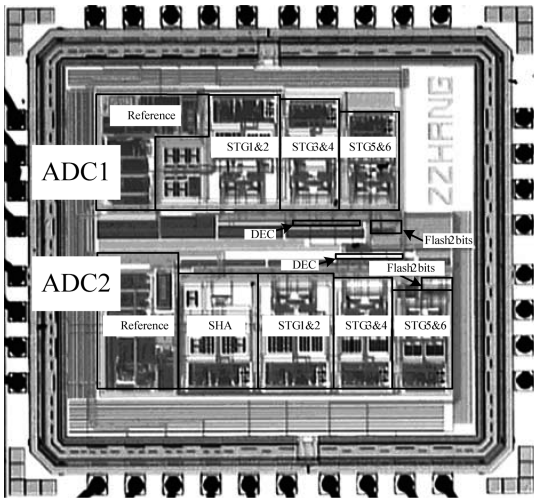

Fig. 5. Photomicrograph of the overall chip.

$$BW_{close} = \frac{\dfrac{\mu_n C_{ox}(1+\lambda V_{DS})}{2L}\dfrac{\theta V_{dsat}^2 + 2V_{dsat}}{(1+\theta V_{dsat})^2}W}{C_L + \alpha WLC_{ox} + \dfrac{C_F\left[(2^{B-1}-1)C_F + \dfrac{2}{3}WLC_{ox}\right]}{C_F + (2^{B-1}-1)C_F + \dfrac{2}{3}WLC_{ox}}} \times \frac{C_F}{C_F + (2^{B-1}-1)C_F + \dfrac{2}{3}WLC_{ox}}. \quad (9)$$

V_{dsat} can be obtained from Eqs. (2), (3). Other parameters are from 0.18-μm CMOS process, $\alpha = 1$, $B = 2$, $C_F = 0.7$ pF, $C_L = 1$ pF, $\mu_n = 340$ cm^2/(V·s), $C_{ox} = 8.91$ fF/μm^2, $\theta = 1$ V^{-1}.

The relationship between BW_{close} and width of input transistors is illustrated in Fig. 4 in order to compare the old model[5], the new model in Eq. (9), and transistor level simulations. The new model is closer to transistor level simulations than the old model. The discrepancy between the new model and transistor level simulations is because the BSIM3 model is much more complex. But the new model gives an accurate analytical expression for the maximum BW_{close}.

4. Measurements and comparison

Figure 5 presents the photomicrograph of the overall chip implemented in a mixed signal 1P6M 0.18-μm CMOS technology. The upper part is ADC1 and occupies an area of 0.53 mm^2, which consists of current/voltage reference, stages1&2, stages3&4, stages5&6, flash2bit ADC, DEC except dedicated SHA. The lower part is ADC2 occupying 0.60 mm^2, which is a conventional ADC with dedicated SHA. The input range of the ADC1 is 1 V_{pp} (peak-to-peak) differentially at a 1.8 V power supply. The dynamic performance of ADC1 is presented in Fig. 6, where a full-scale input sinewave at $f_{in} = 1$ MHz is sampled with frequency $f_s = 100$ MS/s. Spurious-free-dynamic-range (SFDR) is 56.3 dB, signal-to-noise (SNR) is 47.6 dB, and signal-to-noise-and-distortion (SNDR) is 46.5 dB, which results in the effective number of bits (ENOB) of 7.43 bits. The 2nd to 6th harmonics are also shown in that Figure. The SNDR at $f_{in} = 1$ MHz is maintained within 3 dB up to 80 MHz, which is also listed in Table 1. Figure 7 shows dynamic performance in different input frequencies at 100 MS/s. The power dissipation is 23.4 mW including the bandgap-based current/voltage reference. The INL is -0.99 to 0.76 LSB, and DNL is -0.49 to 0.56 LSB in Fig. 8. The performance of ADC1 is also summarized in Table 1. Figure 9 illustrates the ENOB of two ADCs at 100 MS/s versus input frequency up to 100 MHz. The ENOB is more than 7.4 bit at low frequency and about 6.8 bit at 100 MHz. Figure-of-merit

Table 1. ADCs Performance Summary and comparisons.

Input frequency	ADC1				ADC2			
(MHz)	ENOB (bit)	SNDR (dB)	SNR (dB)	SFDR (dB)	ENOB (bit)	SNDR (dB)	SNR (dB)	SFDR (dB)
1	7.43	46.5	47.6	56.3	7.48	46.8	47.7	56.4
80	6.94	43.5	46.2	50.5	6.94	43.5	43.8	57.1

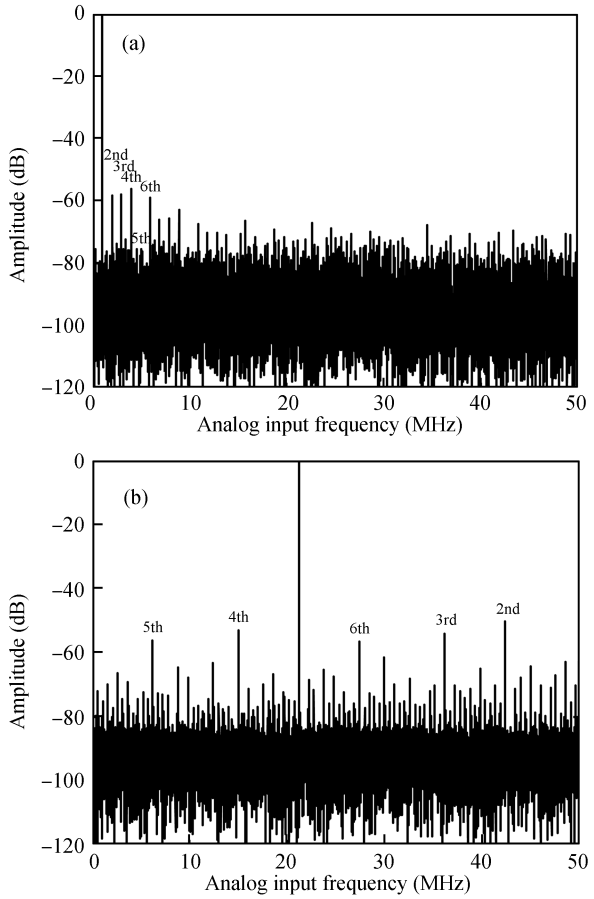

Fig. 6. A fast Fourier transform (FFT) plot of the output for a sampling rate $f_s = 100$ MS/s. (a) Input $f_{in} = 1$ MHz. (b) Input $f_{in} = 80$ MHz.

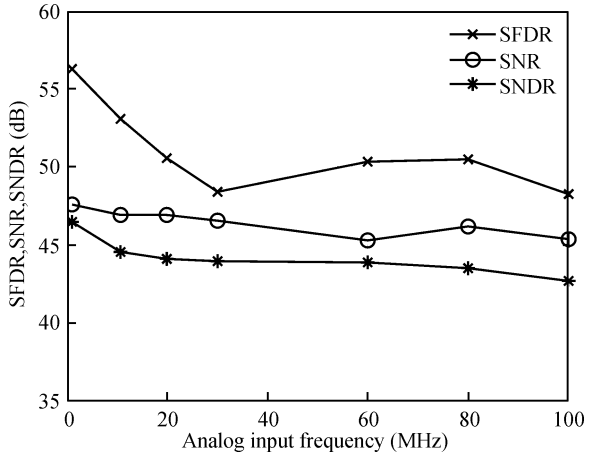

Fig. 7. Dynamic performance at 100 MS/s.

(FoM) is widely used to compare the performance of ADCs[7],

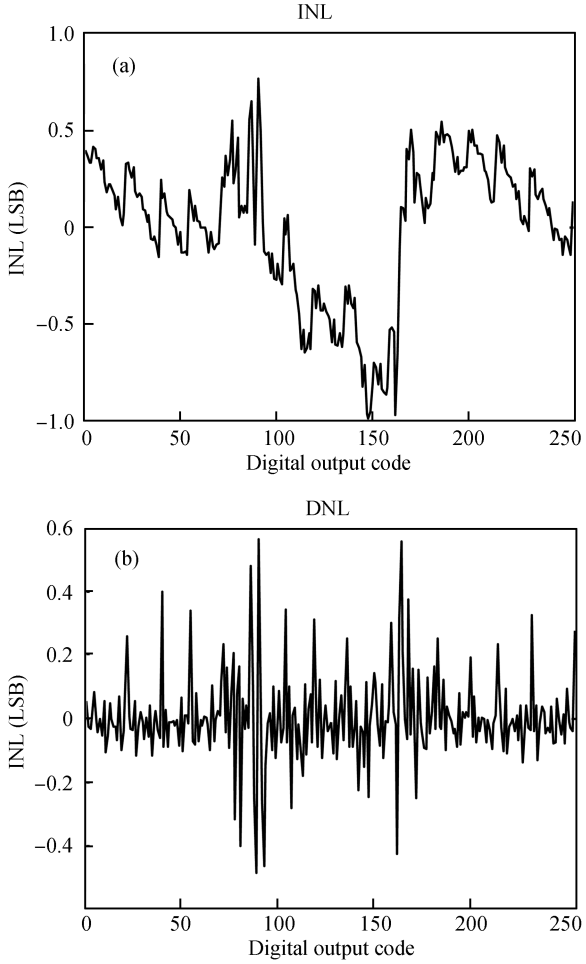

Fig. 8. (a) INL. (b) DNL.

$$\mathrm{FoM} = \frac{P}{2^{\mathrm{ENOB}} \times 2\mathrm{ERBW}}, \tag{10}$$

where P is total power dissipation, ENOB is the effective number of bits at low input signal, and ERBW is the effective resolution bandwidth when the ADC falls 0.5 bit. Here, the ERBW of ADC1 and ADC2 are both 80 MHz. Table 2 also compares the results of two ADCs in terms of power dissipation, area, dynamic performance, statistic performance and FoM, where the power dissipation, area and FoM of ADC1 have 24%, 12% and 21% improvement, respectively, comparing to ADC2. From Table 3, which shows a list of 8bit pipelined ADC with similar sampling rate[8−11] in recent years, FoM of ADC1 is only 0.85 pJ/step which is the lowest.

5. Conclusion

A pipelined ADC without dedicated SHA has been presented in the paper. The architecture used here needs no careful layout matching compared to other architectures. Large die

Table 2. Comparison between ADC1 and ADC2.

Parameter	ADC1	ADC2	Comparisons (ADC1 to ADC2)
INL (LSB)	–0.99 to 0.76	–0.45 to 0.46	
DNL(LSB)	–0.49 to 0.56	–0.46 to 0.46	
Power @ 1.8 V (mW)	23.4	30.6	24%
FoM (pJ/step)	0.85	1.07	21%
Area (mm^2)	0.53	0.60	12%

Table 3. Comparison with previous work.

	Sampling rate (MS/s)	Power (mW)	BW (MHz)	ENOB (bit)	FoM (pJ/step)
JSSC, 2005[8]	150	71	80	7.24	2.94
VLSI, 2006[9]	100	30	20	6.60	7.73
ESSCRIC, 2008[10]	120	9.4	40	7.04	0.89
Journal of Semiconductors, 2009[11]	125	138	30	7.07	17.2
This work ADC2	100	30.6	80	7.48	1.07
ADC1	100	23.4	80	7.43	0.85

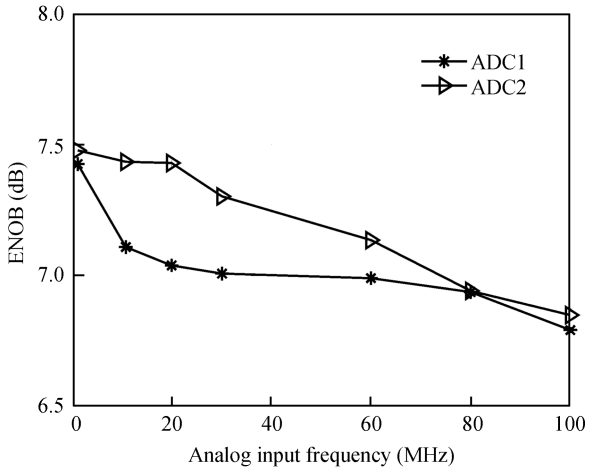

Fig. 9. Comparison of ENOB at 100 MS/s.

area and power dissipation are saved only at the cost of increasing the power dissipation in the 1st stage, which is much smaller than the dedicated SHA. The modeling of BW_{close} in MDAC is proposed with short-channel effects and verified by transistor level simulations. The comparison results show the new model considering short-channel effects is more accurate than old model considering long-channel model to reality. ADC2 with dedicated SHA is also fabricated in the die and the measured comparison shows the less power dissipation and area with similar good performance. The work is also compared with recent published work and FoM indicates the good performance with low power dissipations of the design.

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