A 2-GS/s 6-bit self-calibrated flash ADC

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Abstract: A single channel 2-GS/s 6-bit ADC with cascade resistive averaging and self foreground calibration is demonstrated in 0.18-μm CMOS. The calibration method based on DAC trimming improves the linearity and dynamic performance further. The peak DNL and INL are measured as 0.34 and 0.22 LSB, respectively. The SNDR and SFDR have achieved 36.5 and 45.9 dB, respectively, with 1.22 MHz input signal and 2 GS/s. The proposed ADC, including on-chip track-and-hold amplifiers and clock buffers, consumes 570 mW from a single 1.8 V supply while operating at 2 GS/s.

Key words: analog-to-digital conversion; offset averaging; flash; interpolation; calibration
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1. Introduction

The high-speed analog-to-digital converter (ADC) is a key component in modern high performance digital signal processing systems such as software defined radios, disk drive read channels, and digital oscillographs. For 6- bit resolution, a flash architecture is the most general choice for GS/s converters. However, the conventional flash architecture needs $2^N - 1$ preamplifiers and comparators, which lead to a big challenge of ADC linearity, die area and power consumption. So, many mixed architectures and new technologies have been developed to decrease power dissipation and improve performance. Other than the passive component averaging technology, many digital calibration methods have been used to decrease the offset error in preamplifiers and comparators. The foreground calibration method is the better choice for the high-speed ADC because of its property of one-time or on-line calibration and not decreasing conversion speed[1−5].

The paper describes the realization of a single channel 2-GS/s 6-bit flash ADC with new resistive averaging and self-calibration. The chip uses foreground digital-to-analog (DAC) trimming and cascade resistive averaging to achieve better static linearity and dynamic performance.

2. ADC architecture

A detailed block diagram of the proposed ADC is shown in Fig. 1, including the calibration block, wideband track and hold amplifier (THA), 1st preamplifiers, 2nd cascade amplifiers with 2 time interpolation, comparator stage, digital encoding with error correction and output stage. In the calibration block, foreground DAC trimming is used for self-calibration. In the cascade amplifiers, continual resistor averaging is used to decrease the mismatch between amplifier arrays, which also can relieve the strict requirements of comparator offset and obtain lower power consumption.

2.1. Wideband THA and cascade amplifiers with resistor averaging

The wideband THA is extremely important for the GS/s ADC dynamic performance, especially for effective resolution bandwidth (EPBW). An on-chip open-loop pseudo-differential THA is used in the chip[6, 7]. Also, a new termination method which has an excellent offset averaging effect with lower reference voltage consumption is used. Detailed information about the THA and the new resistor termination method is given in Ref. [8].

2.2. Differential differencing preamplifiers

As known, the biggest kickback voltage in the reference locates in the middle of the reference resistor ladder. For the single signal and reference, the kickback voltage in the middle node of reference is expressed as:

$$V_{\rm mid}/V_{\rm in} = \alpha(\alpha+32)/(\alpha^2+32\alpha+128),\ \alpha = \pi f_{\rm in} RC, \quad (1)$$

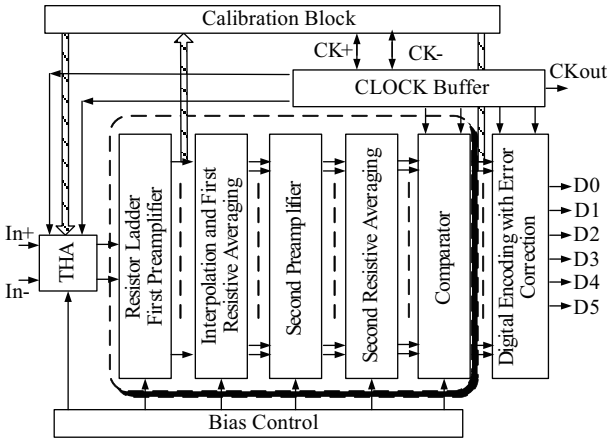

Fig. 1. Block diagram of the proposed ADC.

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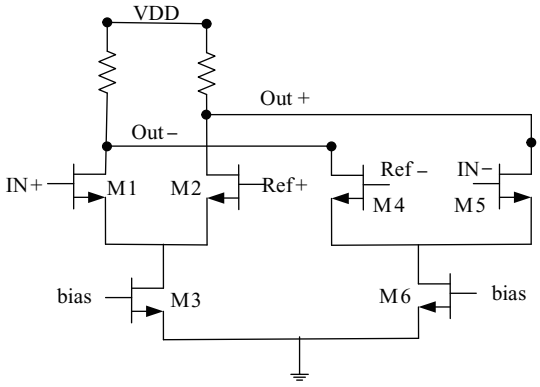

Fig. 2. Differential differencing preamplifier.

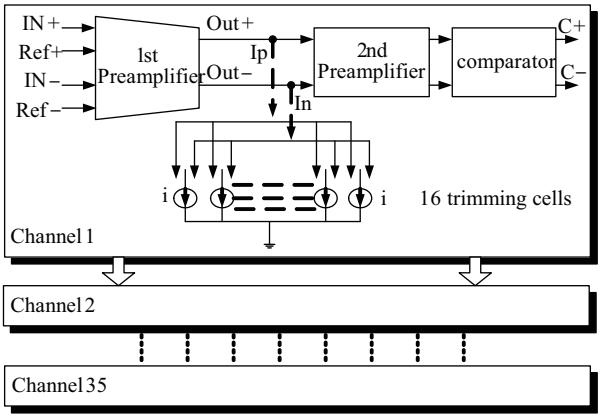

Fig. 3. ADC total calibration process.

where V_{mid} is the voltage of the middle node, R is the total resistance of the reference ladder, and C is the total input capacitance of the first preamplifier stage. For the differential signal and reference, the kickback voltage in the same node is expressed as:

$$\begin{aligned} V_{\text{mid}} &= V_{\text{in+}}\alpha(\alpha+32)/(\alpha^2+32\alpha+128) \\ &\quad - V_{\text{in–}}\alpha(\alpha+32)/(\alpha^2+32\alpha+128) \\ &= 0, \quad \alpha = \pi f_{\text{in}} RC. \end{aligned} \tag{2}$$

So, the kickback voltage in the middle node is decreased to zero. But the above value is based on the ideal difference property. In fact, the non-ideal property still makes it need a low reference resistor. Comparing to the single signal and reference, the differential signal and reference can still decrease the kickback voltage in the reference resistor ladder. As a result, in the first preamplifier stage, a differential differencing topology is used, as shown in Fig. 2. The gates of M1 and M5 are connected to the pseudo-differential signal from THA. The gates of M2 and M4 are connected to the differential reference voltage from the single resistor ladder, which can also cancel the kickback voltage to the first order because each tap point is coupled to both of the input differential signals through the gate-to-source capacitances of the two preamplifiers.

2.3. Self-calibration based on DAC trimming

Although the averaging method can improve ADC linearity, the offsets due to the device mismatch in the preamplifiers and comparators are still the major reason to limit ADC performance. To overcome the offsets from each analog block, many calibration methods or algorithms have been proposed[4, 6, 9]. Foreground self-calibration is the better choice for the high-speed ADC because the calibration does not work during normal ADC operation. The DAC trimming calibration method is used in the chip because of its efficiency and simplicity. The proposed calibration circuits are inserted between the first and second preamplifiers. The calibration could start at power-on or on-line invoking during normal operation. The total calibration process is shown in Fig. 3.

Each channel in the first preamplifier stage should be calibrated individually. The chip needs 35 steps to fulfill the whole chip calibration because there are 35 parallel channels in the first preamplifier stage. For the each channel, the calibration

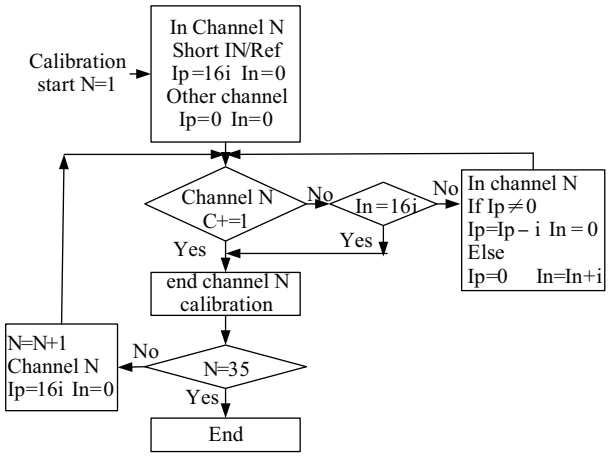

Fig. 4. ADC calibration algorithm.

algorithm and step are the same. The detailed calibration algorithm is shown in Fig. 4.

The major components of the calibration circuit are DAC trimming circuits and calibration control circuits. The trimming current is connected to the differential outputs of the first preamplifier. When calibration starts in channel N, the inputs of the preamplifier in channel N, such as IN+/Ref+ and IN–/Ref–, should be shortened during the whole calibration. At the same time, the entire 16 uniform DAC trimming current cells (I) in channel N should all flow to the I_{p} or flow into the node OUT+ of the preamplifier. Then the calibration control logic judges the condition based on the output of the corresponding comparator. The calibrating current I_{p} will decrease one current cell (I) at each calibrating step by turning off its switch until the output of the comparator changes to logic 1. If I_{p} is decreased to zero and the output of the comparator is still logic 0, the DAC trimming cell current should flow to the I_{n} or flow into the node OUT– of the preamplifier by increasing one current cell (i) at each calibrating step until the output of the comparator changes to logic 1 or I_{n} equals $16i$. Actually, the proposed calibration method reduces not only the offset of the first preamplifiers but also the second preamplifiers and comparators, as shown in the shadow region in Fig. 1. During the calibration, the ADC would not sample the input signal.

The current from a DAC trimming current cell should be

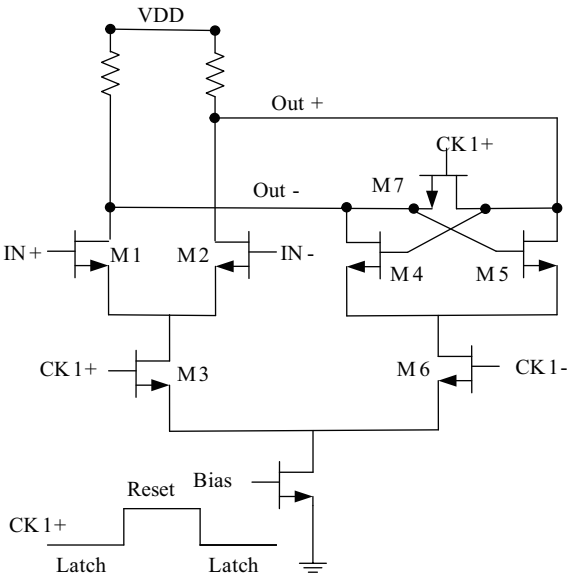

Fig. 5. First stage comparator.

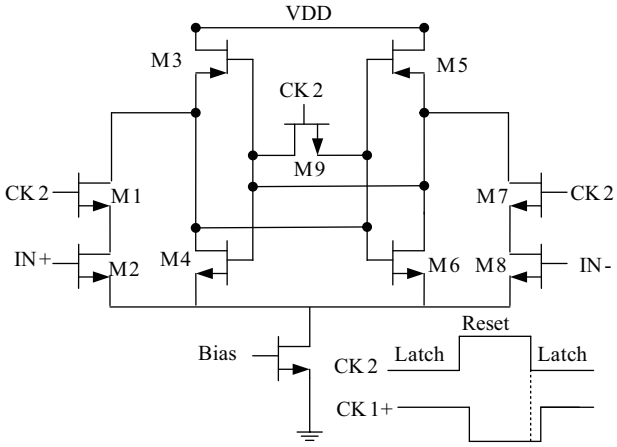

Fig. 6. Second stage comparator.

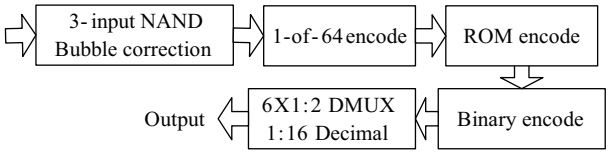

Fig. 7. Digital encoding block.

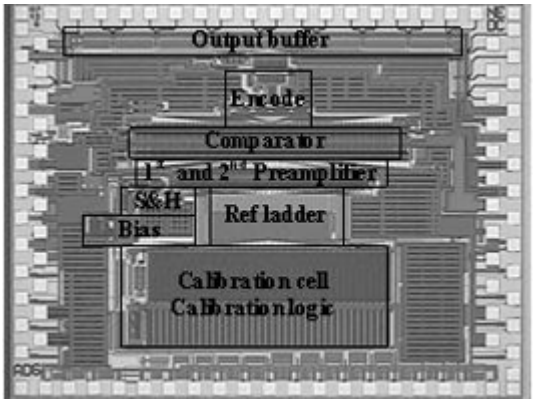

Fig. 8. Chip photograph.

low because it determines the final precision after calibration. Also, the number of DAC trimming current cells should be large enough because it determines the biggest offset which can be calibrated. The clock frequency of calibration is set to 1/8 times of the sample clock to ensure sufficient settling time. For a 1 GHz sample clock, the chip need 13.5 μs to finish the whole chip calibration. At each power-on, the chip could calibrate automatically after the clock input and could invoke online by the control bit during normal chip operation. For the chip the DAC trimming current cell is set to 1.25 μA corresponding to 1.2 mV calibrated voltage. With the control bits changing, the trimming current could increase to calibrate the bigger offset.

2.4. Comparator

The proposed comparators include two stage regenerative comparators and an RS latch. Figure 5 shows the topology of the first regenerative comparator.

A reset switch is added to solve the overdrive recovery which limits the comparator speed. In the track phase, the comparators vary with input differential voltage through M1/M2/M3. At the same time, the reset switch M7 shorts the differential output nodes to quickly eliminate the memory of the previous decision state. In latch phase, the reset switch is open and the comparators are configured into a positive-feedback with M4/M5/M6 so that the comparators output the decision state. Figure 6 shows the second stage comparator directly following the first stage comparator.

A reset switch is also added for the same reason. Two differential CMOS inverters comprising M3–M6 are also configured into a positive-feedback loop. The gain during regenerative latch of the tow stage comparators should be large enough to overcome dynamic offset and instability. The timing between the two stage comparators is shown in Fig. 6, so the comparators could obtain better results. An RS latch follows the comparators to improve the stability and bit error rate further.

2.5. Digital encoding with error correction

The digital encoding block is shown in Fig. 7. A ROM-based encoder after the comparator stage maps the thermometer code to 1-of-n code. 3-input NAND and quasi-Gray encoding are used to overcome bubbles and spikes. Only one-stage XOR gates are needed to convert quasi-Gray to binary code without the pipelined delay of conventional Gray encoding. Flip flops are inserted to guarantee the high-speed timing. 6-channel 1 ： 2 DMUX are used to slow down the output data rate for feasible use. Otherwise, 16-time decimation is optional for testing and debugging. The output buffer could drive the load of 50 Ω with the CML logic level.

3. Experimental results

The ADC is implemented in 0.18 μm CMOS technology. The die size, restricted by many extra pads, is 3.1 × 2.4 mm^2, as shown in Fig. 8. All the results below are obtained after the

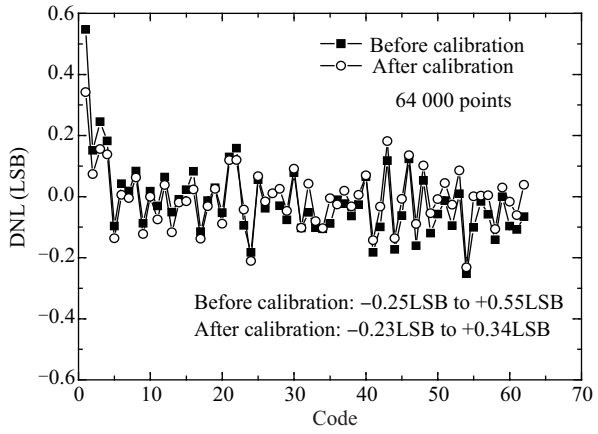

Fig. 9. DNL result.

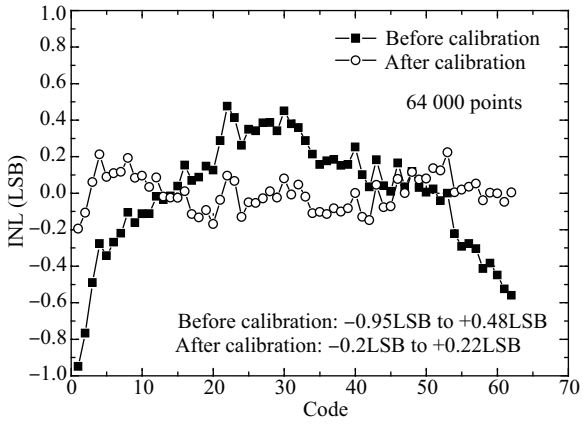

Fig. 10. INL result.

chip is packaged in a 100 pin CQFP.

Many decoupled capacitances are placed on the empty areas of the die. The ADC is mounted in a 100-pin CQFP for all tests. Excluding output buffers and including THA and clock buffer, it consumes about 480 mW from a single 1.8 V at 1 GS/s, and 570 mW at 2 GS/s.

Figures 9 and 10 show the compared static results before and after calibration based on the histogram test method with 1.22 MHz input and 2 GHz clock. Before calibration, the peak DNL and INL are 0.55 LSB and 0.95 LSB. After calibration, the peak DNL and INL are 0.34 LSB and 0.22 LSB. So, the proposed calibration method could improve DNL by 38% and INL by 77%.

Figure 11 shows the FFT (8000 points) result at 1.22 MHz input frequency with 2 GHz clock. The SNDR and SFDR reach 36.5 dB and 45.9 dB, respectively, corresponding to 5.78 bit ENOB. But the test result of the effective resolution bandwidth (ERBW) is only less than 200 MHz with 2 GHz clock, which is also the next optimization target.

Figure 12 shows that the two tone intermodulation distortion (IMD) could reach –45.3 dBFS (8000 FFT points), with 90 MHz/100 MHz input and 900 MHz sample clock.

Figures 13 and 14 show the compared results of SFDR and ENOB with 50 MHz input and different sample clocks from 100 to 900 MHz (8000 FFT points). After calibration, the results show SFDR all above 42 dB and ENOB all above 5.5 bit.

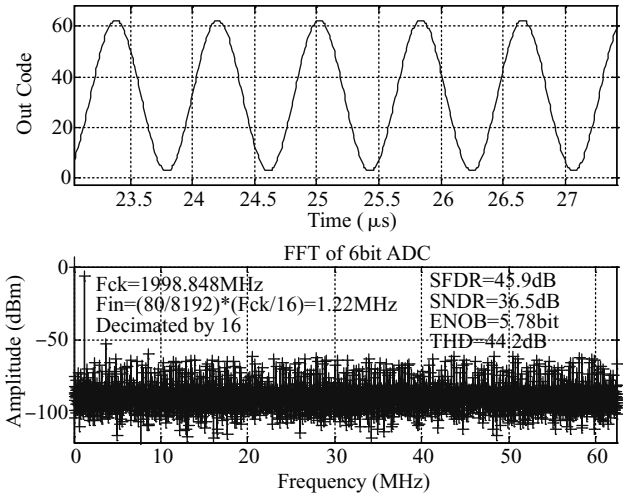

Fig. 11. FFT result.

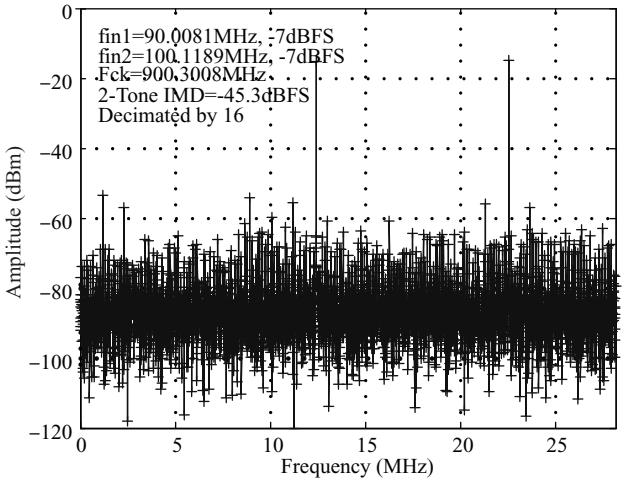

Fig. 12. 2-tone IMD result.

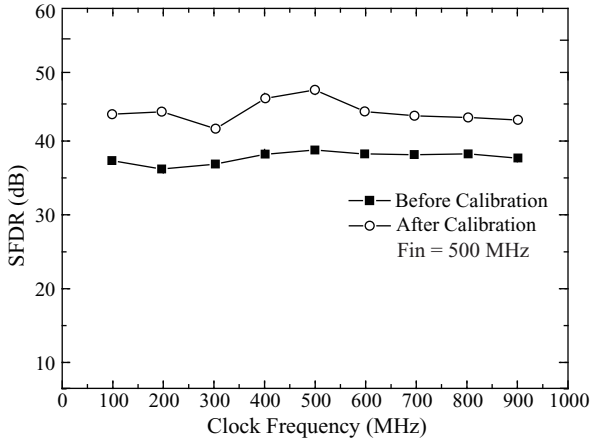

Fig. 13. SFDR result.

After calibration, SFDR could improve by 5 dB and ENOB could improve by about 0.4 bit. The test results prove the efficiency of the calibration method. The chip has a control bit to invoke calibration again during ADC operation if the ambient condition, such as temperature, changes more.

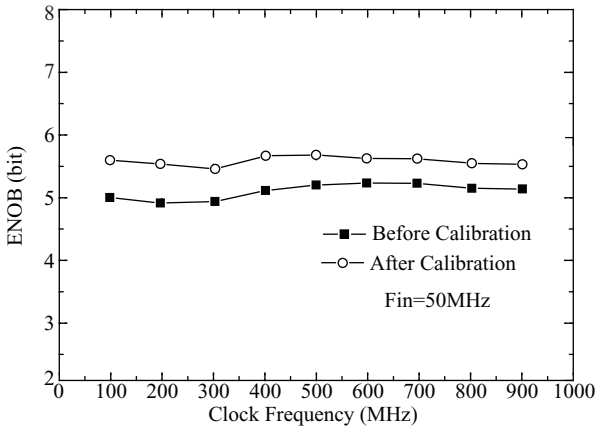

Fig. 14. ENOB result.

Table 1. ADC performance summary.

Parameter	Value
Resolution	6 bit
Supply voltage	1.8 V
Input range	800 mVpp, diff
ENOB	5.78 bit @ 2 GS/s
DNL/INL	0.34 LSB/0.22 LSB
Power consumption	570 mW @ 2 GS/s
Die area	3.1×2.4 mm^2

Table 1 shows a performance summary of the proposed ADC.

4. Conclusion

A single channel 2-GS/s 6-bit ADC is implemented in 0.18-μm CMOS technology with foreground calibration. The architecture of the proposed ADC is based on cascade resistive averaging and DAC current trimming. The proposed termination method has an excellent offset averaging effect with lower reference voltage consumption. The foreground self calibration method could improve the linearity and dynamic performance further. The peak DNL and INL are 0.34 LSB and 0.22 LSB, respectively. The SNDR and SFDR reach 36.5 dB and 45.9 dB at 2 GS/s with 570 mW power consumption.

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