Design and verification of a 10-bit 1.2-V 100-MSPS D/A IP core based on a 0.13-μm low power CMOS process

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Abstract: Based on a low supply voltage curvature-compensated bandgap reference and central symmetry Q^2 random walk NMOS current source layout routing method, a 1.2-V 10-bit 100-MSPS CMOS current-steering digital-to-analog converter is implemented in a SMIC 0.13-μm CMOS process. The total consumption is only 10 mW from a single 1.2-V power supply, and the integral and differential nonlinearity are measured to be less than 1 LSB and 0.5 LSB, respectively. When the output signal frequency is 1–5 MHz at 100-MSPS sampling rate, the SFDR is measured to be 70 dB. The die area is about 0.2 mm^2.

Key words: current-steering digital-to-analog converter; low power; matching error; current source array; mixed-signal integrated circuits

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1. Introduction

The rapid development of WLAN technology, wireless communication systems and VLSI technology demands better integrity of analog signals at the same time as the speed of the digital signal process is continuously increasing. For example, the micro-processor IP used in the HDTV, analog IP and interface IP are all integrated in an SOC with the deep sub-micro process. Moreover, the demand for high-speed, high-resolution, low-power and reusable A/D and D/A IPs is very strong in fields such as WLAN and CDMA[1].

Nowadays, many local and overseas companies and research institutions have done much work on analog IPs. Many analog IPs, with those designed by Nordic and Chipidea being widely used, make the integration of the SOC simpler. However, the design of IPs is different from the design of dies. The IP design is more focused on general use and reusable in that it can be used in the SOC as much as possible.

Current steering DACs are based on an array of matched current cells organized in unary encoded or binary weighted elements that are steered to the DAC output depending on digital input code. This architecture needs large numbers of highly matching current-steering switches to control and steer the source array. In addition, the bandgap reference with high performance is also a design challenge for high accuracy DAC design[2].

In this paper, a novel low supply voltage curvature-compensated bandgap reference and central symmetry Q^2 random walk NMOS current source layout routing method is applied to a low power CMOS DAC. The DAC is implemented in digital SMIC 0.13 μm CMOS technology and can thus be used as an embodied converter. With a spurious-free dynamic range of 70 dB at 1–5 MHz, this current steering DAC achieves good linearities and the integral and differential nonlinearities are measured to be less than 1 LSB and 0.5 LSB, respectively. The total consumption is only 10 mW from a single 1.2 V power supply. The total chip area is only 0.2 mm^2.

2. DAC architecture

A block diagram of the presented 10-bit segmented architecture is depicted in Fig. 1. The 6 most significant bits (MSB's) (referred to as b_4–b_9 in Fig. 1) are encoded from binary to thermometer code in the thermometer encoder, which steers the unary weighted current source array. The four least significant bits (LSB's) (referred to as b_0–b_3 in Fig. 1), which steer the binary weighted current source array, are delayed by the binary delay block to have equal delay with the MSB's. This architecture is reflected directly in the floorplan of the chip (see also Fig. 5).

Every unary current source is split into 16 units, which are spread across the current source array to compensate systematic and graded errors required for 10-bit linearity with a new place routing method called Q^2 random walk, which will be described next. The current in the unit source is I_{unit} and the output of current-steering is given by Eq. (1):

$$I_{\text{OUT}} = I_{\text{unit}} \sum_{k=3}^{0} b_k 2^k + 16 I_{\text{unit}} \sum_{k=9}^{6} b_k 2^{k-6}. \quad (1)$$

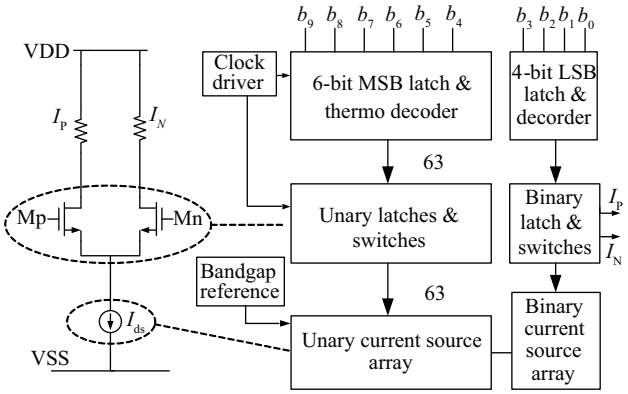

Fig. 1. Block diagram and floorplan of the modified segmented DAC.

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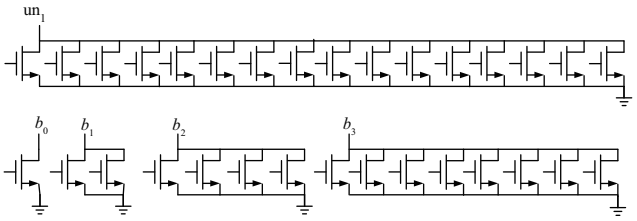

Fig. 2. Implementation of unary and binary current sources.

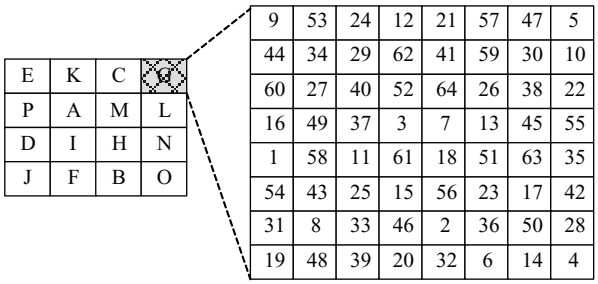

Fig. 3. Proposed unit current source switch sequence for 6-bit MSB.

3. DAC implementation

3.1. Switching and current array implementation

The latches and the current switches Mp and Mn (see Fig. 1) are grouped in the switch/latch array in the middle of the chip. The unary current sources are implemented by connecting 16 units of the array in parallel. The least significant bit b_0 is implemented by 1 unit of the array, bit b_1 is implemented by connecting 2 units of the array in parallel, bit b_2 by 4 units in parallel and bit b_3 by 8 units in parallel, as depicted in Fig. 2.

3.2. Current array placement

A high accuracy current-steering DAC can only be achieved by tackling all possible random, systematic, and graded errors. Important effects that must be taken into account are:

(1) Random errors: device mismatches.

(2) Systematic and graded errors: output impedance of the current source and switch; edge effects; voltage drop in the supply lines; thermal gradients; CMOS technology related error components (such as doping gradients; oxide thickness gradients resulting in a thermal voltage shift across the die).

The random error of the current sources is determined by matching properties, which determine the dimensions of the unit current source. Monte Carlo analysis is always used to simulate the matching characterization of the devices[3]. But in the case of high resolution DAC design, this means a large hardware cost and a very time-consuming step. The statistical relationship has been investigated analytically, resulting in a new and accurate formula directly expressing the relationship between the INL yield specification, the resolution, and the relative unit current standard deviation for the D/A converter[4]. Assuming a normal distribution for the unit current sources, the required accuracy on these current sources is given by:

$$\frac{\sigma(I)}{I} \leqslant \frac{1}{2C\sqrt{2^N}}, \quad C = \text{inv\_norm}\left(0.5 + \frac{\text{yield}}{2}\right), \quad (2)$$

where $\sigma(I)/I$ means the relative standard deviation of a unit current source, N is the resolution of the D/A converter, inv_norm means inverse cumulative normal distribution and yield is the relative number of D/A converters with an INL$<1/2$ LSB. To achieve a 99.7% INL yield specification, the specification for the unity current-source matching is 0.5%[5]. Based on these results and the size versus matching relation for MOS transistors, the dimensions of the current source transistors are given by[6]:

$$W^2 = \frac{I}{2KP\left[\dfrac{\sigma(I)}{I}\right]^2}\left[\frac{A_\beta^2}{(V_{GS}-V_T)_{CS}^2} + \frac{4A_{VT}^2}{(V_{GS}-V_T)_{CS}^4}\right],$$
$$L^2 = \frac{KP}{2I\left[\dfrac{\sigma(I)}{I}\right]^2}\left[A_\beta^2(V_{GS}-V_T)_{CS}^2 + 4A_{VT}^2\right]. \quad (3)$$

The unary and binary current sources are built up out of the wider basic current source transistor, as indicated in Fig. 2. The edge effect (current matching errors at the edge of the current source array) can be avoided by placing sufficient rows and columns of dummy current source cells at the edges[7].

One source of nonlinearity is the finite output impedance of the current source. When output voltage varies between zero and full scale, a different number of current sources are connected to the output, and therefore different impedances are seen at the output node:

$$R_{out} = R_L // \frac{r_o}{j}. \quad (4)$$

The parameter j indicates the number of current sources that are switched on by the thermometer encoder. R_L is the load, and r_o is the output resistance of the current source transistor and the switch transistor. The variation in output impedance causes nonlinearity at the output, given by:

$$\text{INL} = \frac{I_{tot}R_L^2M^2}{4r_o}, \quad (5)$$

where I_{tot} is the full-scale current and M is the number of current sources. Due to the large L of the unit current source, the output resistance r_o is sufficiently high to avoid any impact on the linearity error.

The current source array contains units with thermal gradients and technology-related errors that are linear and quadratic in spatial distribution. It is noted that some current sources have an error higher than average (positive error) and others have an error below average (negative). The linearity of the DAC is now determined by the accumulation of these errors when the current sources are switched on one by one. It is essential to keep the accumulated error as low as possible[8].

There are 64 current sources in the current source array (see Fig. 3). Only 63 current sources are required for the DAC function. One of the 64 current sources is used as a biasing circuit.

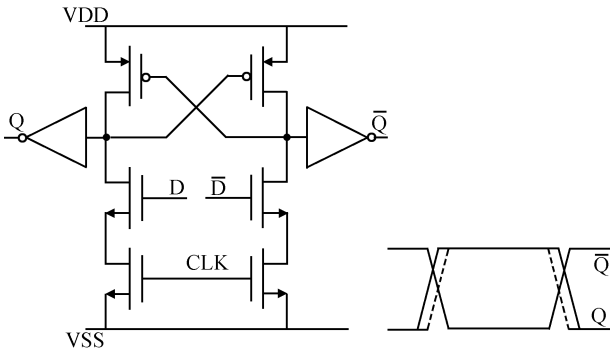

Fig. 4. Switch latch.

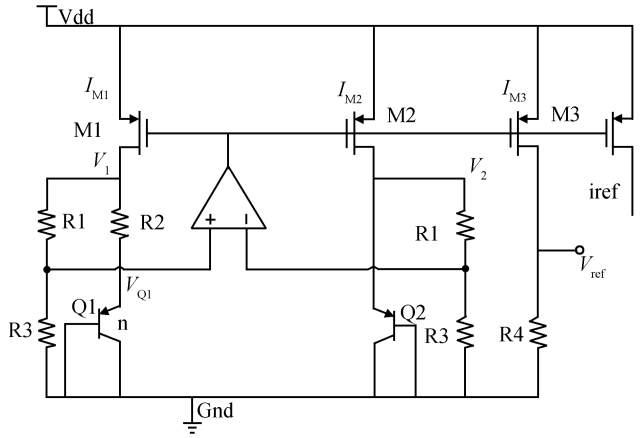

Fig. 5. Proposed bandgap reference circuit.

The switching sequence of the 63 unary current sources is an important design parameter to limit the INL. Many studies have proposed some method to improve the performance of the current source array, such as the work done in Refs. [4, 7]. In this work, the central symmetry Q^2 random walk current source routing method is applied. The 8×8 current source matrix is divided into 16 regions. The goal is to "randomize" the different error contributions (positive and negative) so that no error accumulation could be occurred, as shown in Fig. 3.

3.3. Switch latch of the DAC

The switch latch is very important for the DAC. Figure 4 shows a schematic of the switch latch. First, it synchronizes the steering signals—bad synchronization leads to distortion. Second, by properly sizing the latch, the cross point of the latch's output has been shifted as we can see in Fig. 4, making the circuit avoid switching of both switch transistors simultaneously and thus reducing the current variation due to the drain voltage variation of the current source. Lastly, it reduces digital feedthrough to the output[9].

3.4. Bandgap voltage reference implementation

In this paper, we present a bandgap circuit capable of generating a reference voltage of 0.6 V. The bandgap architecture can operate with a 1.2 V supply, while using BiCMOS technology. Despite its simplicity, the circuit also incorporates a network that allows us to accurately correct the curvature error and achieve good temperature features[10].

Two components build up the output voltage of a bandgap reference (V_{ref}). One is the voltage across a directly biased diode (based–emitter voltage) (V_{BE}) and the other is a term proportional to the absolute temperature (V_t) (PTAT). The negative temperature coefficient of the former term compensates for the positive temperature coefficient of the latter. The bandgap voltage is given by:

$$V_{ref} = V_{BF} + nV_t. \tag{6}$$

Figure 5 shows a schematic diagram of a circuit which implements the described operation. We achieve a fraction of the traditional bandgap voltage by scaling both terms of Eq. (6), using current terms proportional to V_{BE} and nV_t, respectively. These currents are suitably added and transformed into a voltage with a resistor. Two diode connected bipolar transistors with emitter area ratio n drain the same current, leading to a ΔV_{BE} equal to $V_t \ln n$. $V_1 = V_2 = V_{BE}$, the current in M1, M2 and M3 ($I_{M1} = I_{M2} = I_{M3}$) is given by:

$$I_{M1} = \frac{V_1}{R_1 + R_3} + \frac{\Delta V_{BE}}{R_2}. \tag{7}$$

As shown in Fig. 4, $V_{ref} = I_{M1} R_6$, as a result the output voltage is then given by:

$$V_{ref} = \frac{R_6}{R_1 + R_3} V_{BE} + \frac{R_6}{R_2} V_t \ln n. \tag{8}$$

The compensation of the temperature coefficients of V_t and V_{BE} is ensured by choosing values of n and of the resistor ratio. In this paper, we chose $n = 8$. Since transistors M1, M2 and M3 maintain almost the same drain–source voltage, independently of the actual supply voltage, the power supply rejection ratio of circuit is only determined by the operational amplifier. The temperature dependence of the resistors can be compensated in fabricating with the same kind of material.

With the consideration above, we realized the DAC circuit and generated the GDSII file.

4. Measurement

With the help of SMIC, the GDSII file was sent to the SMIC 0.13 μm CMOS process and taped out in October, 2008. The packaged DAC was tested using UltraFlex in Teradyne during June 2009. The noise and coupling signal were isolated in the PCB with several layers for good signal integrity and the match route of the differential signal was for symmetry and consistency. Figure 6 shows the layout of the DAC. Figures 7–9 are the tested SFDR, DNL and INL characteristics of the DAC. From these figures, we can see that when the sample frequency is 100 MHz and the signal frequency is 1–5 MHz, the SFDR of the DAC can be 70 dB. The DNL is less than 0.5 LSB, and the INL is less than 1 LSB. The result reaches the expected goal.

Table 1 gives a summary of the characteristics of the DAC, and Table 2 shows a comparison between the proposed DAC and the DACs in reference.

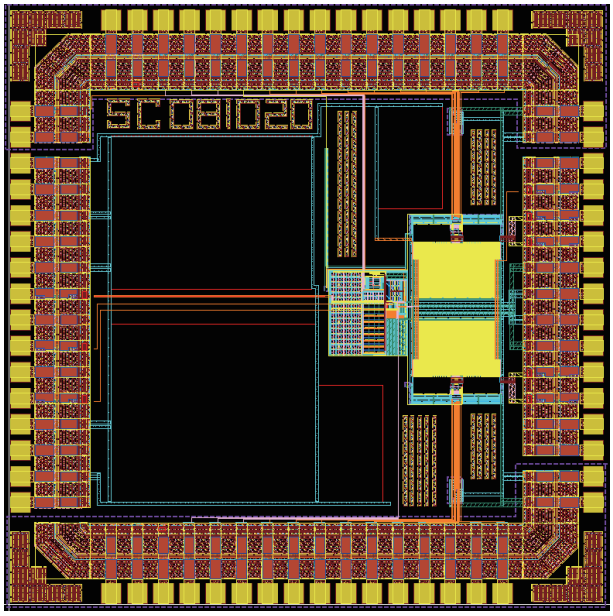

Fig. 6. Layout of the DAC.

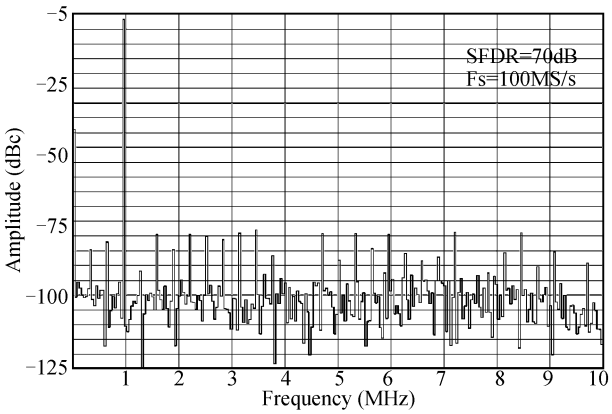

Fig. 7. DAC SFDR characteristic.

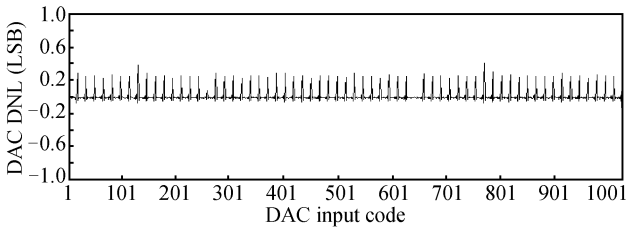

Fig. 8. DAC DNL characteristic.

5. Conclusion

Based on a low supply voltage curvature-compensated bandgap reference and central symmetry Q^2 random walk NMOS current source layout routing method, a 1.2-V 10-bit 100-MSPS CMOS current-steering digital-to-analog converter is implemented in a SMIC 0.13-μm CMOS process. By using the DAC architecture in this paper, the die area and current consumption can be significantly reduced. The integral and differential nonlinearity are measured to be less than 1 LSB and 0.5 LSB, respectively. When the output signal frequency is 5 MHz at 100 MSPS sampling rate, the SFDR is measured to be 70 dB and the total power consumption is only 8 mW. The bias circuit consumes about 3 mW and the DAC core consumes about 5 mW from a single 1.2 V power supply. The die area is about 0.2 mm^2.

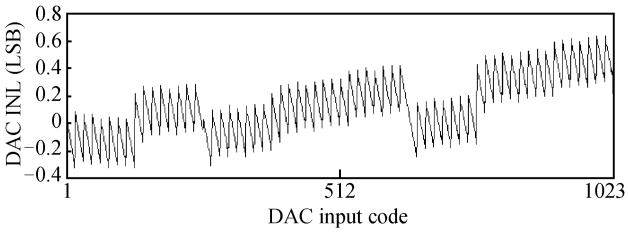

Fig. 9. DAC INL characteristic.

Table 1. Measured performance of the 10-bit DAC.

Parameter	Value
Process	0.13 μm CMOS
Resolution	10 bit
DNL	< 0.5 LSB
INL	< 1 LSB
Update rate	100 MSPS
Full-scale output rage	1 Vptp
SFDR (at f_{out} = 1–5 MHz)	70 dB
SNR	61 dB
THD	–66 dB
Power consumption	8 mW
Power supply	1.2 V
Die size	0.2 mm^2

Table 2. Comparison with other DACs.

Parameter	SSIPEX	Ref. [11]	Ref. [12]
Technology	0.13 μm CMOS	0.35 μm CMOS	0.8 μm CMOS
Resolution	10	10	10
Sampling frequency (MHz)	100	500	125
Area (mm^2)	0.2	0.6	1.8
SFDR	70 @ 1–5 MHz	73 @ 8 MHz	56 @ 3.9 MHz
DNL (LSB)	< 0.5	0.1	0.21
INL (LSB)	< 1	0.2	0.23
Power dissipation (mW)	8	18 (analog) 20 (digital)	150

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