A low jitter, low spur multiphase phase-locked loop for an IR-UWB receiver*

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Abstract: A low jitter, low spur multiphase phase-locked loop (PLL) for an impulse radio ultra-wideband (IR-UWB) receiver is presented. The PLL is based on a ring oscillator in order to simultaneously meet the jitter requirement, low power consumption and multiphase clock output. In this design, a noise and matching improved voltage-controlled oscillator (VCO) is devised to enhance the timing accuracy and phase noise performance of multiphase clocks. By good matching achieved in the charge pump and careful choice of the loop filter bandwidth, the reference spur is suppressed. A phase noise of –118.42 dBc/Hz at a frequency offset of 1 MHz, RMS jitter of 1.53 ps and reference spur of –66.81 dBc are achieved at a carrier frequency of 264 MHz in measurement. The chip was manufactured in 0.13 μm CMOS technology and consumes 4.23 mW from a 1.2 V supply while occupying 0.14 mm^2 area.

Key words: PLL; multiphase; ring oscillator; RMS jitter; reference spur; IR-UWB
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1. Introduction

As wireless communication systems move towards high data rate applications such as the impulse radio ultra-wideband (IR-UWB), high frequency, low phase noise and low spur phase-locked loops (PLLs) become key building blocks in the frequency synthesizer.

The phase noise requirement of these PLLs in IR-UWB is less stringent than that required in conventional standards such as GSM. Thus, PLLs using integrated voltage-controlled oscillators (VCOs) are becoming more attractive. Ring oscillators have been widely used for integrated VCOs due to their easy integration, wide range of tuning property, multiphase output, small area, and low power consumption. The phase noise performance of this kind of VCO can take better advantage of technology scaling since scaling translates directly into a faster slew rate and, hence, better phase noise performance[1].

Current mismatch in the charge pump (CP) is the major cause of reference spur in a PLL. This is especially undesirable for the analog-to-digital converter (ADC) of a receiver where clock spurs convolute with the input signal spectrum[2]. The reference spur can be reduced by simply decreasing the loop filter bandwidth. But this approach will result in less suppression of VCO phase noise. Therefore, careful consideration is necessary to maximize VCO phase noise suppression while minimizing reference spur.

This paper presents a low jitter, low spur 0.13 μm CMOS PLL based on a ring oscillator for an IR-UWB receiver. The PLL is designed to operate at 264 MHz with multiphase outputs. The system requirements of PLL and its topology for multiphase outputs are presented and analyzed. The circuit implementation of PLL is described.

2. Architecture

A simplified block diagram of the sub-sampling IR-UWB receiver is shown in Fig. 1. The PLL should provide a 4.224 GHz clock as the ADC sampling clock with RMS jitter less than 2.36 ps. Through dividers and clock drivers, the PLL also provides 16-phase 264 MHz clocks for 16-channel comparators in ADC. The power budget of this PLL is 10 mW under a supply voltage of 1.2 V.

A previous design of PLL[3] which adopts an LC oscillator has shown good phase noise and spur performance. However, there are some disadvantages with that PLL. First, the phase noise performance of LC oscillators highly depends on the quality factor of on-chip spiral inductors. In most CMOS processes, it is difficult to obtain a high quality factor of the inductor. Second, the tuning range of LC oscillators (around 20%–30%) is relatively low. Therefore, the output frequency may fall out of the locked range because of process variation. Third, on-chip spiral inductors occupy a large chip area which is undesirable for cost and yield considerations. Fourth, the need for numerous high speed dividers and power hungry high speed clock drivers not only increase the total power consumption of the receiver, but also add to the accumulated supply noise.

Using a ring oscillator can overcome these disadvantages due to its intrinsic characteristics. Meanwhile, the effective

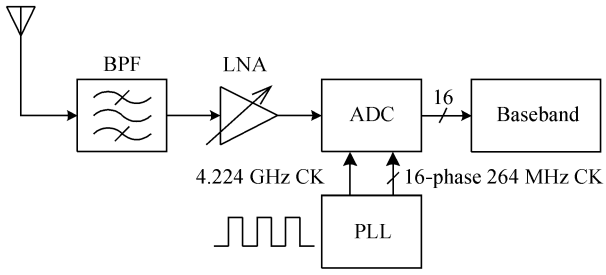

Fig. 1. Simplified block diagram of the IR-UWB receiver.

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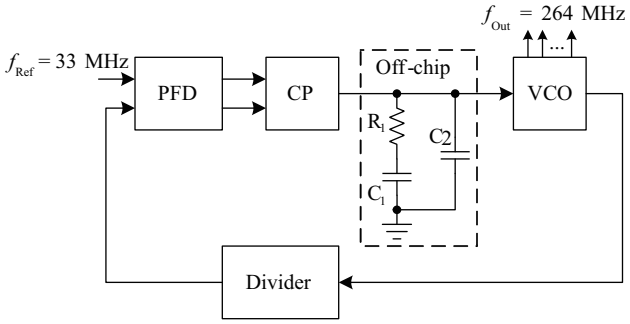

Fig. 2. Block diagram of the proposed PLL.

sampling rate f_{sampling} of the N-phase ring oscillator output is $f_{\text{sampling}} = Nf_{\text{osc}}$, where f_{osc} is the carrier frequency of the oscillator. When f_{osc} is 264 MHz and N equals 16, f_{sampling} will be 4.224 GHz. Thus, a 16-phase 264 MHz ring oscillator can satisfy the clock requirements of the IR-UWB receiver.

However, ring oscillators have poor phase noise characteristics compared with LC oscillators. Although the noise performance can be improved by increasing the current of the VCO, in practice the progress is restricted by the given power budget. So it is necessary to optimize the VCO against noise/jitter performance to make the PLL meet the specifications of the system. The optimization strategy will be discussed in the next section.

A functional block diagram of the proposed PLL is shown in Fig. 2. The PLL includes a phase and frequency detector (PFD), CP, off-chip loop filter, VCO, and divider.

3. PLL design

3.1. VCO

For PLLs with multiphase outputs, the timing accuracy of the multiphase clocks will depend on the matching accuracy among delay cells. However, the mismatch among active devices is worse in advanced deep-micron technology. The mismatch-induced error voltage in the differential delay cells leads to unbalanced currents, affecting the delay accuracy of the delay cells. The shifted-averaging technique[4, 5] can be used to average the mismatch of the differential delay cells.

For instance, Figure 3 shows a shifted-averaging VCO with eight differential delay cells. It has two features. First, the timing error of the delay cells can be averaged to provide the 50% duty cycle and reduce the static timing error. Second, the inputs of each delay cell in the shifted-averaging VCO do not come from the same cell; the mismatch-induced errors occurring at the outputs of the differential delay cells are independent and mutually uncorrelated. Thus, 3 dB improvement in the jitter performance could be obtained[5]. In addition, this technique changes only the interconnection of the differential delay cells and does not increase the hardware and power consumption.

To improve the noise performance of the VCO, the noise sources of delay cells should be considered. The device noise from active transistors is one of the dominant noise sources. For the device noise generated by current flow, $1/f$ noise is dominant at low frequencies around DC, while thermal noise is dominant at high frequencies. Both of the device noise components should be considered for a low noise VCO.

In general, the jitter or phase noise of a VCO is determined by the amount of noise injected to the circuit node under voltage transition. Once the voltage transition saturates to a predefined value, the injected noise does not affect the phase noise performance.

According to Ref. [6], the VCO shows the best performance with respect to device noise when the output waveform is shaped such that the portion of transition time in a period is minimized. Therefore, two pre-charged transistors M2 and M3 are added in the proposed delay cell, as shown in Fig. 4(b). A high slew rate of the output waveform is achieved; as a result, the phase noise performance is improved.

Compared with the traditional delay cell[7] in Fig. 4(a), another difference is the tail current transistor M1, because the tail current transistor limits the slew rate (I_{tail}/C_L) of the delay cell and hence makes the VCO susceptible to device noise. Also, the low frequency $1/f$ noise in the tail current is up-converted into the carrier frequency band due to the nonlinearity of the cell. Therefore, the tail current transistor M1 is removed.

3.2. PFD and CP

The PFD and CP block in the proposed PLL is the same as in our previous work[3]. In that paper, design considerations about in-band noise optimization and mismatch of CP were discussed and analyzed. In this paper, the reference spur due to the mismatch of CP is calculated.

Generally, the mismatch of CP up and down currents ΔI_{CP} causes a periodic ripple on the VCO tuning voltage that results in a spur. The PLL model for spur analysis in Fig. 5 applies for calculating the reference spur. According to this model, the PLL spur level relative to carrier power is given by a multiplication of the loop filter current, loop filter impedance and VCO transfer function. The approximate expression is[8]:

$$\text{spur}(f_{\text{VCO}} \pm f_{\text{Ref}}) = 20\lg\left(\frac{2K_{\text{VCO}}\Delta I_{\text{CP}}}{\pi f_{\text{Ref}}}\,|Z_{\text{filt}}(f_{\text{Ref}})|\right) + 10\lg\left\{\alpha^2 - 2\alpha\sin\alpha\cos\left[\alpha\left(1+\frac{\Delta I_{\text{CP}}}{I_{\text{CP}}}\right)\right] + \sin\alpha^2\right\},$$

where $\alpha = \pi\tau_{\text{PFD}}f_{\text{Ref}}$, τ_{PFD} is the reset delay of the PFD, f_{Ref} is the reference frequency, K_{VCO} is the VCO tuning gain in Hz/V, I_{CP} is the nominal CP current, and $Z_{\text{filt}}(f_{\text{Ref}})$ is the loop filter impedance at f_{Ref}.

The expression above shows that the reference spur can be reduced by decreasing $Z_{\text{filt}}(f_{\text{Ref}})$, K_{VCO}, τ_{PFD}, and ΔI_{CP}. The loop filter is determined by the desired PLL bandwidth, phase margin and settling time, so the amount of impedance that can be lowered is limited. K_{VCO} is proportional to the tuning range of the PLL. A wide tuning range is needed to keep the output frequency of the PLL in the locked range despite supply, process and temperature variation. Hence, τ_{PFD} and ΔI_{CP} are two degrees of freedom to lower the reference spur. τ_{PFD} is deliberately added to the reset path of the PFD to avoid phase noise degeneration caused by the dead zone. The delay time is minimized to several hundreds of pico-seconds in the circuit design, so that the noise contributed by PFD and CP is minimized and the steady mismatch of CP is reduced. By balancing the switch signals of CP in the circuit design, a good dynamic matching characteristic of CP is achieved. Therefore, the minimized τ_{PFD} and ΔI_{CP} guarantee good spur suppression.

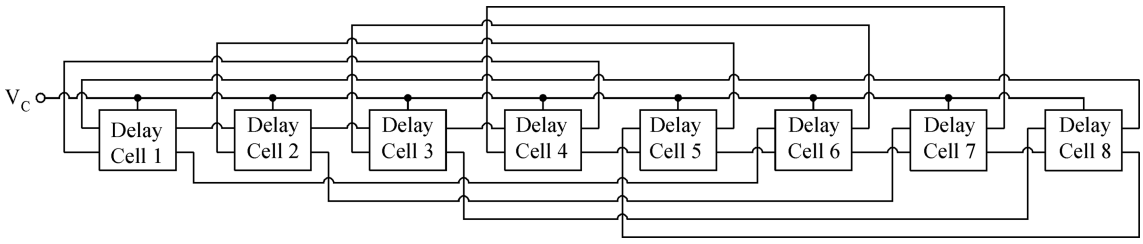

Fig. 3. Shifted-averaging VCO.

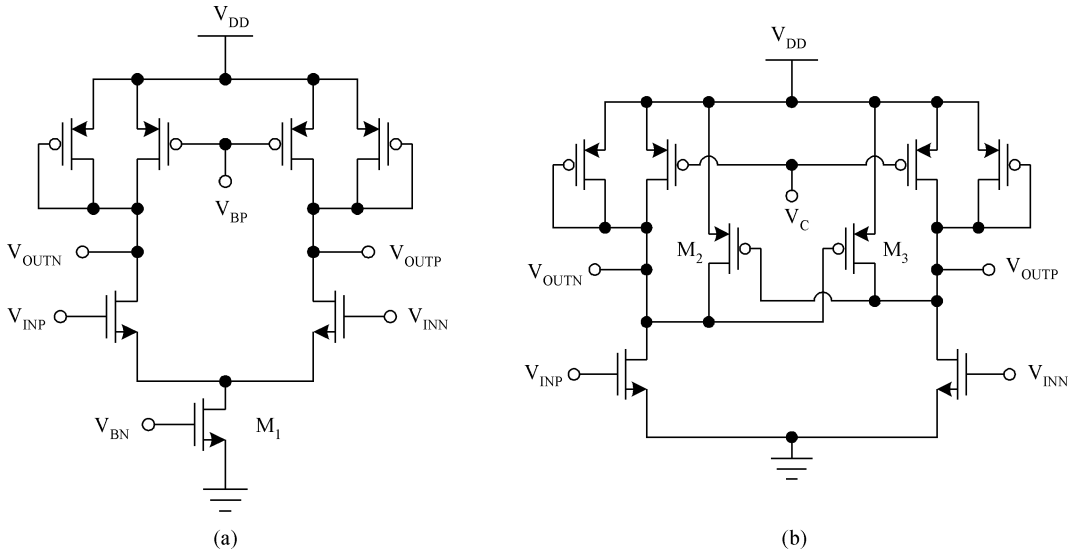

Fig. 4. (a) Traditional delay cell[7]. (b) Proposed delay cell.

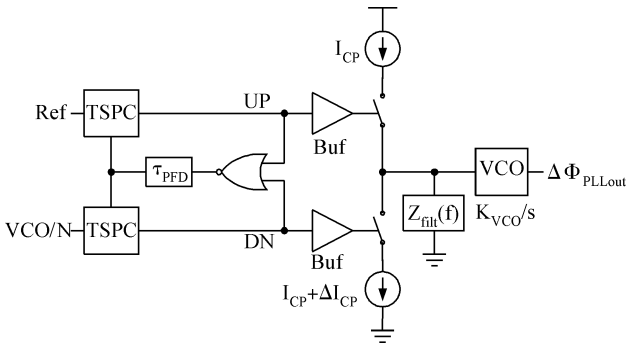

Fig. 5. PLL model for spur analysis.

3.3. Loop filter

As shown in Fig. 2, a traditional second-order passive loop filter is used in the proposed PLL. The loop bandwidth ω_c is:

$$\omega_c = \frac{K_{PD}K_{VCO}R_1}{N}\frac{C_1}{C_1+C_2}\frac{\dfrac{\omega_{p2}}{\sqrt{\omega_c^2+\omega_{p2}^2}}}{\dfrac{\omega_c}{\sqrt{\omega_c^2+\omega_z^2}}},$$

$$\omega_z = \frac{1}{R_1C_1},\ \omega_{p2} = \frac{C_1+C_2}{R_1C_1C_2},$$

where K_{PD} is the PFD gain and CP, N is the division ratio of the divider.

The Agilent software advanced design system (ADS) is used in the loop filter design for frequency response simulation and loop parameter optimization. When the loop bandwidth is chosen between 100 and 300 kHz, for example, the value of C_2 is on the order of nano-farad. So the loop filter has to consist of off-chip resistors and capacitors. An off-chip loop filter also has the advantage of adjustable bandwidth.

4. Experimental results

The proposed PLL is manufactured in the SMIC 0.13 μm CMOS process. The core area is 0.14 mm^2 excluding pads. A microphotograph of the die is depicted in Fig. 6. To reduce the supply noise and the off-chip loop filter noise on the VCO control signal, large on-chip bypass capacitors realized with MOS transistors and MIM capacitors are included wherever space allows.

The phase noise plot and jitter histogram of the PLL at 264 MHz output are shown in Figs. 7 and 8, respectively. The phase noises are –104.16 dBc/Hz at a frequency offset of 100 kHz and –118.42 dBc/Hz at a frequency offset of 1 MHz. The RMS jitter and peak-to-peak jitter are 1.53 ps and 9.97 ps, respectively. These specifications are sufficiently low to meet the IR-UWB receiver requirements. The PLL output spectrum is shown in Fig. 9, which indicates the –66.81 dBc reference spur level. The good phase noise and spur performance proves that the techniques used in the circuit design are efficient.

Since the delay cell only consists of a stack of one NMOS

Table 1. Performance summary and comparison.

Reference	Ref. [7]	Ref. [9]	Ref. [10]	This work
Supply voltage (V)	1.5	1.8	1.2	1.2
Process	0.13 μm CMOS	0.18 μm CMOS	0.13 μm CMOS	0.13 μm CMOS
Center frequency (MHz)	240	270	128	264
VCO architecture	Ring	Ring	Ring	Ring
Phase noise (dBc/Hz)	—	—	—	-118.42 @ 1 MHz
RMS/p-p jitter (ps)	4/30.5	< 4 / < 32	4.62/34.66	1.53/9.97
Reference spur (dBc)	—	< -57	—	–66.81
Power (mW)	7	24.3	36	4.23
Chip area (mm^2)	0.18	0.16	0.506	0.14

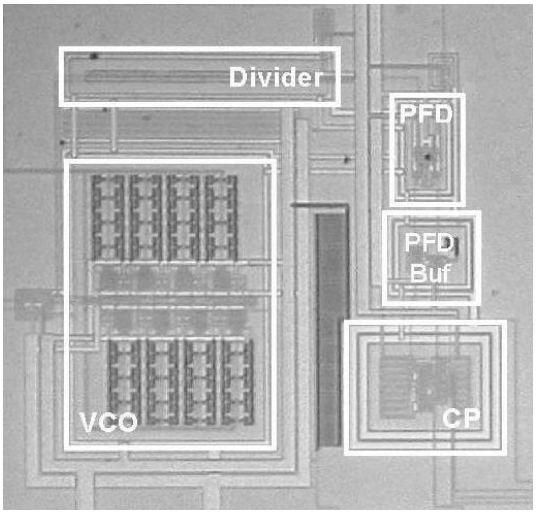

Fig. 6. Die microphotograph.

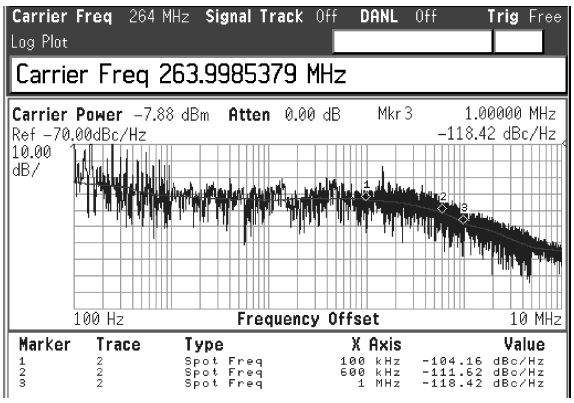

Fig. 7. Measured PLL phase noise at 264 MHz output.

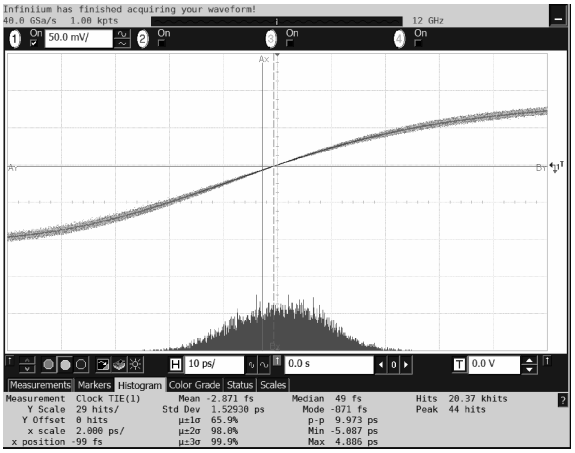

Fig. 8. Measured PLL jitter histogram.

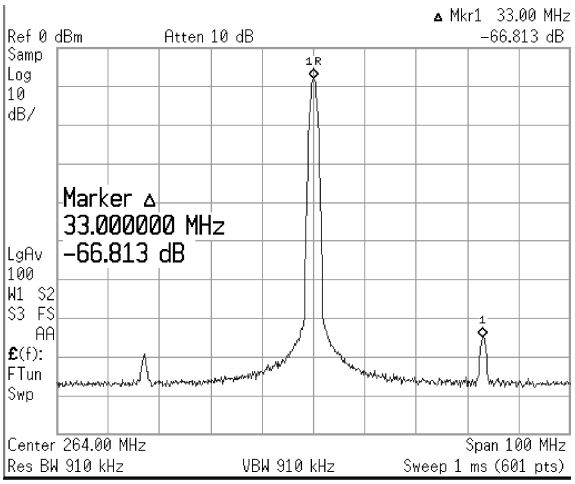

Fig. 9. Measured output spectrum of the PLL.

and one PMOS transistor, the measured PLL can function at supply voltages as low as 0.87 V. Under a 1.2 V supply, the chip consumes 3.527 mA current. The main performance of the proposed PLL is summarized and compared in Table 1.

5. Conclusion

A low jitter, low spur 0.13 μm CMOS PLL based on a ring oscillator for an IR-UWB receiver is presented in this paper. The system requirements of the PLL and its topology for multiphase outputs are discussed. In the circuit implementation the noise/jitter performance of the VCO was optimized and the reference spur due to the mismatch of CP was calculated. Measured performance indicates that the optimization strategies are efficient and the spur is kept at a relatively low level. The proposed PLL fulfills the specifications of the system requirements while overcoming the disadvantages of the LC oscillator, making it suitable for an IR-UWB receiver.

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