

Influence of the external component on the damage of the bipolar transistor induced by the electromagnetic pulse*

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Abstract: A study on the influence of the external resistor and the external voltage source during the injection of the electromagnetic pulse (EMP) into the bipolar transistor (BJT) is carried out. Research shows that the increase of the external resistor R_b at base makes the burnout time of the device decrease slightly, the increase of the external voltage source V_{be} at base can aid the damage of the device when the magnitude of the injecting voltage is relatively low and has little influence when the magnitude is sufficiently high causing the device appearing the PIN structure damage, and the increase of the external resistor R_e can remarkably reduce the voltage drops added to the device and improve the durability of the device. In the final analysis, the effect of the external circuit component on the BJT damage is the influence on the condition which makes the device appear current-mode second breakdown.

Key words: electromagnetic pulse; bipolar transistor; current-mode second breakdown; external component

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1. Introduction

Electromagnetic pulse (EMP) is one of the main reasons inducing the external electrical-over-stress, which has a great effect on the device reliability. There were early studied on the subject of the EMP-induced damage on the single device^[1–6], which provided a certain theoretical basis to the EMP assessment and hardening of the electronic systems. However, the semiconductor device is not in circuit alone, it is useful to study the influence of the external component to reflect truly the effect of EMP on the device during the injection of EMP into the circuit.

Hane *et al.*^[7] studied the influence of the external resistor at collector on the device damage induced by EMP. When the value of the external resistor is relatively low the current-mode second breakdown (CSB) occurs with extremely short delay time, and when the value of the external resistor is sufficiently high the thermal-mode second breakdown (TSB) occurs with long delay time. Based on the current distribution relationship, Chen *et al.*^[8] researched the influence of typical components during the damage process of the device under EMP.

The purpose of this paper is to present the influence of the component on the typical position of the bipolar transistor under the effect of EMP. Based on the damage mechanism of the single BJT induced by EMP, three typical connections of the bipolar transistor are analyzed. It is demonstrated that the external component can change the speed of the device damage.

2. Device structure

The geometric structure of the analyzed bipolar n^+p-n^+ silicon transistor is shown in Fig. 1. Only half emitter

finger is analyzed due to the symmetry. Here B, C, and E stand for its base, collector, and emitter respectively; P and N represent the p- and n-type silicon regions, respectively; N^+ denotes the heavy doped region of the n-type silicon. Referring to the research method in Refs. [1–4], here the authors take the device lattice temperature reaching the silicon melting point of 1688K as the burnout criteria. By use of the device simulator Medici and the curve fitting soft Origin, the influence of the external resistor R_b at base, the voltage source V_{be} at base, and the external resistor R_e at emitter on the burnout time of BJT under EMP is analyzed.

3. Results and analysis

3.1. Damage effect of the single device

Under the intense EMP the single device will appear CSB, which is initiated only when the emitter is injecting^[9]. At the beginning of voltage rising, the current of the reverse-biased PIN under the emitter only flows to the base and results in a

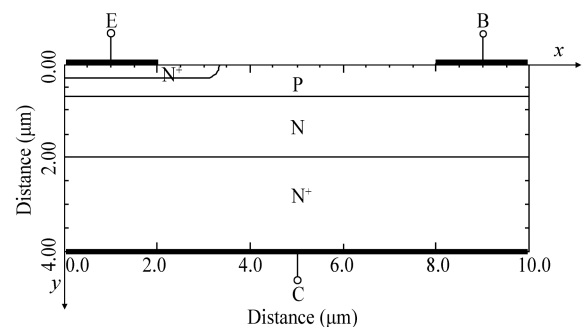


Fig. 1. Two-dimensional n^+p-n^+ transistor structure.

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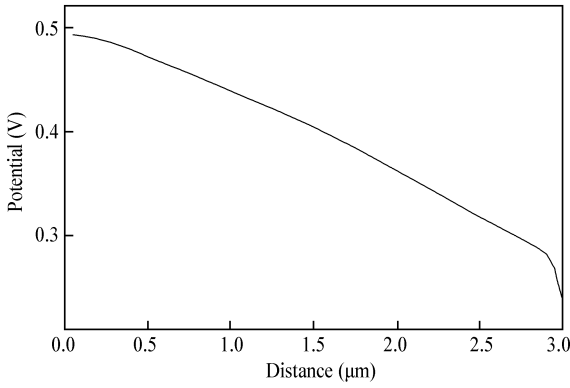


Fig. 2. Transverse voltage drops along the horizontal direction (line $y = 0.3 \mu\text{m}$)^[10].

transverse potential drops. The authors have analyzed the transient response of the single BJT under the intense EMP in Ref. [10], and Figure 2 depicts the transverse voltage drops along the horizontal direction from the emitter center to the emitter edge at line $y = 0.3 \mu\text{m}$ before CSB occurs. When the current of the reverse-biased PIN has built up sufficiently to forward-bias a portion of the emitter, the current-mode second breakdown happens, the current increases sharply and burns the device finally. Due to that the transverse voltage drops, the center of the emitter is forward biased firstly resulting the damage appears firstly near the position under the center of the emitter.

3.2. Influence of the external resistor R_b at base

The simulation circuit with an external resistor R_b at base is illustrated in Fig. 3. The bipolar transistor is injected voltage on the collector with the magnitude setting at 50, 55, and 60 V respectively. Figure 4 depicts the variation of the burnout time with R_b as a parameter. It is shown that the burnout time has little decrease with the increase of R_b . The mechanism of the influence of R_b on the burnout time is that the influence of R_b on the condition which makes the device appear CSB. When the applied voltage can not make the device breakdown, all of the collector current flows to the base through the base spreading resistor r_b and the external resistor R_b at base. It is proposed that when the current is much enough to make the emitter junction forward-bias, the device appears CSB. Assuming that the emitter is forward-biased when the potential drops of the junction reach 0.6 V, the following expression gives the relationships among the base spreading resistor r_b , the external resistor R_b at base and the critical current I_c at which CSB begins.

$$I_c(r_b + R_b) = 0.6. \tag{1}$$

It is seen from Eq. (1) that the external resistor R_b is inversely proportional to the critical current I_c . Accordingly, the greater R_b , the smaller I_c , and the shorter the burnout time. However, the influence of the external resistor at base on the burnout time is not obvious because the current I_c flowing to the base is mainly the reverse-biased current which value is very small (Fig. 4).

The similar experiment was performed in Ref. [9]. For each value of R_b , the critical current I_c at which CSB began was measured, as shown in Table 1. It is seen that the critical current

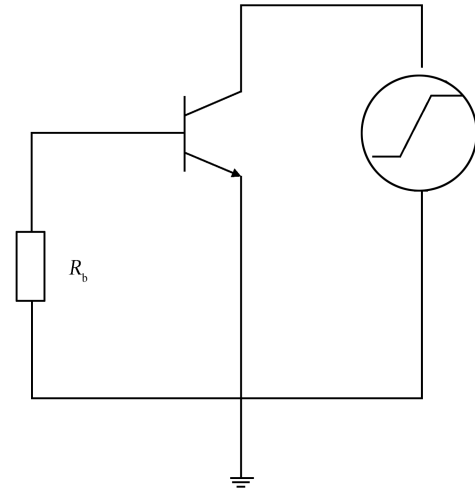


Fig. 3. Circuit diagram with an external resistor R_b at base.

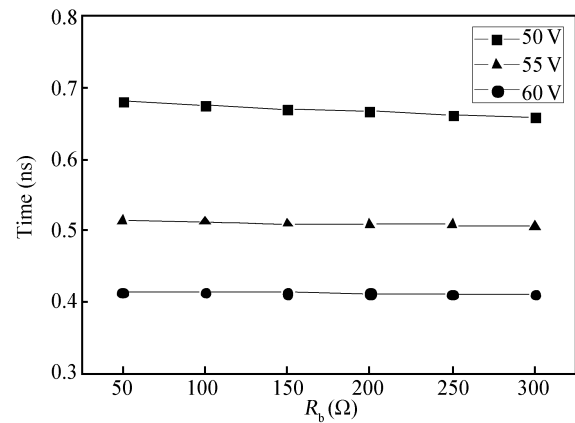


Fig. 4. Dependence of the burnout time on R_b .

Table 1. Relationship between the base resistor and the critical current^[9].

$R_b(\Omega)$	$I_c(\text{mA})$	$R_b I_c(\text{V})$
1000	0.45	0.45
470	0.90	0.42
100	4.2	0.42
47	8.2	0.39
15	18	0.27

I_c gets smaller with the increase of R_b . The variation trend is in agreement with the simulation analysis.

3.3. Influence of the voltage source V_{be} at base

Under the operation state of the bipolar transistor, the emitter junction is always forward-biased. It is necessary to study the influence of the forward-biased emitter junction during the damage process of the device induced by EMP. The simulation circuit with a voltage source V_{be} at base is illustrated in Fig. 5, at which the value of V_{be} is set at 0 V and 0.8 V respectively. Figure 6 shows the relationship between the burnout time and the injecting voltage on the collector with different value of V_{be} . It is seen that the burnout time with $V_{be} = 0.8 \text{ V}$ is shorter than that with $V_{be} = 0 \text{ V}$ under the same magnitude of the injecting voltage. However, the aiding effect of the voltage source

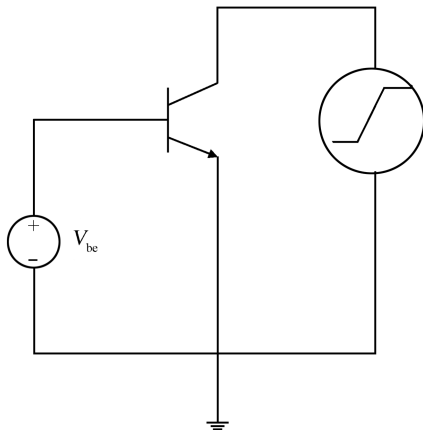


Fig. 5. Circuit diagram with an external voltage source V_{be} at base.

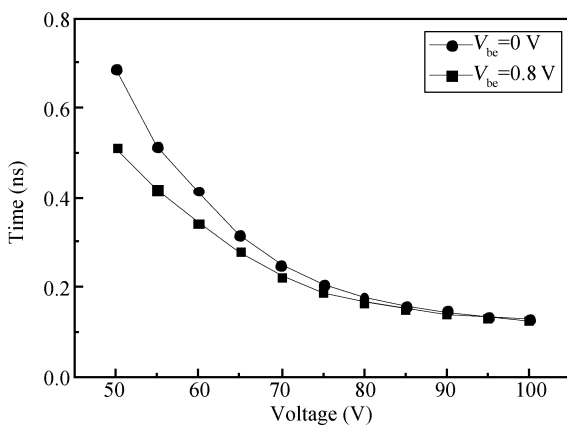


Fig. 6. Dependence of the burnout time on the injecting voltage with different values of V_{be} .

at base decreases gradually as the increase of the magnitude of the injecting voltage (Fig. 6). The reason is that the damage mechanism of the device is different in different injecting levels.

Figure 7 depicts the temperature distributions of the device under 50 V and 100 V injecting voltage respectively. When the magnitude of the injecting voltage is low, the damage of the device results from CSB (Figs. 7(a), 7(b)). The voltage source at base has a significant influence on the burnout time (Fig. 6) since the emitter injection is a necessary condition for the device occurring CSB. But, when the magnitude of the injecting voltage is sufficiently high, the voltage source at base has little effect on the burnout time (Fig. 6) due to the breakdown of the PIN structure composed of the base-epitaxial layer-substrate resulting in a burnout spot at the edge of the base near the emitter region (Figs. 7(c), 7(d)).

3.4. Influence of the external resistor R_e at emitter

In order to stabilize the quiescent operation point, commonly a resistor is inserted in series to the emitter for feedback effect. Figure 8 shows the simulation circuit with an external resistor R_e at emitter. When the collector is injected the pulse voltage, R_e is equivalent to raising the potential of the emitter and reducing the voltage drops on the device. Thus, the greater R_e , the smaller the voltage drops on the device, and the longer

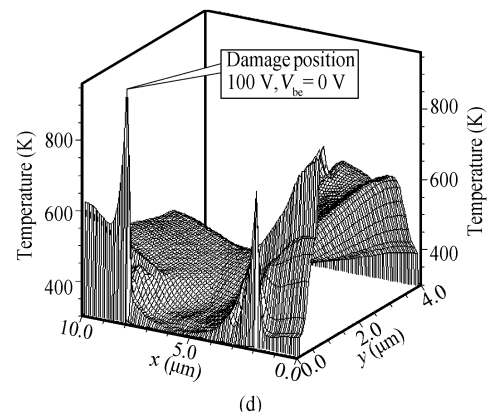
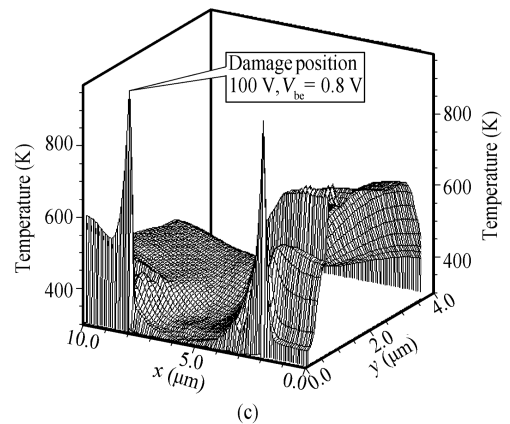
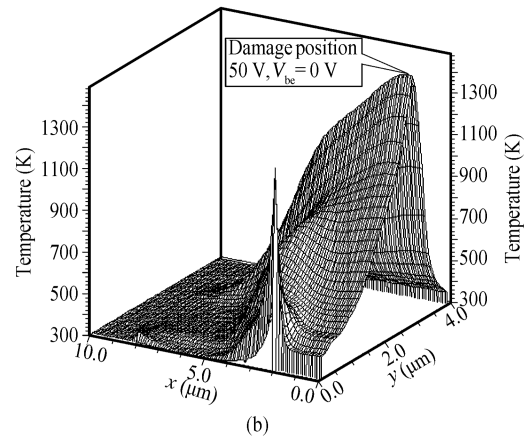
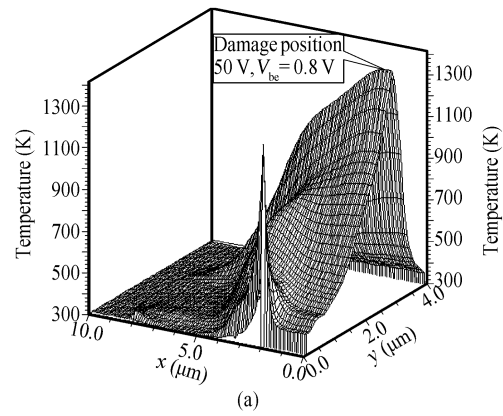


Fig. 7. Temperature distributions of the device under different injecting voltage magnitudes. (a) 50 V with $V_{be} = 0.8$ V. (b) 50 V with $V_{be} = 0$ V. (c) 100 V with $V_{be} = 0.8$ V. (d) 100 V with $V_{be} = 0$ V.

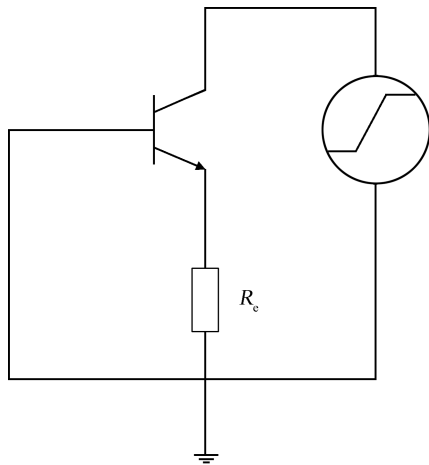


Fig. 8. Circuit diagram with an external resistor R_e at emitter.

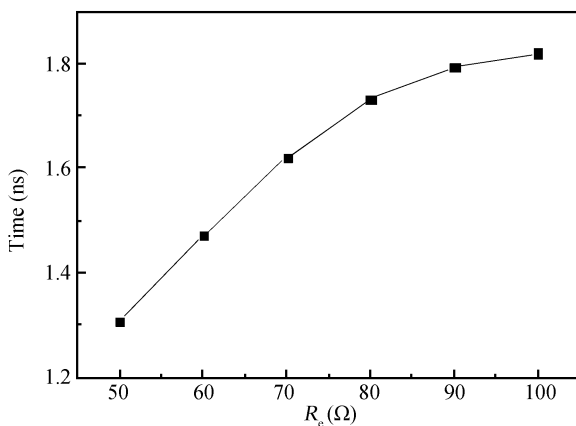


Fig. 9. Dependence of the burnout time on R_e .

the burnout time. The bipolar transistor is difficultly damaged under EMP with R_e at emitter. Figure 9 illustrates the influence of R_e on the burnout time with an injection pulse voltage of 50 V on the collector. It is seen that the burnout time is increasing as the increase of R_e . The external resistor at emitter can not only stabilize the quiescent operation point, but also be a method to defend the electromagnetic pulse damage effectively.

4. Conclusion

For the $n^+ - p - n^+$ bipolar transistor, the damage mechanism induced by EMP is mainly CSB. The emitter injection is a necessary condition for the device occurring CSB. R_b and V_{be} can accelerate the device reaching the condition and make the device damage easily. R_e can reduce the magnitude of the

pulse voltage on the device and significantly improve the durability of the device against EMP. Therefore, it is believed that the external component of the device can change the speed of the EMP-resulted damage.

The damage effect of the device in circuit under EMP is very complicated in nature. To understand the influence of basic components in the typical position of the bipolar transistor, this paper analyses the connection of three kinds of electronic components on the damage effect of the circuit under EMP on the collector of the device. In practice, however, every ports of the device may be the EMP injecting ports. For the emitter injected EMP, Reference [8] analyzes the influence of the external components from the current distribution relationship of the device. For the base injected EMP, the device will not appear CSB, which damage mechanism still needs further studies. At the same time, the research of the circuit should consider parasitic effects among the electronic components to make it closer to the actual situation because the entire circuit is integrated on a chip in practice.

References

- [1] Yu W, Cai X H, Huang W H, et al. The current-mode destroy of semiconductor devices by electromagnetic pulse. *High Power Laser and Particle Beams*, 1999, 13(3): 355
- [2] Zhou Huaian, Du Zhengwei, Gong Ke. Transient response of bipolar junction transistor under intense electromagnetic pulse. *High Power Laser and Particle Beams*, 2005, 17(12): 1861
- [3] Yuan Qingyun, Wu Zhancheng, Yang Jie, et al. Research on effects of ESD and square-wave EMP on microelectronic device. *High Voltage Engineering*, 2006, 32(6): 47
- [4] Yang Jie, Liu Shanghe, Yuan Qingyun, et al. Square-wave EMP damage of microwave low-noise silicon transistors. *High Voltage Engineering*, 2007, 33(7): 111
- [5] Wunsch D C, Bell R R. Determination of threshold failure levels of semiconductor diodes and transistors due to pulse voltage. *IEEE Trans Nucl Sci*, 1968, 15(6): 244
- [6] Tasca D M. Pulse power failure modes in semiconductors. *IEEE Trans Nucl Sci*, 1970, 17(6): 364
- [7] Hane K, Mogi M, Suzuki T. Influence of an external resistor on second breakdowns in epitaxial planar transistors. *IEEE Trans Electron Devices*, 1979, 26(2): 157
- [8] Chen Xi, Du Zhengwei, Gong Ke. Influence of circuit during injection of EMP into bipolar junction transistor. *High Power Laser and Particle Beams*, 2007, 19(7): 1197
- [9] Grutchfield H B, Moutoux T J. Current mode second breakdown in epitaxial planar transistors. *IEEE Trans Electron Devices*, 1966, 13(11): 743
- [10] Xi Xiaowen, Chai Changchun, Ren Xingrong, et al. Transient response of bipolar transistor under intense electromagnetic pulse on collector. *Proceedings of the 16th IEEE International Symposium on the Physical and Failure Analysis of integrated Circuits*, 2009: 443