4 GHz bit-stream adder based on ΣΔ modulation*

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Abstract: The conventional circuit model of a bit-stream adder based on sigma delta (ΣΔ) modulation is improved with pipeline technology to make it work correctly at high frequencies. The integrated circuit (IC) of the bit-stream adder is designed with the source coupled logic structure and designed at the transistor level to increase the operating frequency. The IC is fabricated in TSMC's 0.18-μm CMOS process. The chip area is 475×570 μm^2. A fully digital ΣΔ signal generator is designed with a field programmable gate array to test the chip. Experimental results show that the chip meets the function and performance demand of the design, and the chip can work at a frequency of higher than 4 GHz. The noise performance of the adder is analyzed and compared with both theory and experimental results.

Key words: bit-stream; adder; sigma delta; digital signal generator
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1. Introduction

The method of traditional digital signal processing (DSP) is to convert the analog signal to a multi-bit digital signal, and then to process it. All of the transmissions go through the multi-bit bus. In the high speed signal processing area, the difference between the delay time, coupling and electromagnetic interference of different lines cause problems for the performance of the system. These problems influence the stability and limit the operating frequency. Moreover, the structures of multi-bit digital signal processing units are complicated, and multi-bit signal lines occupy a large area for routing.

These problems are obvious in large scale DSP cases. A notable example is the hardware implementation of an artificial neural network (ANN)[1]. An ANN consists of some DSP units, including adders, multipliers and activation function units. The total number of the DSP units and the mutual connections of an ANN are very large. Researchers have found that it is almost impossible to realize a biggish ANN with the traditional multi-bit DSP method. The reason for this is that the circuit scale is too large. The hardware implemented ANN reported in the literature only has several neurons[2]. It obstructs the hardware implementation of a general ANN.

Recently, a new DSP method appears to solve these problems. This method processes a bit-stream digital signal which comes from a ΣΔ modulator[3−6]. Since only one line is needed for one signal, the problem of the connection in a large scale signal process array is easy to solve. The adder is a fundamental DSP module. The implementation of the bit-stream adder is an important step in verifying the performance and theory of the novel DSP method and pushing it into application. The implementation and noise analysis of the bit-stream adder and digital ΣΔ signal generator are discussed in this paper.

2. IC design of bit-stream adder

2.1. Source of bit-stream signal

The bit-stream signal comes from the ΣΔ modulator. The ΣΔ modulator is one part of a ΣΔ analog-to-digital converter (ADC). With the techniques of noise shaping and oversampling, the ΣΔ ADC has become quite popular for achieving high resolution.

A ΣΔ ADC has two sections: a ΣΔ modulator and a digital filter. The ΣΔ modulator converts the analog signals to a bit-stream digital signal. Then, the bit-stream signal is transformed into a traditional multi-bit digital signal by using a digital filter. The bit-stream digital signal is just an inner signal in the ΣΔ ADC. However, in some new DSP arithmetic of recent years, the bit-stream signal is directly processed[3−6]. In this arithmetic, the DSP units are very simple and only one bit is used for one signal.

2.2. Model improvement

Both the input and output signals of the bit-stream adder are one-bit ΣΔ modulated signals. The signification of the bit-stream is totally different from the bits in a multi-bit adder. The arithmetic of the bit-stream adder is given in Ref. [3].

The adder performs the following operation for two ΣΔ modulated signals $x(n)$ and $y(n)$ (only +1 or –1 can be taken).

$$Z(n) = \begin{cases} (x(n) + y(n))/2, & x(n) = y(n), \\ q(n), & x(n) \neq y(n), \end{cases} \tag{1}$$

$$q(n) = \begin{cases} q(n-1), & x(n) = y(n), \\ -q(n-1), & x(n) \neq y(n), \end{cases} \tag{2}$$

where sum $Z(n)$ is the output signal of the adder, and $q(n)$ is an inner signal in the adder. The adder always gives the half of the sum. When $x(n) = y(n)$, then $Z(n) = x(n)$, otherwise, $q(n)$ is employed to denote the sum of –1 and +1. A sequence of $q(n)$ means zero when $x(n) \neq y(n)$. In a physical digital circuit, we do not have –1. So, 0 is employed to denote –1. Reference [3] also provides the corresponding circuit of the adder, which is shown in Fig. 1. Compared with a multi-bit adder, such as a 4 bit full adder chip 4560, the bit-stream adder is quite simple.

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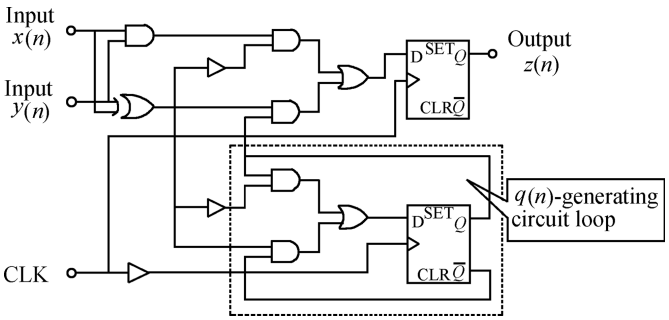

Fig. 1. Equivalent circuit of the conventional bit-stream adder.

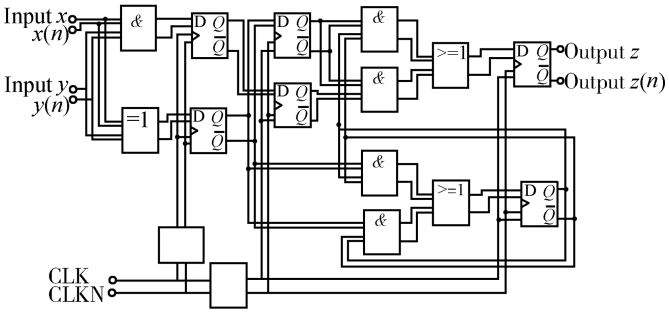

Fig. 2. Structure of the improved bit-stream adder.

Owing to the delay difference between different signal paths, some error codes appear at high operation frequencies when the conventional adder is simulated in Hspice. At the same time, the model simulation in Simulink is perfect. The circuit models in the library of Simulink are ideal models, i.e., no delay time, so the problem is concealed in model simulation. It can be found that the most important delay problem comes from the three-stage $q(n)$-generating circuit loop, which is indicated in Fig. 1.

To solve the problem, pipeline technology is introduced into the bit-stream adder. The signals through different traces have more time to transfer. As a result of the tradeoff between cost and speed, a two-stage pipeline structure is employed. The structure of the improved bit-stream adder is shown in Fig. 2.

2.3. Circuit and layout design

The bit-stream solution based on $\Sigma\Delta$ modulation achieves high resolution, and the bit-stream DSP modules are very simple and robust. At the same time, it has to pay the price of signal bandwidth. A very high clock frequency has to be used to process relatively low bandwidth signals. Increasing the operating frequency of the bit-stream modules will expand its signal bandwidth[4]. The SCL logic style is preferred to other logic families for its higher speed[7]. All the signals in coupled logic structure (SCL) logic should be differential signals. The differential signal lines are denoted in Fig. 2 too. This chip, shown in Fig. 3, is realized in the TSMC 0.18-μm mixed-signal 1P6M SALICIDE CMOS process. The terminals and components of the adder are indicated in Fig. 3.

2.4. Noise analysis

The total noise estimation equation of the adder is given in Ref. [3]. The estimated noise has two components. The first

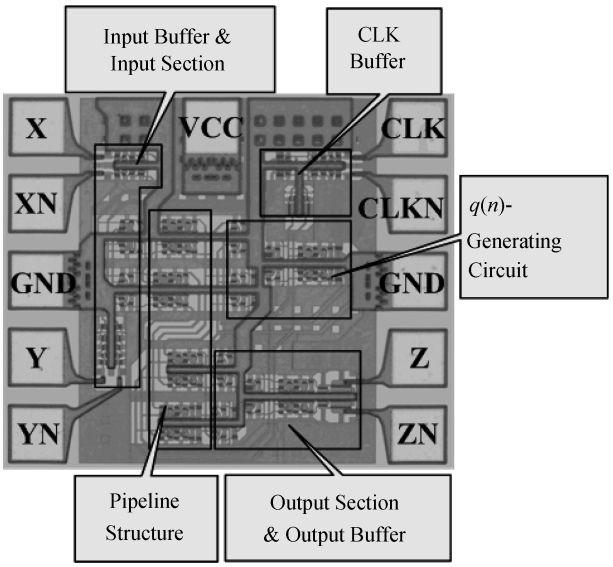

Fig. 3. Chip photograph.

Table 1. SNR of the input and output signals of the bit-stream adder.

Signal	SNR (dB)	
	1 MHz	500 kHz
Input (300 kHz)	28.05	35.83
Input (500 kHz)	23.95	30.29
Input average	26.0	33.06
Output signal	25.97	33.01

one is the modulation quantization noise, $e_x(n)$ and $e_y(n)$, which consists in the $\Sigma\Delta$ modulated signals $x(n)$ and $y(n)$. The power spectrum density (PSD) of the $e_x(n)$ or $e_y(n)$ is

$$E(\omega) = 2\frac{\Delta}{\sqrt{12}}\sqrt{\frac{2}{f_s}}\sin\frac{\omega}{2f_s}, \tag{3}$$

where Δ is the quantization spacing, and f_s is the sampling frequency.

Another noise source generated by the action of $q(n)$. The PSD of $e_q(n)$ is presented as follows:

$$R(\omega) = r(0) + 2\sum_{m=1}^{\infty} r(m)\cos\frac{\omega m}{f_s}. \tag{4}$$

The total noise $P_z(\omega)$ in the output signal is computed by summing $E(\omega)$ and $R(\omega)$.

$$P_z(\omega) = R(\omega) + |E(\omega)|^2/2. \tag{5}$$

Actually, the noise estimated from the theory analytical method is larger than the result in circuit simulation. Also, the test results of the adder IC we implemented shows that most of the noise of the output signal of the bit-stream adder comes from the quantization noise of the input signals, $e_x(n)$ and $e_y(n)$. Details of the data are shown in Table 1.

3. Digital sigma delta signal generator

To verify the function and performance of the adder, a generator, based on a field programmable gate array (FPGA)

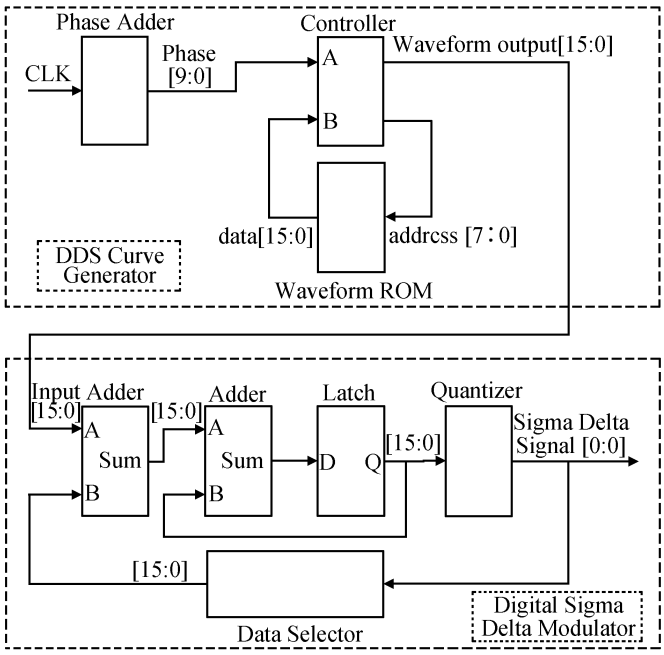

Fig. 4. Block diagram of ΣΔ signal generator.

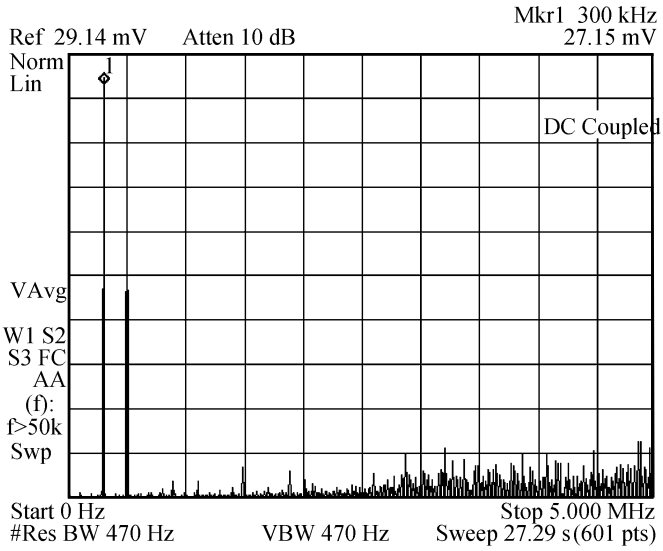

Fig. 5. Output frequency spectrum of the improved adder.

evaluation board, is developed to generate the desired ΣΔ signals.

The generator is composed of two sections: the first section acts as a direct digital synthesizer (DDS) curve generator to provide a multi-bit digital sine wave, and the second section acts as a digital ΣΔ modulator to convert the multi-bit digital sine wave signal to a single bit ΣΔ signal.

Figure 4 shows a block diagram of the FPGA ΣΔ signal generator; the upper part is the DDS curve generator, and the lower part is the digital ΣΔ modulator. Normally, the input of the ΣΔ modulator is an analog signal. However, we do not have an appropriate ΣΔ modulator in hand for the test. So, a new type fully digital ΣΔ modulator is designed with FPGA to build a ΣΔ signal generator. In this generator, the analog signal is replaced with a multi-bit digital signal, and the digital signal is denoted as a complement code to convert the subtracting operation to an addition operation.

4. Experimental results

Two ΣΔ signals with frequencies of 300 kHz and 500 kHz are generated by the digital ΣΔ signal generator and applied to the adder IC. Figure 5 shows the frequency spectrum of the output signal of the adder. The figure denotes that the output signal has both the components of two input signals and the distinct characteristic of noise shaping.

The signal-to-noise ratio (SNR) of the input and output signals of the bit-stream adder can be obtained by calculating the test data. These data are collected by a spectrum analyzer, Agilent E4440. Because the clock frequency of the employed FPGA is 50 MHz, 1 MHz or 500 kHz are chosen as the signal bandwidth of the baseband, so the oversampling ratio is set to 25 or 50.

Table 1 shows that the SNR of the output signal is a little lower than the SNR of the average of the input signals. This means that the adder only brings very little noise to the output signal.

The result also indicates that the action of $q(n)$ does not generate as much noise as the equation given in Ref. [3]. The reasons for this are that the system of the bit-stream adder is treated as a linear system and the quantization noise is analyzed as white noise by the analysis theory used in Ref. [3]. Actually, the system of the bit-stream adder is a nonlinear system. We do not have an appropriate theory to analyze the nonlinear system now. So, we have to use a linear model. Otherwise, Gray[8] indicates that the quantization noise is not real white noise in the low order ΣΔ modulator case. Thus, the theory analysis result should be checked in practice.

As the result of the digital ΣΔ modulator being only a one order ΣΔ modulator, the oversampling ratio is not very high and the DDS curve generator has inherent phase-truncation and amplitude-truncation noise, the SNR of the signal generated by the digital ΣΔ modulator is not perfect. But the digital ΣΔ signal generator provides a convenient method to check the performance of the bit-stream adder.

The tested frequency spectrum and SNR of the chip show that the function of the adder is correct and it can retain the characteristics of ΣΔ modulation, that is, noise shaping and high resolution.

Although the clock frequency (50 MHz) of the FPGA limits the highest frequency of the ΣΔ signal for testing, we can verify the logic function at a higher frequency to explore the margin of the adder.

Two periodic square waves are supplied to the adder, and the period of one signal is double the other. The clock frequency is set to 4 GHz. Figure 6 shows the output signal of the adder. The test waveform completely matches the theoretic result of the model. When $x(n) = y(n)$, then $Z(n) = x(n)$, otherwise, every two clocks bring one pulse to the $Z(n)$ terminal. This means that the adder can work at a frequency of higher than 4 GHz and the circuits in the three-stage $q(n)$-generating loop can work at about 12 GHz.

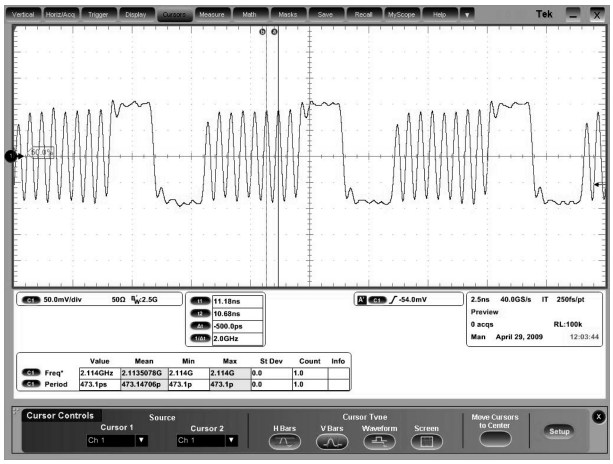

Fig. 6. Test waveform.

5. Conclusion

The conventional bit-stream adder circuit is improved with pipeline technology and designed with SCL structure to make it work properly at higher frequencies. A fully digital FPGA $\Sigma\Delta$ signal generator is designed to check the performance of the adder. It also provides a convenient way to verify the other bit-stream DSP units in further research. Experimental results show the function and performance of the adder chip meet the demand of the design and the chip can work at 4 GHz. The original noise theory is verified by the actual SNR data of the adder.

As a new DSP method, almost all the research is still at the model simulation stage. To the authors' knowledge, this is the first time that a bit-stream adder IC has been implemented and its performance verified. The design and layout of the bit-stream adder can be used in further applications as an intellectual property (IP) core. It can be used in a lot of DSP solutions, especially in ANN.

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