A fully integrated UHF RFID reader SoC for handheld applications in the 0.18 μm CMOS process*

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Abstract: A low cost fully integrated single-chip UHF radio frequency identification (RFID) reader SoC for short distance handheld applications is presented. The SoC integrates all building blocks—including an RF transceiver, a PLL frequency synthesizer, a digital baseband and an MCU—in a 0.18 μm CMOS process. A high-linearity RX front-end is designed to handle the large self-interferer. A class-E power amplifier with high power efficiency is also integrated to fulfill the function of a UHF passive RFID reader. The measured maximum output power of the transmitter is 20.28 dBm and the measured receiver sensitivity is –60 dBm. The digital baseband including MCU core consumes 3.91 mW with a clock of 10 MHz and the analog part including power amplifier consumes 368.4 mW. The chip has a die area of 5.1×3.8 mm^2 including pads.

Key words: UHF RFID; reader; single chip; transceiver; system on chip
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1. Introduction

The idea of the reflected-power communication method which is the basis of RFID (radio frequency identification) was first conceived in 1948 by Stockman[1]. RFID has increasingly received considerable attention worldwide recently. Today it is finding its way into industrial sectors ranging from retail for tracking inventory to manufacturing for tracking product status to airlines for finding lost baggage. RFID has numerous advantages over the traditional bar code, such as the capability of programmability, possibility of multiple tag identification, unlimited storage capacity, out-of-sight operation distance, and high data throughput[2]. Different frequencies can be used in RFID systems. The RFID systems operating in low frequency (LF) and high frequency (HF) are limited in their data rates and operating range. Due to the demand for higher data rate, longer read range and smaller antenna size, technology using passive RFID tags operating in the 860–960 MHz UHF band is gaining worldwide momentum[3]. Currently many different UHF RFID stationary readers are available in the market to meet different demands. Mobile and handheld readers operating in the UHF band are also being developed to meet the requirements of different applications such as pharmaceuticals where doctors can carry such readers on their belts. The market for mobile or handheld readers is increasing rapidly at the moment, much faster than that for stationary readers.

The requirements for handheld readers are very different from those for stationary readers. The key goal in the design of handheld readers is low power consumption to get a longer battery life and low cost for integration in cheap handheld equipment, while the first goal in the design of stationary readers is high sensitivity to operate over a longer range. All the building blocks including power amplifier and protocol processor should be integrated to make the work of high level design easier for handheld readers due to the limited processing capability of handheld equipment.

In this paper, a fully integrated single-chip UHF radio frequency identification (RFID) reader SoC for short distance handheld applications in the 0.18 μm CMOS process is reported. The significant improvement of the reader in this paper is the integration of a high efficiency power amplifier (PA) with satisfactory output power and all the building blocks including a low power MCU and a protocol process module to meet the requirements of handheld applications. The system specifications for the UHF RFID reader and architectures choices are discussed. Circuit design consideration and implementations are also shown.

2. System design

A typical UHF RFID system consists of a reader and several passive tags (Fig. 1). The communication between the reader and the tags is half duplex, and the forward data transfer utilizes the ASK modulation scheme while the return data transfer utilizes the back-scattered modulation scheme[4]. This leads to a carrier-wave leakage problem. Compared with the

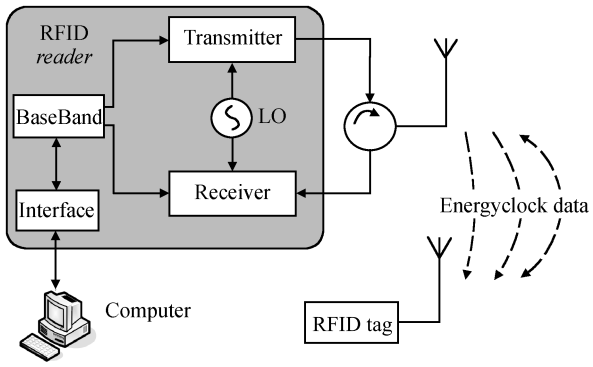

Fig. 1. RFID system.

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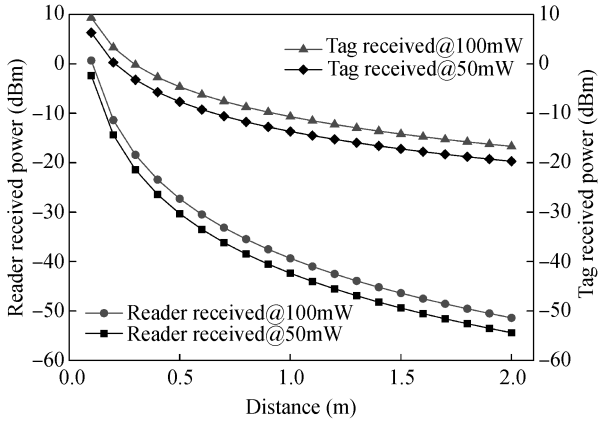

Fig. 2. Power received by the tag and power received by the reader versus distance between the reader and tag.

backscattered signal, the carrier-wave leakage is huge, but it is almost unchanged. The leakage level is mainly decided by the isolation between the transmitter and receiver. Although the carrier-wave leakage and the back-scattered signal from tags are in the same frequency, the carrier-wave is unchanged and the back-scattered signal is modulated. Then the carrier-wave leakage can be converted to DC by direct-conversion and filtered out by a DC offset cancellation circuit. So it is very convenient for the reader to use I/Q direct-conversion architecture in the receiver to get high integration, low power consumption and to avoid a blind zone in the reader, and meanwhile to utilize the ASK modulation scheme for forward data transfer to meet the non-coherent demodulation method of the tags[5]. PA should be integrated on chip for convenient use in handheld devices. Considering the cost of the chip and the battery lifetime, OOK modulators and a high-efficient non-linear PA can be used in the transmitter chain. An MCU with protocol processing ability should also be integrated to release the requirements of high level design.

Next the sensitivity and transmitted power requirements of the handheld UHF RFID reader will be discussed from the system point of view. We can determine the receiver sensitivity which is related to the effective range of the RFID system, which is around 50 cm for short range handheld applications. The power received by the tag and the power of the backscattered signal modulated by the tag (ASK modulation) and received by the reader can be calculated as[2]:

$$P_{\text{tagReceived}} = \frac{P_{\text{reader}} G_{\text{reader}} G_{\text{tag}} \lambda^2}{(4\pi R)^2}, \tag{1}$$

$$P_{\text{back}} = \frac{P_{\text{reader}} G_{\text{reader}}^2 \lambda^2 \Delta\sigma}{(4\pi)^3 R^4}, \tag{2}$$

where R is the distance between the reader and tag, P_{reader} is the transmitted power to the reader antenna, G_{reader} is the antenna gain of the reader, G_{tag} is the antenna gain of the tag, and λ is the wave length of the carrier wave whose frequency is 915 MHz here. $\Delta\sigma$ is the differential radar cross-section of the tag determined by the two modulating states of chip input impedance which is no less than 0.005 m^2required in Ref. [9], then the minimum gain of the tag antenna is around –2 dB. Due to the antenna size limitation of handheld equipment, the antenna gain usually is about 3 dB. Assuming the antenna is perfectly matched at 915 MHz, Figure 2 shows the power received by the reader and power received by the tag versus the distance between the reader and the tag at different transmitted powers.

It can be concluded that a sensitivity of –55 dBm and an output power of 50 mW for the reader can work at a distance of more than 2 m from the tag without considering the power limits of the tag. That is enough for handheld applications. But the communication range limitation of the RFID system is mainly the power consumption of the tag[6]. The power consumption of the tags reported recently ranges from –10.9[7] to –18 dBm[8], and this value is usually greater than –13 dBm for commercial EPC tags. So 100 mW output power is required to meet the requirements of different tags. Thus the sensitivity of the reader for handheld applications should be no worse than –55 dBm and the transmitted power had better be greater than 20 dBm.

The presented reader SoC architecture is shown in Fig. 3. It consists of all the building blocks including frequency synthesizer, I/Q direct-conversion mixer, operational amplifier, comparator, OOK modulator, power amplifier in the transceiver front-end and an MCU with a protocol process module in the baseband. The DC offset cancellation is realized by an off-chip capacitor. The transceiver does not use LNA in the receiver. This is because the target sensitivity is not very high and it is good to avoid the LNA saturation problem induced by carrier leakage in the RFID system. The protocol processing module is designed to deal with different protocols such as ISO/IEC 18000-6 type A, type B and type C[9]. The protocol processing module can be fully accessed by the MCU integrated through the address bus and data bus of the MCU.

3. Circuit implementation

3.1. Frequency synthesizer

The carrier frequency is generated by an integer-PLL with a divide-by-8/9 circuit to meet the frequency resolution of different local regulations as depicted in Fig. 3. The output frequency can be calculated by $f_{\text{out}} = (M/N) f_{\text{ref}}$, where M is the division ratio of the programmable divider and N is the division ratio of the prescaler. M is equal to $N_1 \times 8 + N_2$. N_1, N_2 and N can be changed by the integrated MCU through refreshing specified registers. The synthesizer is designed for the UHF RFID band in China, which has 250 kHz channel spacing. The channel spacing can be changed by rewrite prescaler N. The frequency synthesizer integrates a voltage-controlled oscillator (VCO), a phase frequency detector (PFD), a charge pump, a high-frequency dual-modulus divider, and a digital programmable divider. A 1.8 GHz LO signal is generated by the integrated VCO and then 900 MHz differential I/Q LO signals are obtained by a divide-by-two circuit to avoid VCO pulling.

To meet the phase-noise requirement, an LC VCO (Fig. 4) was designed with the following characteristics.

(1) A long-channel pMOS transistor tail current source is used to reduce the $1/f$ noise.

(2) Cross-coupled pMOS with a symmetric inductor using thick top-layer metal transistors are added to improve the symmetry of the differential output for better close-in phase-noise

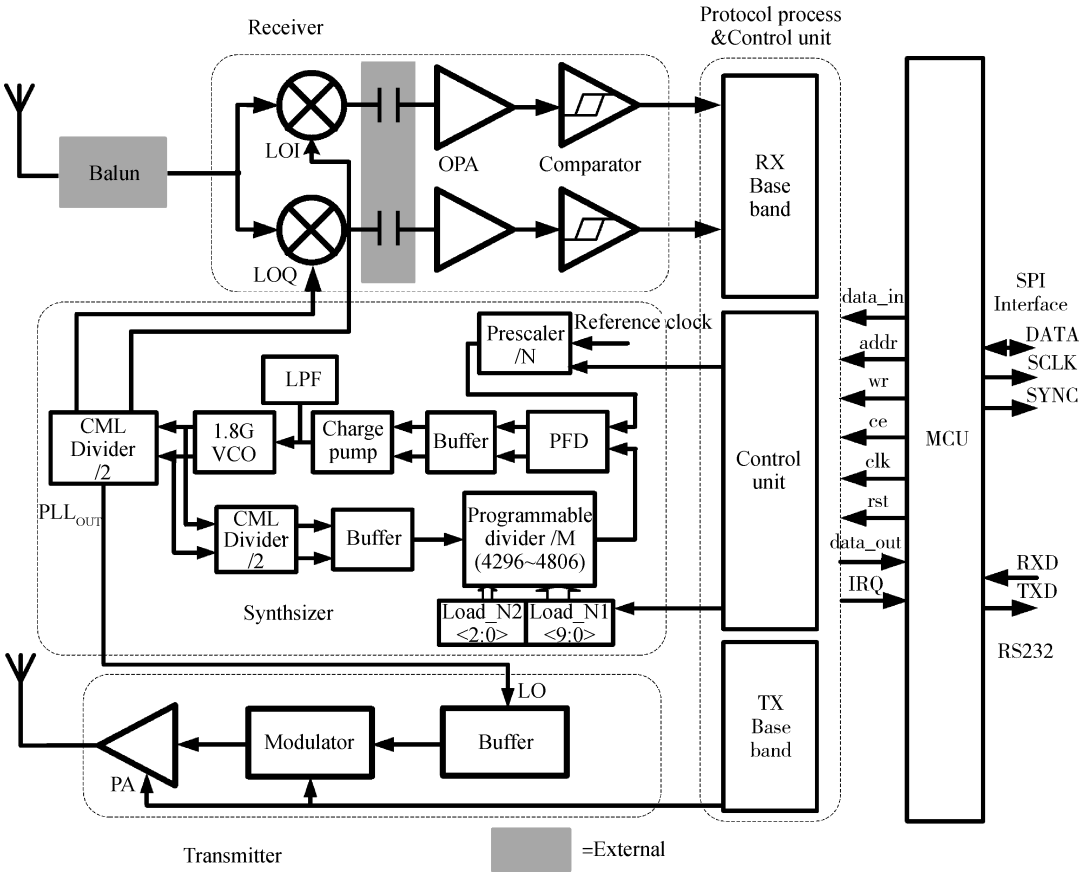

Fig. 3. Block diagram of the presented RFID reader SoC.

performance[10].

(3) Coarse frequency tuning is performed using a bank of three switched capacitors and fine frequency tuning with a varactor. Separate and dedicated VCO and reference supplies are used to further decouple the supply noise from other on-chip blocks. In addition, this block is surrounded by a guard ring to mitigate substrate noise coupling.

3.2. ASK modulator and power amplifier

The transmitter front-end is composed of an OOK modulator and a two-stage class-E power amplifier. The direct-conversion architecture minimizes the off-chip components and provides a low-cost, high-efficient solution. The modulator (Fig. 5) controls the RF signal to the PA to generate the amplitude modulation wave. In order to obtain different RF output signals, two series of resistors are connected to the source node of a source follower. Meanwhile, two switch transistors are followed in the RF signal path, respectively. The gates of the switch transistors are controlled by the transmitted OOK data, fulfilling the different modulations of RF signal by different ratios of R_1 and R_2. Both R_1 and R_2 are implemented on chip to generate a default modulation depth. Also, an off-chip resistor can be connected in shunt with R_2 to adjust the modulation depth to satisfy the different requirements of various tags.

A high efficiency non-linear PA is chosen to reduce the power consumption. Among all the switched-mode power amplifier modes, class-E is the most attractive candidate in term of circuit simplicity and high frequency performance. Figure 6 shows a schematic of the presented 2-stage class-E PA. The first stage works in class-AB mode and the second stage works

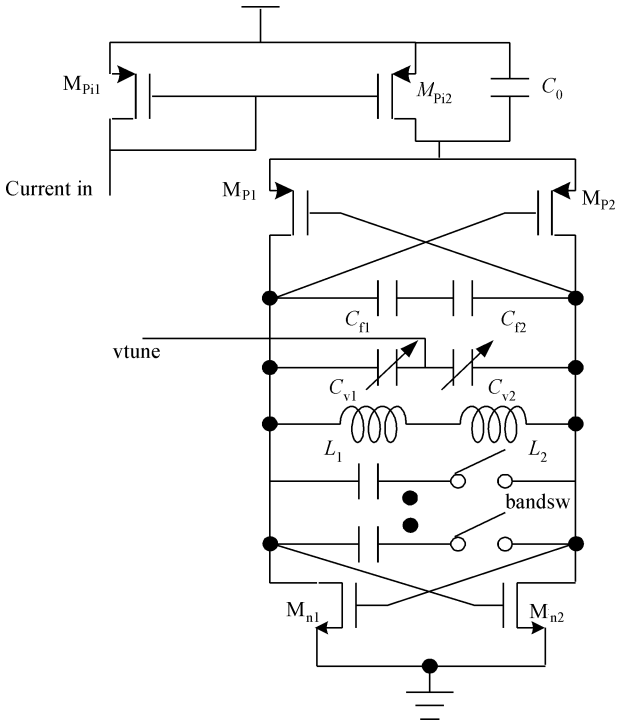

Fig. 4. VCO schematic.

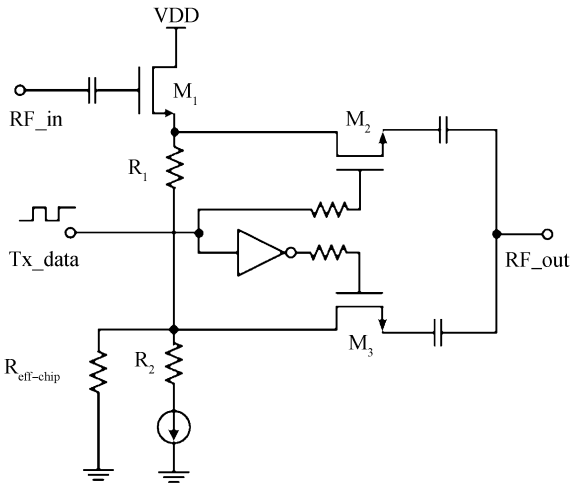

Fig. 5. Schematic of the modulator.

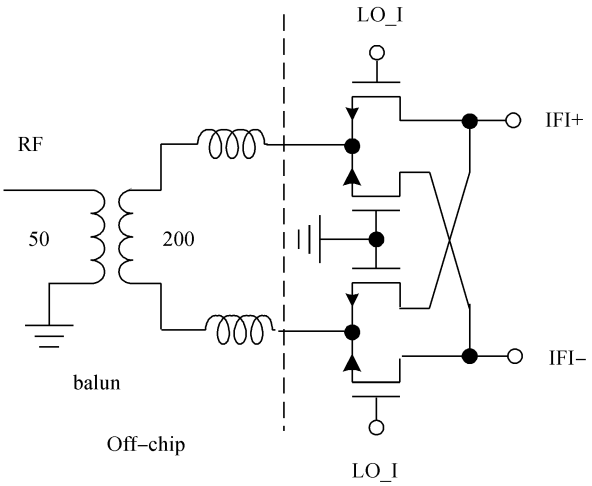

Fig. 7. Schematic of the down–conversion mixer.

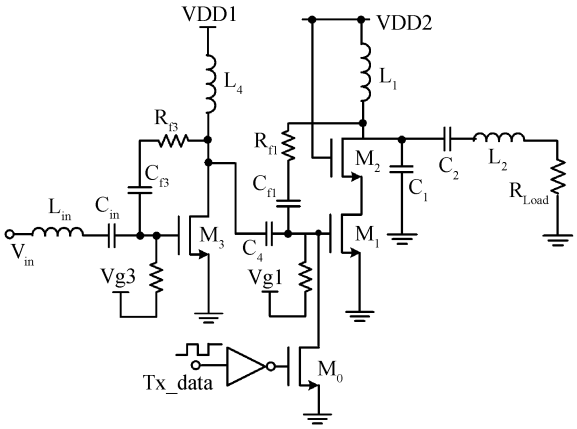

Fig. 6. Schematic of the class-E PA.

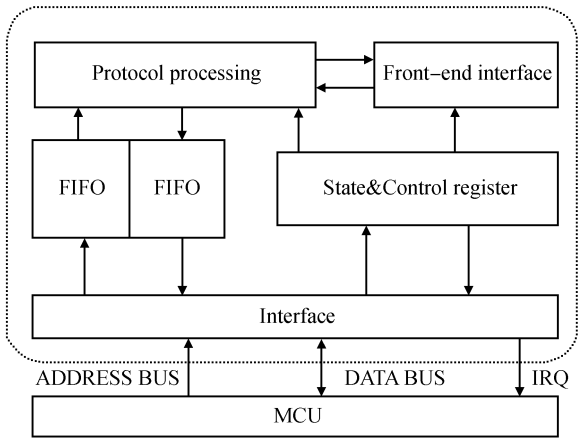

Fig. 8. Digital baseband architecture.

in class-E mode. Each stage has about 11 dB power gain. Note that the second stage can be shut down by a control signal through M_0. The power transistors are put in deep N-well to release the substrate noise coupling impact to other parts.

3.3. Down-conversion mixer and IF circuits

As the first stage of the receiver, the linearity of the mixer should be high enough to deal with the large LO leakage in the passive RFID reader. A passive differential mixer is used due to its high linearity (Fig. 7). An off-chip balun is employed to realize the single-ended to differential transform. The balun employed provides 6 dB voltage gain because its unbalanced impedance is 50 Ω while its balanced impedance is 200 Ω. The voltage gain of the off-chip matching network not only compensates the $2/\pi$ voltage attenuation caused by the switch of the passive mixer, but also provides the receiver with some voltage gain to improve the noise performance.

The output signals of the RF front-end are coupled to the input of the IF amplifiers through capacitances of about 100 nF. A 40 dB gain, 2 MHz bandwidth OPA is designed as an IF amplifier. The OPA is designed using cascaded architecture to get high voltage gain and low power consumption. All the bias voltages are obtained by resisters in series on chip. A hysteretic structure comparator is chosen to avoid the noise interference. A buffer stage is also added at the end of the circuit to increase the output drive capability. To deal with the DC drift in the receiver, one input of the comparator is obtained directly from the OPA output while the other is a low-pass filtered signal of the OPA output. The corner of the low-pass filter is carefully designed to achieve the best sensitivity.

3.4. Digital baseband

The digital baseband (as shown in Fig. 8) is designed based on a DW8051 IP core with stronger performance than the traditional 8051 processor[11]. The associated protocol processing module is designed coincident with the requirement of the MCU data bus and address bus. The associated protocol processing module mainly deals with the decoding and encoding task which has strict timing requirements. The module can generate a timing signal or decode backscattered signal with different rates and encoding methods under the control of the MCU through control registers. The firmware running in the MCU core mainly deals with protocol flow control just like anti-collision arithmetic realization.

Table 1. Summary of the reader SoC performance.

	Parameter	Conditions	Measured results
Transmitter	Output power	Masimun	20.28 dBm
	Power consumption	1.8 V for modulator and driver stage 2.95 V for output stage	332.74 mW
PLL+ receiver	ICP		5 dBm
	Sensitivity	40 kHz data rate	–60 dBm
	Frequency range	$f_{\text{ref}} = 13$ MHz	760–1005 MHz
	Power consumption	1.8 V	35.6 mW
Digital part with MCU	Power consumption	CLK = 10 MHz 1.8 V for core without I/O	3.91 μW

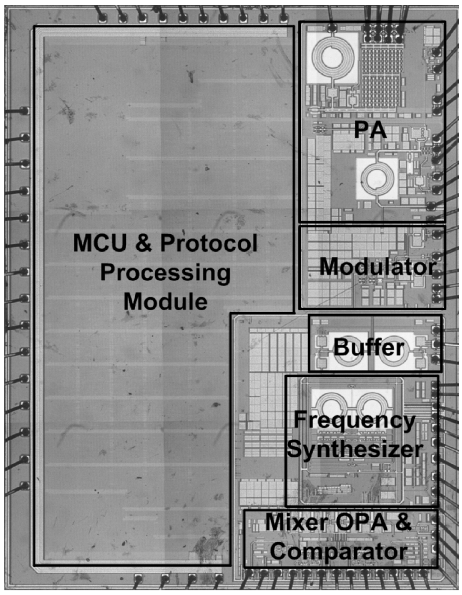

Fig. 9. Die photo of the proposed reader Soc.

Fig. 10. Die photo of the proposed reader Soc.

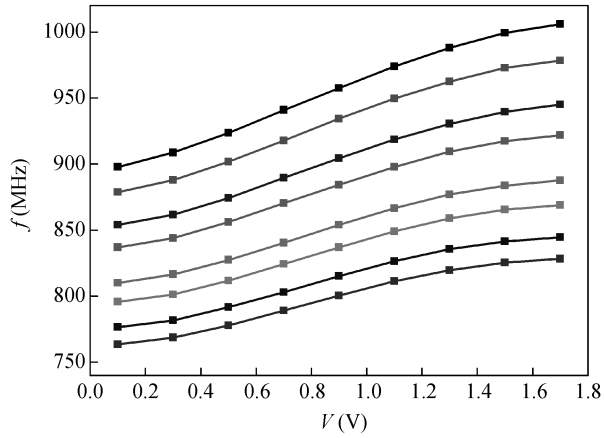

Fig. 11. Measured VCO tuning curve after divider.

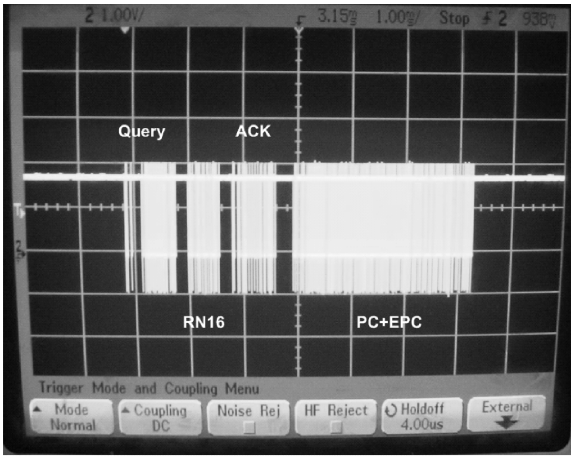

Fig. 12. Communication procedure between the proposed reader and tags.

4. Measurement results

The RFID reader SoC was fabricated using a 0.18 μm CMOS process. The chip microphotograph is shown in Fig. 9 with a die area of 5.1 × 3.8 mm^2 including pads. The IC was packaged in a 9 × 9 mm body 64-lead QFN package with excellent thermal properties and RF grounding (Fig. 10). The IC performance was evaluated on an FR-4 test board. To get the sensitivity, we set output of the PLL at a fixed frequency and connect the RF input of the IC to a signal generator which has a 40 kHz difference in frequency from that of the PLL. When the output power of the signal generator is –60 dBm, the signal can still be demodulated at the output of the IC. So the sensitivity of the IC can achieve –60 dBm @ 40 kbps. The reader performance is summarized in Table 1. The measured VCO tuning curve is plotted in Fig. 11. The 8 bands cover frequencies from 760 to 1005 MHz which can cover the whole passive UHF RFID band in the world. A load tuner is employed to get the maximum output power of the power amplifier which is 20.28 dBm.

The reader performance is summarized in Table 1.

Figure 12 illuminates the captured communication procedure between the proposed reader and ISO 18000-6 type C tags. The reader first sends the query command. When the tag re-

Table 2. Performance summary of single-chip RFID readers.

Parameter	Ref. [12]	Ref. [13]	Ref. [14]	Ref. [15]	This work
Process (μm)	0.18 SiGe BiCMOS	0.18 CMOS	0.18 CMOS	0.18 CMOS	0.18 CMOS
Integration level	RF+Analog+Digital Baseband	RF+Analog+Baseband modem+MPU+ Memory	RF+Analog+Data Converter	RF+Analog+Digital Baseband	RF+Analog+Baseband modem+MPU+ Memory
PA on chip	Yes	No	No	No	Yes
Rx input R_{1dB} (dBm)	11	8	–8	3.5	5
Sensitivity (dBm)	–95	N/A	–85	–90	–60
Output pwer (mW)	79.4	25.1	10	1096	106.7
Die size (mm^2)	21	23.9	36	18.3	19.38
Total power (mW)	1200	160	540	< 276.4	372.3

ceives the correct command Query, it returns a random number RN16. The reader gets the RN16 and sends an ACK command with the received RN16. After the tag receives the correct acknowledgement, it returns the PC and EPC codes.

Table 2 shows the comparison results between the UHF RFID reader IC presented in this paper and with other recently published works. We can see that the proposed reader achieves a higher power output with limited power consumption. To our knowledge it would be the best choice for handheld UHF RFID reader applications.

5. Conclusion

A single chip UHF passive RFID reader is fabricated in the 0.18 μm CMOS process with a die area of 5.1 $\times$ 3.8 mm^2 including pads. The IC was packaged in a 9 $\times$ 9 mm body 64-lead QFN package with excellent thermal properties and RF grounding. The IC integrates all building blocks—including an RF transceiver, a PLL frequency synthesizer, a digital baseband and an MCU. A high-linearity RX front-end and a low-phase-noise synthesizer are designed to handle the large self-interferer. A class-E power amplifier with high power efficiency is also integrated to fulfill the function of a UHF passive RFID reader. A high power output with low power consumption is achieved by careful analysis of requirements from handheld applications, system-level design and circuit structure optimization. The measured maximum output power of the transmitter is 20.28 dBm and the measured receiver sensitivity is –60 dBm. The digital baseband including MCU core consumes 3.91 mW with a clock of 10 MHz and the analog part including power amplifier consumes 368.4 mW.

References

[1] Stockman H. Communication by means of reflected power communication by means of reflected power. Proc IRE, 1948, 36(10): 1196

[2] Finkenzeller K. RFID handbook. 2nd ed. London , UK: Wiley, 2003

[3] Glidden R, Bockorick C, Cooper S, et al. Design of ultra-low-cost UHF RFID tags for supply chain applications. IEEE Commun, 2004, 42(8): 140

[4] Rao K V. An overview of backscattered radio frequency identification system (RFID). Asia Pacific Microwave Conference, 1999: 746

[5] Wang Jingchao, Chi Baoyong, Sun Xuguang, et al. System design considerations of highly-integrated UHF RFID reader transceiver RF front-end. 9th International Conference on Solid-State and Integrated-Circuit Technology, 2008: 1560

[6] Nikitin P V, Rao K V. Performance limitations of passive UHF RFID systems. IEEE Antennas and Propagation Society International Symposium, 2006: 1011

[7] Nakamoto H, Yamazaki D, Yamamoto T, et al. A passive UHF RF identification CMOS tag IC using ferroelectric RAM in 0.35-μm technology. IEEE J Solid-State Circuits, 2007, 42(1): 101

[8] Karthaus U, Fischer M. Fully integrated passive UHF RFID transponder IC with 16.7 μW minimum RF input power. IEEE J Solid-State Circuits, 2003, 38(10): 1602

[9] ISO/IEC 18000-6. Information technology-Radio frequency identification for item management-Part 6: parameters for air interface communications at 860 MHz to 960 MHz AMENDMENT 1: extension with type C and update of types A and B. ISO/IEC, 2006

[10] Hajimiri A, Lee T H. A general theory of phase noise in electrical oscillators. IEEE J Solid-State Circuits, 1998, 33(2): 179

[11] Synopsys Inc. DesignWare Components DW8051 MacroCell Databook, 2003

[12] Chiu S, Kipnis I, Loyer M, et al. A 900 MHz UHF RFID reader transceiver IC. IEEE J Solid-State Circuits, 2007, 42(12): 2822

[13] Kwon I, Eo Y, Bang H, et al. A single-chip CMOS transceiver for UHF mobile RFID reader. IEEE J Solid-State Circuits, 2008, 43(3): 729

[14] Khannur P B, Chen X, Yan D L, et al. A universal UHF RFID reader IC in 0.18-μm CMOS technology. IEEE J Solid-State Circuits, 2008, 43(5): 1146

[15] Wang W, Lou S, Chui K W, et al. A single-chip UHF RFID reader in 0.18 μm CMOS process. IEEE J Solid-State Circuits, 2008, 43(8): 1741