Ultra high-speed InP/InGaAs SHBTs with f_t and f_{max} of 185 GHz *

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Abstract: An InP/InGaAs single heterojunction bipolar transistor (SHBT) with high maximum oscillation frequency (f_{max}) and high cutoff frequency (f_t) is reported. Efforts have been made to maximize f_{max} and f_t simultaneously including optimizing the epitaxial structure, base–collector mesa over-etching and base surface preparation. The measured f_t and f_{max} both reached 185 GHz with an emitter size of $1 \times 20\ \mu m^2$, which is the highest f_{max} for SHBTs in mainland China. The device is suitable for ultra-high speed digital circuits and low power analog applications.

Key words: InP; single heterojunction bipolar transistor; maximum oscillation frequency
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1. Introduction

InP/InGaAs based single heterojunction bipolar transistors (SHBTs) with inherent material advantages provide a promising solution to ultra-high-speed digital circuits and optoelectronic communication ICs. Compared with InP based double heterojunction bipolar transistors (DHBTs), SHBTs with InGaAs collectors are more suitable for digital and low-power analog applications. First, the electron mobility in InGaAs is much higher than InP at low field. Second, the higher velocity allows SHBTs to have a lower doping density in the collector which contributes to the lower base–collector capacitance[1]. In digital circuit design, the base–collector capacitance is critical to the total propagation delay. Lower capacitance makes SHBTs competitive in high speed digital applications.

In characterizing the high frequency performance of transistors, two key factors are widely used: cutoff frequency (f_t) and maximum oscillation frequency (f_{max}). In terms of high speed digital circuit design, both of them should be high in order to minimize total propagation delay. A simplified figure-of-merit (FOM) for bipolar junction transistors can be given by Eq. (1) as a factor to evaluate the devices' capability for high speed digital operations[2].

$$\mathrm{FOM} = 2\left(\frac{1}{f_t} + \frac{1}{f_{max}}\right)^{-1}. \quad (1)$$

In our previous work, InP/InGaAs SHBTs with ultra-high cutoff frequency performance were reported. In Ref. [3], the measured f_t reached 210 GHz and f_{max} reached 56 GHz. In Ref. [4], SHBTs with f_t of 238 GHz and f_{max} of 67 GHz were fabricated successfully. Although a satisfactory f_t was achieved, f_{max} was relatively low in previous works, limiting their usage in circuit design. This is because f_{max} is strongly dependent on the parasitics, such as base contact resistance and base–collector capacitance. A high f_{max} requires mature processing control to reduce the parasitics[5].

In this paper, efforts have been made to maximize f_t and f_{max} simultaneously. Epitaxial structure is optimized first. Careful base surface preparation is carried out to minimize base contact resistance. Base–collector over-etching technology developed in Ref. [4] is applied to reduce the base–collector junction area. The benzocyclobutene (BCB) passivation and planarization technique is applied to reduce the parasitics.

The measured f_t and f_{max} have both reached 185 GHz indicating good processing control. A high FOM is achieved. The device also shows excellent DC and RF characteristics which are suitable for high speed and low power applications.

2. Epitaxial structure and device fabrication

The epitaxial layer of the HBTs was grown by molecular beam epitaxy on a Fe-doped semi-insulating (100) InP substrate. The layer structure is listed in Fig. 1.

Compared with the structure used in Refs. [3, 4], several

$In_{0.53}Ga_{0.47}As$	150 nm	Si	$1\times10^{19}\ cm^{-3}$
InP	50 nm	Si	$1\times10^{19}\ cm^{-3}$
InP	70 nm	Si	$3\times10^{17}\ cm^{-3}$
$In_{0.53}Ga_{0.47}As$	5 nm	UID	UID
$In_{0.53}Ga_{0.47}As$	50 nm	Be	$3\times10^{19}\ cm^{-3}$
$In_{0.53}Ga_{0.47}As$	300 nm	Si	$1\times10^{16}\ cm^{-3}$
$In_{0.53}Ga_{0.47}As$	50 nm	Si	$1\times10^{19}\ cm^{-3}$
InP	20 nm	Si	$1\times10^{19}\ cm^{-3}$
$In_{0.53}Ga_{0.47}As$	40 nm	Si	$1\times10^{19}\ cm^{-3}$
InP substrate			

Fig. 1. Layer structure for the InP/InGaAs SHBT.

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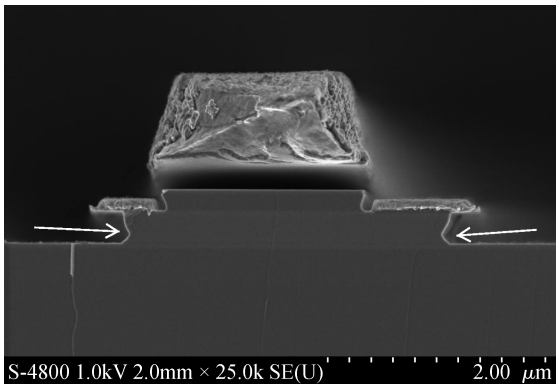

Fig. 2. SEM of the cross section of the device after base–collector etching. The arrow shows the effect of over-etching.

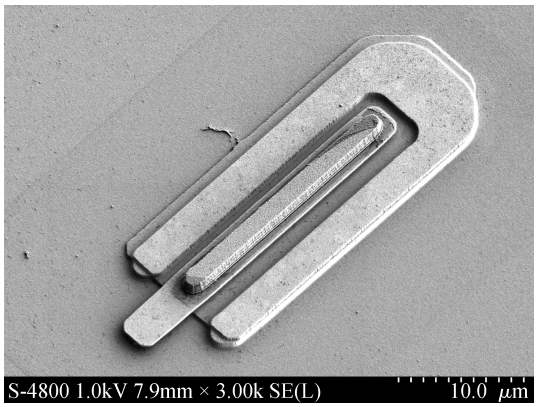

Fig. 3. SEM picture of the fabricated SHBT before BCB planarization.

changes have been made to improve f_{max}. The collector layer is changed from 200 to 300 nm. Therefore the base–collector junction capacitance is reduced at the Kirk point when the collector is in full depletion. The base layer is increased to 50 nm which helps to decrease the base sheet resistance.

The device fabrication follows a standard triple mesa, conventional wet-etch process. First, the InGaAs cap layer was reduced to about 75 nm by wet etching. Then Ti/Pt/Au emitter contact metal was formed by electron-beam evaporation with a width of 1 μm. Emitter etching was carried out using selective wet etching. The InGaAs emitter contact layer and the InP emitter layer were etched by $H_2O_2/H_3PO_4/H_2O$ and $HCl:H_3PO_4$ solutions, respectively. An effective 0.8 μm size emitter was formed by slight emitter undercut. Before depositing the base contact metal, a careful surface preparation procedure was employed. This is because the particular resistivity attained by nonalloyed ohmic contacts has a strong dependence on the procedures used to remove surface oxides[6]. Then a self-aligned Pt/Ti/Pt/Au base metal was evaporated. Base–collector etching was carried out after the emitter was protected by photo-resist. The base–collector region was over-etched in order to have a smaller BC junction capacitance. Figure 2 shows the cross section of the device after base–collector etching.

Then the subcollector was etched for device isolation, and Ti/Pt/Au collector metal was evaporated. Next, a BCB based etch-back process was employed for device passivation and planarization. Compared with polyimide, BCB has several advantages. First, the dielectric constant of BCB is $\varepsilon_r = 2.7$ which is lower than polyimide. This is helpful in reducing parasitics between the pad and the device. Secondly, BCB has a higher resistivity, which helps to minimize leak current. Besides, the planarization effect is better for BCB, which is important considering the multilevel interconnection in large-scale ICs[7]. Figure 3 shows an SEM picture of the fabricated device before BCB planarization.

3. Device measurement result and test

3.1. DC test

The DC characteristics of the HBT were measured with an HP4155A parameter analyzer. Figure 4 shows DC common emitter output characteristics. The emitter size is $1.0 \times 20\ \mu m^2$.

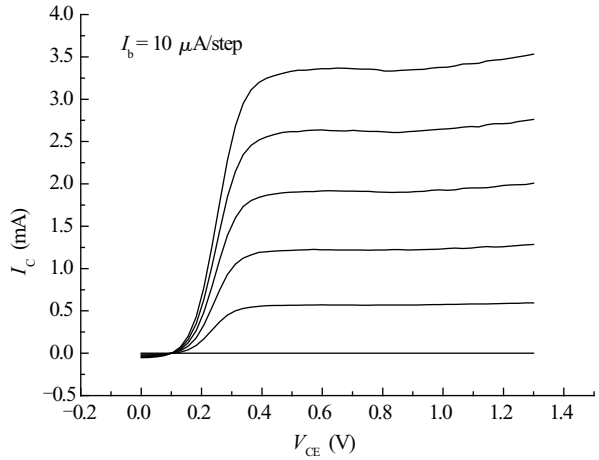

Fig. 4. Common emitter V_{ce}–I_c characteristics of the HBT with a $1 \times 20\ \mu m^2$ emitter.

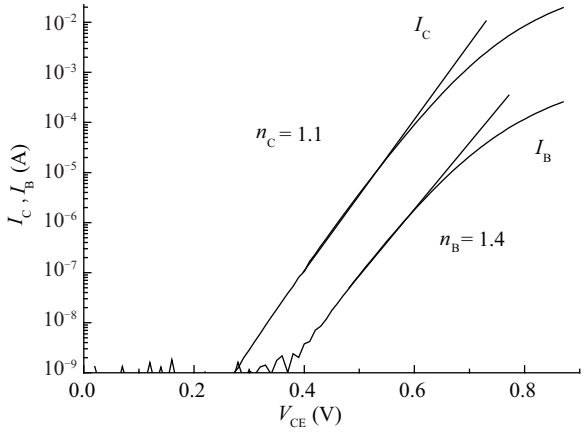

Fig. 5. Typical Gummel plot of the HBT with a $1 \times 20\ \mu m^2$ emitter.

The common emitter DC current gain (β) varies slightly at different collector currents, from 61 at $I_b = 20\ \mu$A to 66 at $I_b = 50\ \mu$A. This indicates that the base surface recombination current is small due to good surface preparation. The device exhibits a common emitter breakdown voltage (BV_{CEO}) of 4.5 V and a collector–emitter offset voltage (V_{OS}) of 0.1 V. A typical Gummel plot is given in Fig. 5, which shows ideality factors of 1.1 and 1.4 for I_c and I_b, respectively.

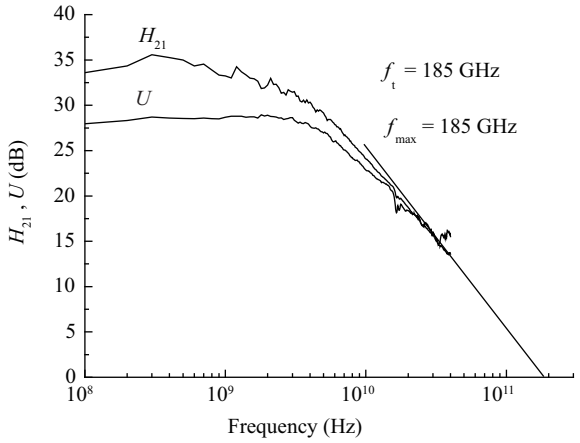

Fig. 6. High frequency performance of the HBT with a 1 × 20 μm^2 emitter.

3.2. RF test

The small signal S parameters of the InP/InGaAs SHBT were measured on-wafer using an HP8510C network analyzer over a frequency range from 100 MHz to 40 GHz. The RF calibration was achieved using short-open-load-through calibration. Figure 6 shows the current gain (H_{21}) and Mason's unilateral power gain (U). The f_t and f_{max} were obtained by extrapolating the H_{21} and U curves at a 20 dB decade slope[5]. As shown in Fig. 3, both f_t and f_{max} reached 185 GHz. The maximum f_t and f_{max} were achieved at I_c = 42.51 mA, I_b = 580 A, corresponding to a J_c of 210 kA/cm^2. The RF measurements were carried out under a collector–emitter voltage (V_{CE}) of 1.1 V.

4. Discussion

The value of the maximum oscillation frequency f_{max} can be written as[5]:

$$f_{max} = \sqrt{f_T/8\pi R_b C_{jc}}, \quad (2)$$

where R_b stands for base resistance. Efforts to increase f_{max} include reducing R_b and the BC junction capacitance (C_{jc}) simultaneously. R_b can be divided into three parts as Equation (3) illustrates:

$$R_b = R_{bc} + R_{bi} + R_{bx}, \quad (3)$$

where R_{bc} is base contact resistance, R_{bi} is intrinsic base resistance, and R_{bx} is extrinsic base resistance. Among the three parts, the base contact resistance contributes most to the total base resistance. R_{bc} can be calculated as:

$$R_{bc} = 0.5\left(\sqrt{R_{SHB}\rho_c}/L_E\right) \times \coth\left(W_B\sqrt{R_{SHB}/\rho_c}\right), \quad (4)$$

where R_{SHB} is the sheet resistance of the base region, ρ_c is the specific contact resistance, W_B is the width of base contact metal, and L_E is the length of emitter mesa. In this paper, R_{SHB} and ρ_c were attained by standard transmission line measurements (TLM). The measured R_{SHB} is 1072 Ω/□ and ρ_c is 1.020752 × 10^{-6} Ω·cm^2. From Eq. (4), we can calculate R_{bc} = 11.5 Ω. In Cheng's paper[3], the measured R_{SHB} and ρ_c are 2184 Ω/□ and 2.4 × 10^{-5} Ω·cm^2; the calculated base contact resistance is 76.5 Ω. The decrease of R_{bc} is largely due to a novel base surface preparation process. In this work, the calculated R_{bi} and R_{bx} are 6 Ω and 18 Ω respectively; the total R_b is 35.5 Ω. This paper demonstrates a significant decrease in R_b which consequently results in an improvement of f_{max}.

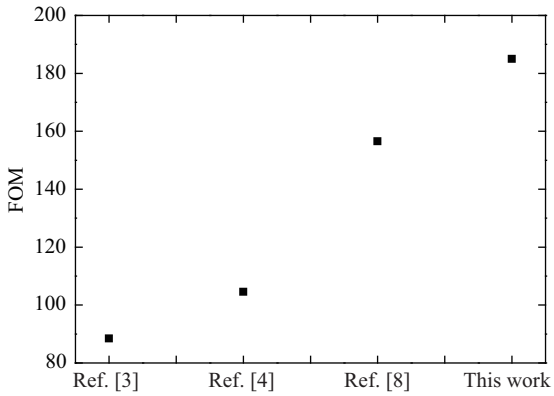

Fig. 7. FOM comparison of reported SHBTs in China in recent years.

According to Eq. (2), a small C_{jc} is also important in pursuit of high f_{max}. In our work, the base–collector region was thus over-etched to minimize base–collector junction capacitance. A simple estimation of C_{jc} can be employed.

$$C_{jc} = A_c\varepsilon_s/X_{dep}, \quad (5)$$

where A_c is the base–collector junction area, and X_{dep} is the base–collector depleting depth. At the Kirk point when the collector region is fully depleted, X_{dep} is equal to the depth of the collector layer. In this paper, the calculated C_{jc} is about 14 fF which is smaller than that in Ref. [3]. This is because a thicker collector is applied. Besides, the effective B–C junction area is reduced due to over-etching technology. The effective B–C junction area is about 2.2 × 20 μm^2 in this work. According to Eq. (2), the calculated f_{max} is 171 GHz, which is close to the extrapolating f_{max} of 185 GHz.

A comparison of reported SHBTs in China in terms of FOM is shown in Fig. 7. This work has demonstrated the highest FOM indicating good performance for high speed digital applications.

5. Conclusion

We report an InP/InGaAs SHBT with conventional triple mesa typology. The f_t and f_{max} reached 185 GHz simultaneously. A high FOM is achieved, indicating that this device is suitable for ultra-high speed digital circuits.

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