A full on-chip CMOS low-dropout voltage regulator with VCCS compensation*

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Abstract: A full on-chip CMOS low-dropout (LDO) voltage regulator with high PSR is presented. Instead of relying on the zero generated by the load capacitor and its equivalent series resistance, the proposed LDO generates a zero by voltage-controlled current sources for stability. The compensating capacitor for the proposed scheme is only 0.18 pF, which is much smaller than the capacitor of the conventional compensation scheme. The full on-chip LDO was fabricated in commercial 0.35 μm CMOS technology. The active chip area of the LDO (including the bandgap voltage reference) is 400 × 270 μm^2. Experimental results show that the PSR of the LDO is –58.7 dB at a frequency of 10 Hz and –20 dB at a frequency of 1 MHz. The proposed LDO is capable of sourcing an output current up to 50 mA.

Key words: voltage regulator; full on-chip; high PSR; VCCS; LDO
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1. Introduction

The demand for system-on-chip (SoC) is increasing significantly nowadays. Full on-chip low-dropout (LDO) voltage regulators[1−3] are therefore highly desirable. LDO regulators provide constant voltage supply to different functional blocks of an SoC. Since LDO regulators have to be integrated on a single chip, two design challenges are brought in. First, LDO is typically utilized to provide a regulated power source for noise-sensitive blocks such as the VCO and charge-pump[4, 5] in a PLL. Since the performance of a PLL can deteriorate because of the fluctuation of the supply voltage, the PSR of the LDO should be improved to reject the ripple coming from the input power supply. Second, the capacitors used in CMOS technology occupy a large chip area. In order to design a full on-chip LDO regulator, the number of compensating capacitors must be minimized.

Different methods have been introduced recently to improve the performance of full on-chip LDO. In Ref. [6], a regulator utilizing damping-factor-control frequency compensation was proposed. The regulator is based on a three stage amplifier. The output voltage of the regulator is 1.5 V. A PSR of –60 dB is achieved by the regulator at low frequency. Three compensating capacitors are included in the proposed regulator. The active chip area is 568 × 541 μm^2. An LDO regulator based on the technique of removing the feed forward path was presented in Ref. [1]. Similarly, the proposed regulator has a three-stage amplifier structure. A 100 pF load capacitor is attached at the output node. Furthermore, the regulator needs two or three additional capacitors for stability, thereby increasing the area overhead significantly. The PSR of the regulator in Ref. [1] is –57 dB at low frequency. The core area of the regulator is 538 × 538 μm^2.

In this paper, an LDO regulator based on a two-stage amplifier is presented, thereby simplifying the compensating circuit drastically. The error amplifier (EA) with the proposed regulator is a folded cascade amplifier. The proposed regulator generates a zero by Voltage - controlled current source (VCCS) which contains only one capacitor of 0.18 pF. The core area of the proposed regulator (including bandgap voltage reference) is 400 × 270 μm^2.

2. Design consideration of the proposed LDO

2.1. Stability of the proposed LDO

The proposed LDO employs the VCCS[7] compensation scheme for stability. Figure 1 shows the LDO voltage regulator topology. Two low-frequency poles have to be taken into consideration when the frequency response of the LDO's loop transfer function is evaluated. A low-frequency pole w_{P1} lies at the output node V_{out}, because a large on-chip capacitor C_1 about 100 pF is attached at the output node V_{out} to attain good transient response. There is another low-frequency pole w_{P2} at the output node N_{EA} of the error amplifier owing to the large

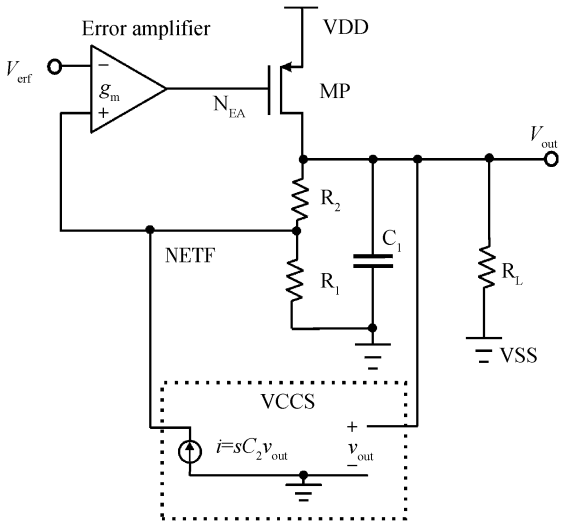

Fig. 1. Proposed LDO voltage regulator topology.

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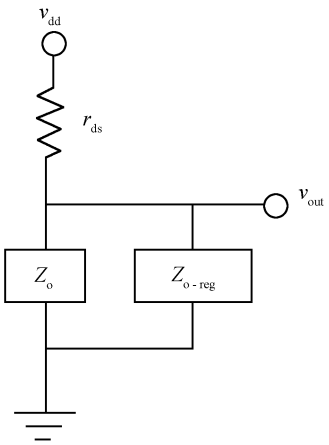


Fig. 2. Model for the PSR transfer function.

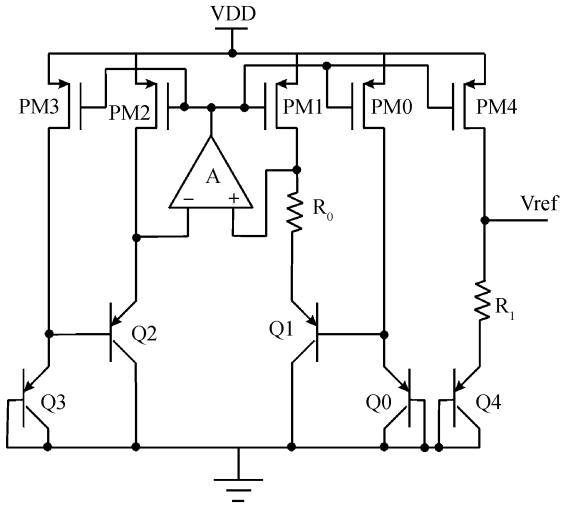


Fig. 3. Bandgap voltage reference circuit.

size of the pass transistor (MP) together with the high output impedance of the error amplifier, which provides a large RC time constant. The distance between the two poles is small, thereby affecting the stability of the regulator. To solve this problem, a zero is introduced by the VCCS scheme to compensate the phase contribution of the pole w_{P1}. (The detailed implementation of VCCS scheme is illustrated in Fig. 4.)

If the internal poles of the error amplifier are ignored, the loop transfer function of the proposed LDO is given by:

$$H(s) \cong \frac{A_0\left(1+\dfrac{s}{w_Z}\right)}{\left(1+\dfrac{s}{w_{P1}}\right)\left(1+\dfrac{s}{w_{P2}}\right)}, \tag{1}$$

where A_0 is the DC loop gain, which is given by:

$$A_0 = g_m R_E g_{mp}[r_{ds}//(R_1+R_2)//R_L]\frac{R_1}{R_1+R_2}, \tag{2}$$

where g_{mp}, r_{ds} are the transconductance and small-signal resistance of pass transistor MP, respectively. R_E is the output resistance of the error amplifier.

The poles and zeros of $H(s)$ can be expressed as:

$$w_{P1} \approx \frac{1}{[r_{ds}//(R_1+R_2)//R_L]\left(C_1 - C_2\dfrac{R_1}{R_1+R_2}\right)}, \tag{3}$$

$$w_{P2} \approx \frac{1}{\left\{C_p + g_{mp}\left[r_{ds}//(R_1+R_2)//R_L\right]C_{gdp}\right\}R_E}, \tag{4}$$

$$w_Z = \frac{1}{R_2 C_2}, \tag{5}$$

where C_p and C_{gdp} are the gate capacitance and gate–drain capacitance of MP, respectively. The VCCS circuit generates a zero w_Z. Therefore, pole-zero cancellation is achieved by w_Z and w_{P1}.

2.2. PSR analysis of LDO

The PSR transfer function can be viewed as the ratio of the impedance between the supply and the LDO output to the impedance between the output and the ground[8] as shown in Fig. 2. Z_O is the open-loop impedance between the output and the ground. $Z_{O\text{-reg}}$ represents the shunting effect of the feedback loop. Therefore, the PSR is given by:

$$\mathrm{PSR} = \frac{v_{out}}{v_{dd}} = \frac{Z_O||Z_{O\text{-reg}}}{r_{ds}+Z_O||Z_{O\text{-reg}}}, \tag{6}$$

where $Z_O = Zc_1 \;||\; (R_1+R_2) \;||\; R_L$, $Z_{O\text{-reg}} = (Z_O \;||\; r_{ds})/\beta A$, β is the feedback factor, and A is the open-loop gain of the proposed LDO regulator.

Therefore, the PSR at low frequency is:

$$\mathrm{PSR}_{dc} \approx \frac{1}{A_{dc}\beta_{dc}}. \tag{7}$$

So the low-frequency PSR of the proposed LDO regulator is improved by enhancing the DC loop gain.

The PSR at moderate frequency can be expressed as:

$$\begin{aligned}\mathrm{PSR}_{f\leqslant \mathrm{UGF}} &\approx \frac{1+\dfrac{s}{\mathrm{BW_A}}}{A_{dc}\beta+1+\dfrac{s}{BW_A}} \\ &\approx \frac{1+\dfrac{s}{\mathrm{BW_A}}}{A_{dc}\beta_{dc}\left(1+\dfrac{s}{w_Z}+\dfrac{s}{A_{dc}\beta_{dc}\mathrm{BW_A}}\right)},\end{aligned} \tag{8}$$

where $\beta_{dc} = R_1/(R_1+R_2)$, $\beta = (1+SC_2R_2)R_1/(R_1+R_2)$, $\mathrm{BW_A}$ is the bandwidth, and A_{dc} is the open-loop DC gain. As predicted by Eq. (8), the zero of VCCS acting as the PSR pole can alleviate the PSR degeneration.

3. Transistor-level design of the proposed LDO

3.1. Bandgap voltage reference

A schematic of the bandgap voltage reference employed for the LDO regulator is shown in Fig. 3. Provided that $I_{PM3} =$

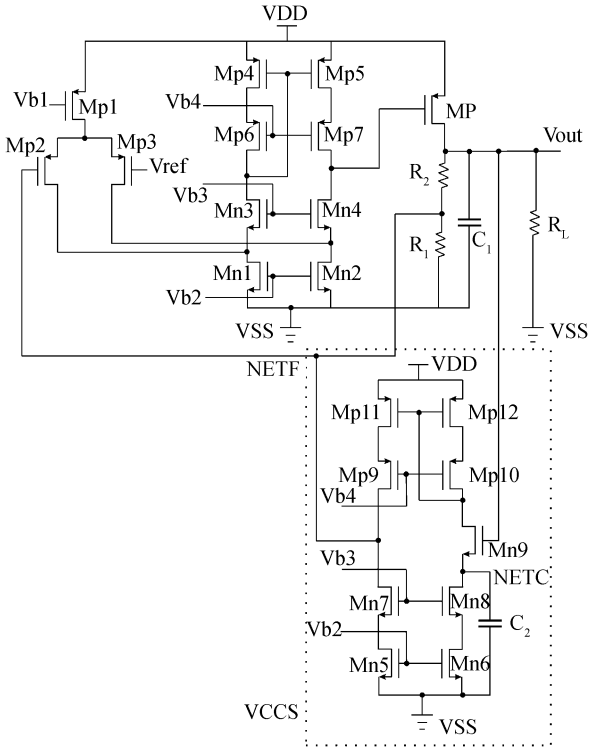


Fig. 4. Schematic of the error amplifier and the VCCS.

$I_{PM2} = nI_{PM1} = nI_{PM0} = nI_{PM4}$, $I_{SQ1} = I_{SQ0} = mI_{SQ2} = mI_{SQ3}$, the expression of the output reference voltage is:

$$V_{ref} = V_{BEQ4} + 2V_T \frac{R_1}{R_0} \ln(mn). \tag{9}$$

The structure shown in Fig. 3 can reduce the offset voltage. Q0, Q1, Q2, Q3, Q4, and Q5 are vertical PNP BJT with 5×5 μm^2 emitter area. Post-layout simulation shows that the variation of the output voltage of the presented bandgap voltage reference is only 4.7 mV in the worst case with temperature varying from –25 to 125 °C.

3.2. Error amplifier and VCCS

The structures of the error amplifier and the VCCS are shown in Fig. 4. The error amplifier has a folded-cascode structure, thereby providing high gain to improve the PSR of the proposed LDO as shown by Eqs. (7) and (8). The LDO has a two-stage structure, thereby simplifying the compensation circuits significantly. For a full on-chip scheme, the output capacitor C_1 is typically smaller than 100 pF.

The circuit of the proposed VCCS is shown within the dashed rectangle of Fig. 4. The VCCS is based on a cascode structure. The output impedance of the VCCS is high, thereby not affecting the static state voltage of the LDO. In addition, the VCCS is insensitive to the supply noise, thereby avoiding affecting the PSR of the LDO. The VCCS acts as a source follower and a current mirror. Thus, v_{out} is converted to small signal current and feeds into node NETF. The small signal current is given by:

$$i_{out} = \frac{sC_2 v_{out}}{1 + \dfrac{sC_2}{g_{mn9}}}. \tag{10}$$

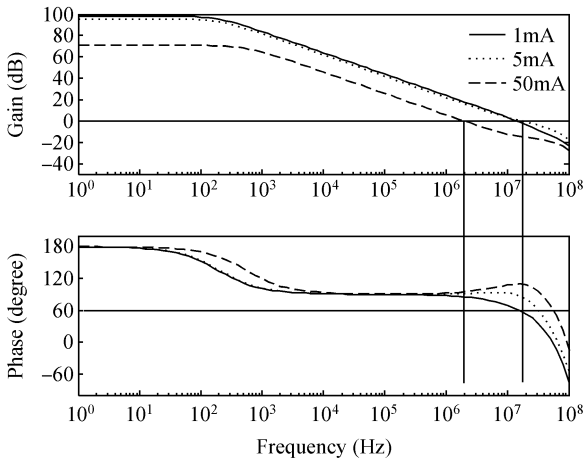


Fig. 5. Simulated open-loop gain of the proposed LDO (1 mA, 5 mA, and 50 mA).

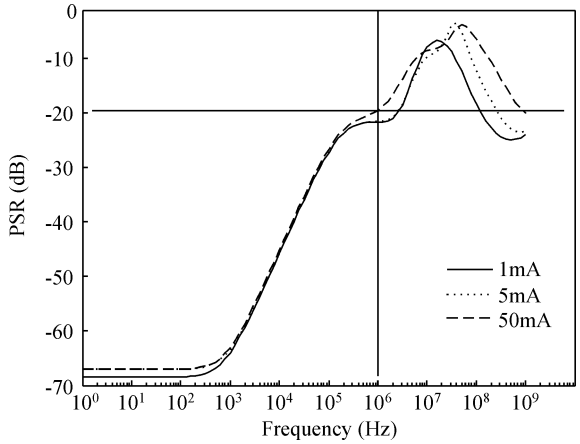


Fig. 6. Simulated PSR of the proposed LDO (1 mA, 5 mA, and 50 mA).

In this expression, g_{mn9} is the transconductance of Mn9. By ignoring the pole:

$$i_{out} = sC_2 v_{out}. \tag{11}$$

There are only two on-chip capacitors with the proposed VCCS. C_1 attached at the output node V_{out} for good transient response is about 50 pF. The compensation capacitor C_2 is about 0.18 pF, which is significantly smaller than other compensation techniques[1, 6]. Therefore, the proposed VCCS scheme is suitable for full on-chip design.

4. Simulated and experimental results

4.1. Simulation results

The proposed LDO was implemented in commercial 0.35 μm CMOS technology. Post-layout simulation of the proposed LDO regulator was performed with HSPICE. The open-loop gain results are shown in Fig. 5. The load current was changed from 1 to 50 mA. The open-loop gain is higher than 95 dB when the load current is smaller than 5 mA and is up to 70 dB when the load current is 50 mA. The unity gain frequency is in

Table 1. Performance summary and comparison of different full on-chip LDO implementations.

Parameter	Ref. [1]	Ref. [6]	This work
Technology (μm)	0.35	0.6	0.35
Supply voltage (V)	3.3	1.5–4.5	3.3
Nominal vout (V)	2.8	1.3	2.57
Active area (mm^2)	0.289	0.307	0.108
PSR (dB)	–57 @ 1 kHz	–60 @ 10 Hz	–58.7 @ 10 Hz
		–30 @ 1 MHz	–20 @ 1 MHz
Compensation capacitor (pF)	21	About 12 pF	0.18
Maximum load (mA)	50	100	50
Load regulation (mV/mA)	N/A	N/A	0.45
I_Q (μA)	65	38	92

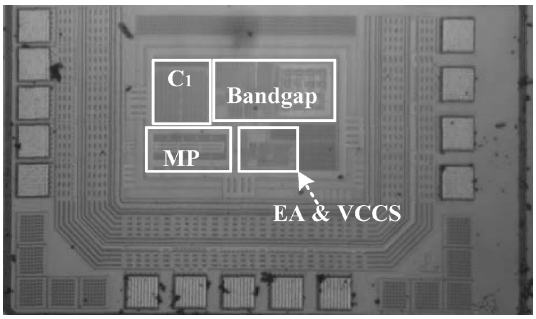


Fig. 7. Micrograph of the proposed LDO.

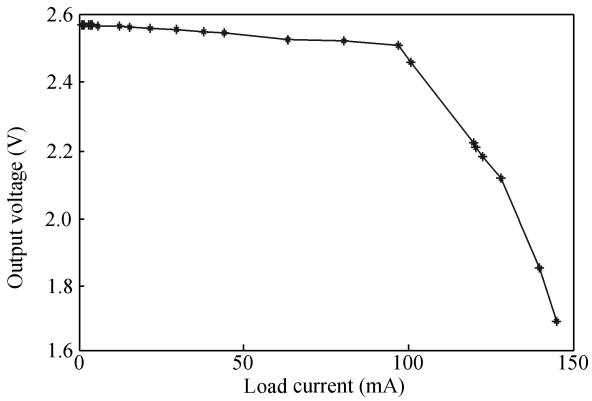


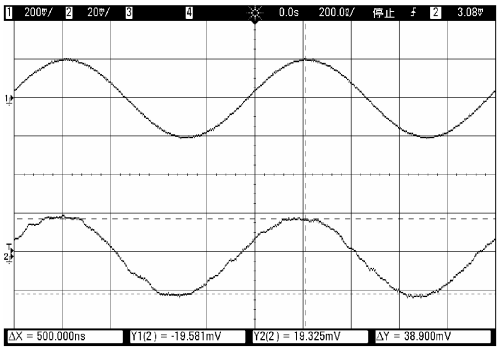
Fig. 8. Experimental output voltage as a function of the load current.

the range of 1.9–18 MHz. Furthermore, the PSR is effectively improved due to the wide loop-gain bandwidth.

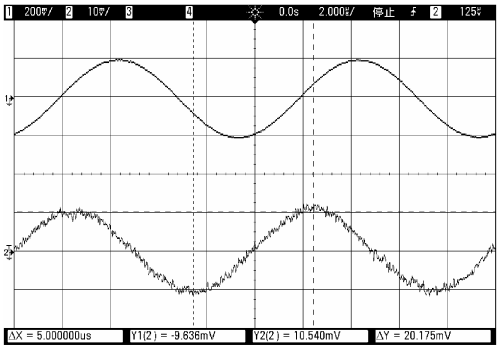
Figure 6 shows the PSR of the LDO. The simulated results reveal that the PSR is –67 dB at low frequency, –20 dB at a frequency of 1 MHz, and –27 dB at 100 kHz.

4.2. Experimental results

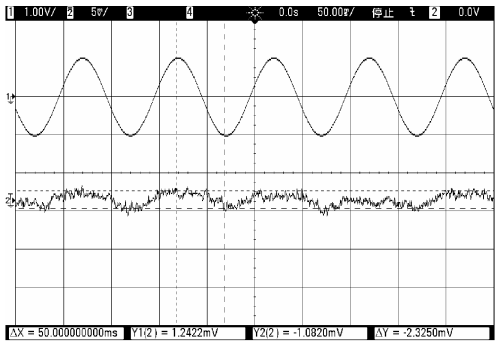
The proposed LDO was fabricated in commercial 0.35 μm CMOS technology. The chip micrograph is shown in Fig. 7. The active area is 400 × 270 μm^2. The output voltage of the LDO with the load current varying from 0.8 to 150 mA is shown in Fig. 8. When the load current is 0.8 mA, the output voltage is 2.572 V. Alternatively, the output voltage deviation is 20 mV when the load current is 44 mA. Therefore, the load regulation is 0.45 mV/mA. Figures 5, 6, and 8 indicate that the LDO is capable of sourcing an output current by up to 50 mA when the PSR of the proposed LDO is less than –20 dB.



(a)



(b)



(c)

Fig. 9. Measured PSR. (a) PSR at 1 MHz. (b) PSR at 100 kHz. (c) PSR at 10Hz.

Figures 9(a), 9(b), and 9(c) show the measured PSR at 1 MHz, 100 kHz, and 10 Hz, respectively. Channel 1 is the sinusoidal waveform applied to the supply voltage, and channel 2 is the AC ripple of the output voltage. In Fig. 9(a), the peak-to-peak voltage of channel 1 is 400 mV. Alternatively, the peak-to-peak voltage of channel 2 is 38.9 mV. Thus, the measured

PSR is –20.2 dB at 1 MHz. Figure 9(b) shows that the PSR is –25.9 dB at 100 kHz. The experimental results of 100 kHz and 1 MHz are similar to the simulated results shown in Fig. 6. Figure 9(c) shows that the PSR is –58.7 dB at 10 Hz, which is worse than the simulated result of –67 dB. The difference between the simulated result and experimental result at 10 Hz is partly caused by the accuracy of the oscilloscope, which is $\pm$2 mV.

The proposed LDO regulator consumes 92 μA quiescent current ($I_{\rm Q}$). Furthermore, the compensating capacitor is as small as 0.18 pF. A comprehensive comparison is made with other full on-chip LDO regulators[1, 6] as listed in Table 1, illustrating the advantages of the proposed full on-chip LDO regulator. Not only does the proposed LDO need the smallest compensating capacitor, but it also provides similar PSR as compared to the previously published techniques at low frequency.

5. Conclusions

A full on-chip CMOS low-dropout voltage regulator with high PSR is proposed in this paper. The proposed LDO is mainly used as the regulated power source for a VCO and charge-pump in PLL. The new LDO regulator was implemented in commercial 0.35 μm CMOS technology with 0.108 mm^2 active area. Experimental results show that the PSR of the LDO is –58.7 dB at a frequency of 10 Hz and –20 dB at a frequency of 1 MHz. The proposed LDO generates a zero by VCCS instead of relying on the zero generated by the load capacitor and its equivalent series resistance for stability. The compensating capacitor for the proposed scheme is only 0.18 pF, which is suitable for full on-chip design. The proposed error amplifier is a folded-cascode amplifier, which can provide high gain to improve the PSR of the LDO. The simple structure and small chip area are the advantages for full on-chip voltage regulators of integrated systems. The proposed LDO is able to deliver up to 50 mA load current.

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