A low power fast-settling frequency-presetting PLL frequency synthesizer*

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Abstract: This work presents the design and implementation of a 2.4 GHz low power fast-settling frequency-presetting PLL frequency synthesizer in the 0.18 μm CMOS process. A low power mixed-signal LC VCO, a low power dual mode prescaler and a digital processor with non-volatile memory are developed to greatly reduce the power consumption and the setting time. The digital processor can automatically calibrate the presetting frequency and accurately preset the frequency of the VCO under process variations. The experimental results demonstrate that the power consumption of the synthesizer is about 4 mA @ 1.8 V and that the typical setting time of the synthesizer is less than 3 μs.

Key words: fast-settling; presetting; low power; PLL; synthesizer
DOI: 10.1088/1674-4926/31/8/085002 **EEACC:** 2220

1. Introduction

Fast frequency switching of frequency synthesizers is one of the challenges in modern wireless communication circuit design. In a time-division multiple access system and fast frequency hopping spread spectrum systems, the lock-in time determines how fast the communication channels can be switched and therefore is a crucial specification of these systems. On the other hand, in order to prolong the life of a battery, a wireless communication terminal which a battery provides the power for should operate in low or ultra low power consumption. This paper proposes a low power fast-settling frequency-presetting PLL frequency synthesizer to solve the problem of low power and fast lock-in time in PLL synthesizer design.

Some methods have been proposed to reduce the lock-in time in PLL frequency synthesizers[1−3]. However, these methods cannot avoid a design tradeoff between the lock-in time and the phase noise or spurs. Recently we reported a direct frequency-presetting technique to realize a fast-settling PLL frequency synthesizer[4, 5]. The method can directly preset the target frequency with very small initial frequency error so that the synthesizer can speed up the lock-in process and avoid the tradeoff between the lock-in time and the phase noise or spurs. It can automatically compensate preset frequency variation with process and temperature. However, the calibration process usually is carried out case by case. The power consumption of the frequency synthesizer is not optimized and is not low enough.

This paper presents a novel low power fast-settling frequency-presetting PLL frequency synthesizer. We develop a mixed-signal LC VCO. The oscillation frequency of the VCO can be preset with a small initial frequency error by a digital processor. A non-volatile memory (NVM) inside the digital processor is used to store the presetting signals in order to avoid the calibration process case by case. A low power dual mode prescaler (DMP) is developed to reduce the total power of the synthesizer further. The proposed technique can accurately preset the target frequency of the mixed-signal LC VCO while drawing little power from the power supply and can avoid the calibration process case by case. In section 2 we describe the architecture of the proposed PLL frequency synthesizer, the frequency-presetting technique and the circuit implementation.

2. Circuit architecture and implementation

2.1. System architecture

Figure 1 shows a block diagram of the proposed low power fast-settling frequency-presetting PLL frequency synthesizer. It consists of six main blocks: a phase-frequency detector (PFD), a charge pump (CP), a second order loop filter (LPF), a mixed-signal LC VCO, a DMP and a digital processor with NVM. The mixed-signal LC VCO generates a sinusoidal signal with a frequency dependent on the output signal C[5:0] and P[3:0] of the digital processor and output voltage V_a of the LPF. The high frequency output signal f_o of the VCO is first divided by the DMP and then divided by the programmable divider which is inside the digital processor to generate a low frequency output so as to compare with the reference frequency f_r. The digital processor outputs the presetting signals C and P according to the divide ratio of the programmable divider and the divide ratio of the DMP. The digital processor can automatically compensate the presetting frequency variation with process and temperature. After first calibration by the digital processor, the presetting signals C and P are stored in the NVM of the digital processor so as to be used next time without calibration again.

Since the VCO and DMP always consume most of the power in the frequency synthesizer due to their high operation frequency, their power optimization is our main object. The digital processor consumes little power when it goes into operation mode due to its low frequency property, and the other

* Project supported by the National High-Tech Research and Development Program of China (Nos. 2008AA010703, 2009AA011606).
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Received 11 February 2010, revised manuscript received 1 April 2010

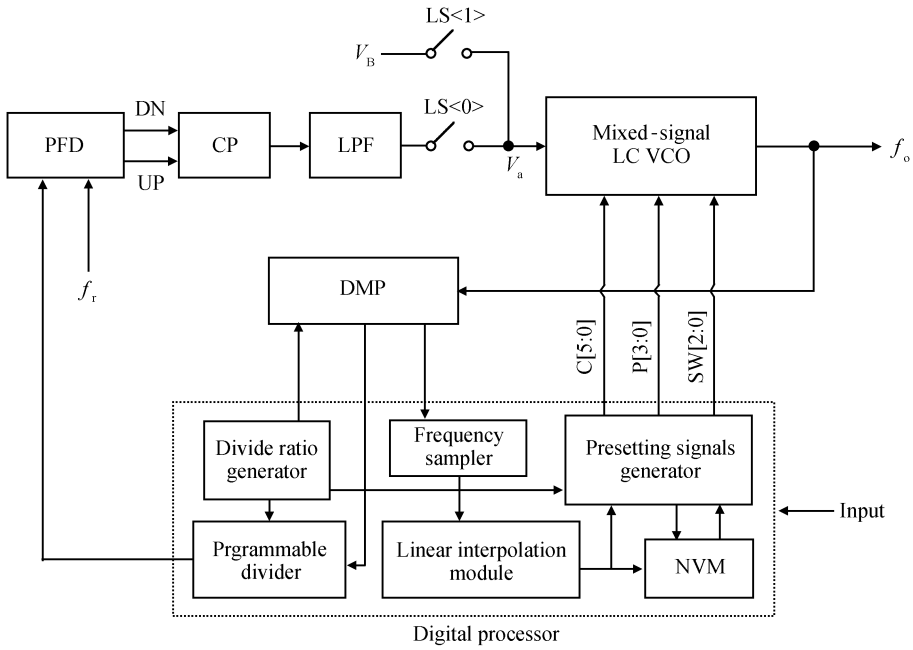

Fig. 1. System architecture of the PLL frequency synthesizer.

modules in the synthesizer also consume little power, so we can ignore their power compared with the VCO and DMP.

2.2. Frequency-presetting method and process

Since the lock-in time is significantly dependent on the magnitude of the initial frequency error, the smaller the initial frequency error is, the faster the lock-in time will be[5]. The lock-in time can be shortened as long as the initial frequency error can be reduced. In order to reduce the initial frequency error, a novel mixed-signal LC VCO is developed. The oscillation frequency of the VCO can be preset by the digital signal and can be controlled by the output voltage V_a of the LPF. The frequency-presetting method is to preset the frequency of the VCO to the target frequency by presetting signals P and C from the digital processor.

Figure 2 shows the dependence of the VCO presetting frequency on the presetting signals C and P at $V_a = 0.9$ V. The simulated result shows a good linear relation between the presetting frequency and the signal C under three P signals. However, the measured result shows that the dependence of the VCO presetting frequency on signal C deviates from the simulation result due to process variation and device parasitic effect. In order to preset the VCO frequency accurately, we need to obtain the actual relation between the presetting signals and the VCO oscillation frequency, so an automatic calibration process is needed. The automatic calibration process automatically calibrates the relation between the presetting frequency and the presetting signals C and P and produces measured data to form a fitting curve. The whole calibration process can be done by the frequency sampler and the linear interpolation module of the digital processor[5].

The frequency synthesizer can operate in the following two modes: calibration mode and operation mode. In calibration mode, the phase lock loop is opened by switch LS<0>, and the input of the presetting module is biased at VB through the switch LS<1>, then we input the frequency information into the

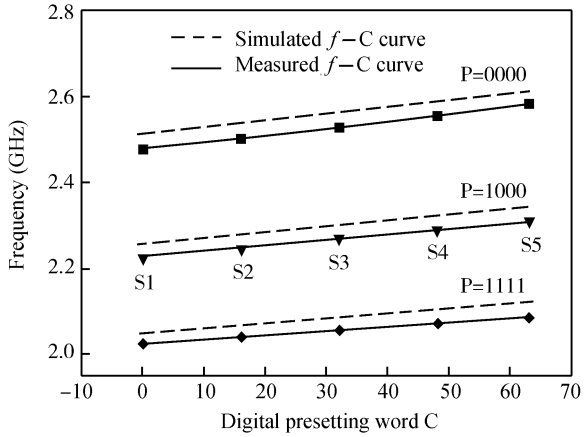

Fig. 2. Output frequency f_o versus presetting signal C[5:0].

digital processor. With the aid of the frequency sampler and the linear interpolation module of the digital processor, the digital processor can automatically calculate and obtain the presetting signals C and P. Then these C and P are sent to the NVM to store. In most situations, we need to store several different presetting signals C and P in the NVM which are related to several different frequencies, so the process described above may be carried out several times. After the several groups of presetting signals C and P are stored in the NVM, the calibration mode is finished. In operation mode, the switch LS<1> is opened, and the phase lock loop is closed by switch LS<0>. The digital processor reads out the

presetting signals C and P from the NVM according to the divide ratio information of the programmable divider and outputs to the mixed-signal LC VCO. After the output frequency of the VCO is preset with very small initial error, the output voltage V_a of the LPF precisely tunes the frequency of the VCO to the target frequency. Therefore the synthesizer can be settled

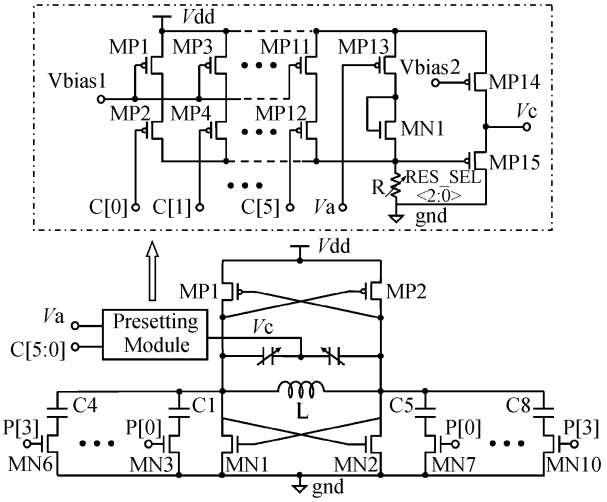

Fig. 3. Mixed-signal LC-tank VCO with presetting module.

down in a very short time. Its lock-in time does almost not depend on frequency step, process variation, device parasitic effect and chip temperature. It can avoid the calibration process case by case due to the non-volatile property of the NVM.

2.3. Low power mixed-signal VCO implementation

Figure 3 shows the proposed mixed-signal VCO. In order to reduce the power consumption of the VCO, a complementary type LC-tank VCO is used in our mixed-signal VCO. The fundamental minimum for the power consumption of an LC VCO is expressed as follows[6]:

$$P_{\text{loss}} = \frac{R}{2L^2\omega_{\text{c}}^2} V_{\text{peak}}^2, \tag{1}$$

where R represents the loss of the inductor, L is the inductor value, ω_{c} is the VCO oscillation frequency, and V_{peak} is the oscillation amplitude. Under the low power restriction, a large value of inductor L is chosen according to Eq. (1). A large inductor L means less frequency tuning range, so a design tradeoff has been made between the tuning range and low power. The presetting module receives the presetting digital signal C[5:0] and the output voltage V_{a} of the LPF, and then produces a VCO control signal V_{c}. On the other hand, the digital signal P[3:0] controls the capacitance of the LC tank and generates sixteen overlapping discrete tuning curves to lower the VCO gain K_{v} and to cover the desired frequency range. A smaller K_{v} will be of benefit to the phase noise performance. The multiple tuning curves can compensate for the variation in the VCO frequency due to the process variation.

The presetting module is a mixed-signal circuit. In order to reduce the power of the presetting module, we use a resistor R with a large value. The value of R can be tuned by the 3-bit digital signal RES_SEL<2:0> to make the presetting frequency more accurate. The last stage of the presetting module is a source follower to make sure that the output voltage V_{c} is in the middle area of the VCO linear tuning region. When a digital signal C[5:0] is inputted into the presetting module, the module will produce a voltage signal V_{c} to preset the frequency of the VCO with a small initial frequency error. Then the output voltage V_{a} of the LPF accurately tunes the frequency of the VCO by adjusting the current through MP13. If the divide ratio of the synthesizer is changed, the presetting signals C[5:0] and P[3:0] can accurately preset the frequency of the VCO. Then the output voltage V_{a} of the LPF precisely tunes the frequency of the VCO within a very short time.

The mixed-signal LC VCO operates at 1.8 V power supply. We select an inductor of relatively large value and quality factor in the process design kit. The post-simulation results indicate that the power consumption of the mixed-signal LC VCO is about 3 mA (2.6 mA for the LC VCO and 0.4 mA for the presetting module) while achieving 1.3 V peak-to-peak amplitude at a standard process corner. The phase noise is –121 dBc/Hz at 3 MHz offset from the center frequency of 2.4 GHz.

2.4. Low power DMP implementation

In order to reduce the total power of the frequency synthesizer, a low power DMP is developed. Figure 4 shows the proposed low power DMP module. The DMP is a divide-by-32/33 dual mode prescaler operating at 2.4 GHz. The proposed DMP consists of divide-by-2/3 circuits and four divider stages. The first and second stages consist of divide-by-2 circuits (Div_HS) and NAND gates (Nand2_HS) operating at high frequency, the third and four stages consist of divide-by-2 circuits (Div2_LP) and NAND gates (Nand2_LP) operating at low frequency.

All these modules are implemented in differential circuit topologies in order to reduce the number of inverters used in the circuits and make sure that the DMP operates at a low supply voltage. The divide-by-2/3 circuit is composed of a high speed D flip flop with the function of NOR logic. All the dividers and the NAND gates used in the DMP are implemented by source-couple logic (SCL) which has the merits of low amplitude, low noise, high speed and high anti-interference ability. In order to optimize the power consumption, we use different SCL logic circuits according to the operation frequency. Figure 5 shows the divide-by-2 circuit operating at high frequency. M3, M6, M9 and M12 are the input transistors, the gates of M1 and M2 are connected to the differential output OUTN and OUTP respectively. Figure 6 shows the divide-by-2 circuit operating at low frequency; this divider uses M13–M16 instead of the resistors R1–R4 used in Fig. 5 to reduce the static power consumption. Figure 7 shows the NAND gate operating at low frequency and high frequency.

The DMP operates at 1.8 V power supply. The post-simulation result indicates that the power consumption of the DMP is about 0.6 mA.

3. Experimental results

The proposed synthesizer is implemented in the 1P6M, 0.18 μm CMOS process with 1.8 V power supply. It integrates a 192 bit NVM memory in the standard CMOS process[7]. Figure 8 shows a micrograph of the chip. Since the PLL and the NVM are integrated on a larger transceiver single chip, we only mark the PLL and the NVM respectively. The total synthesizer core area is 0.7 mm^2.

Figure 9 shows the dependence of the VCO presetting frequency on the signals C and P at V_{a} = 0.9 V. As shown in Fig. 9, the measured result shows a good linear relation between the presetting frequency and the signal C under five P[3:0] signals. Considering that there are sixteen P[3:0] sig-

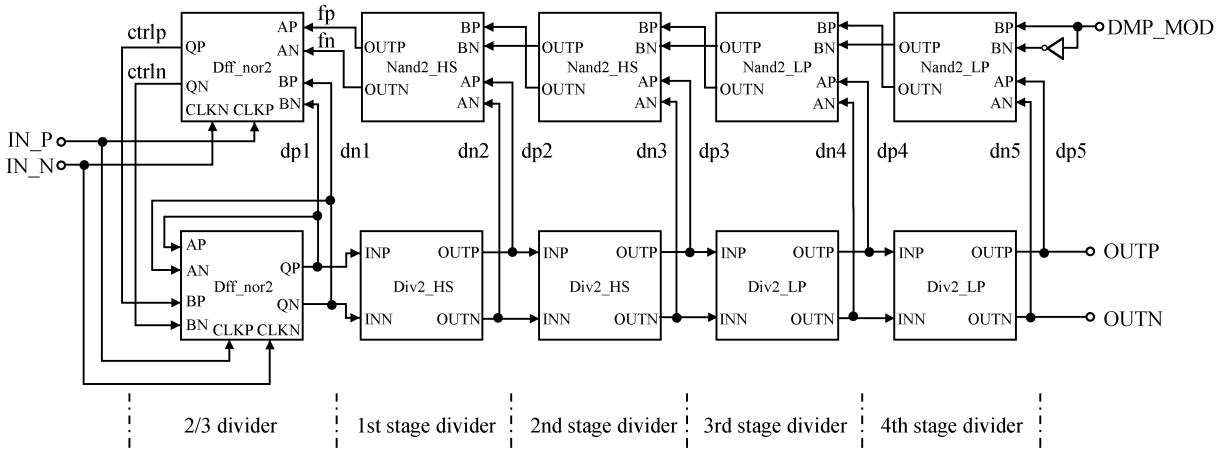

Fig. 4. Low power DMP module.

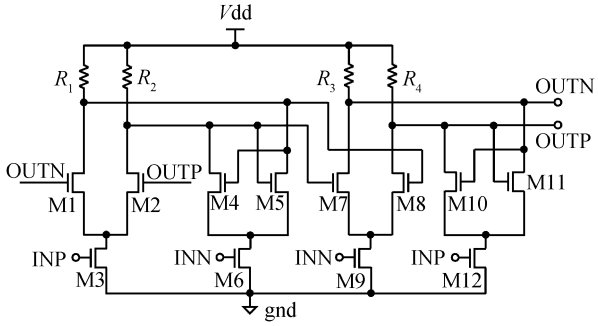

Fig. 5. Divide-by-2 circuit operating at high frequency.

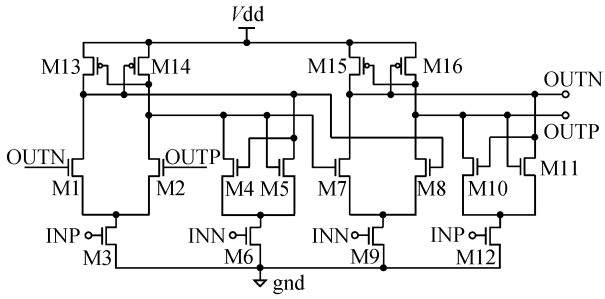

Fig. 6. Divide-by-2 circuit operating at low frequency.

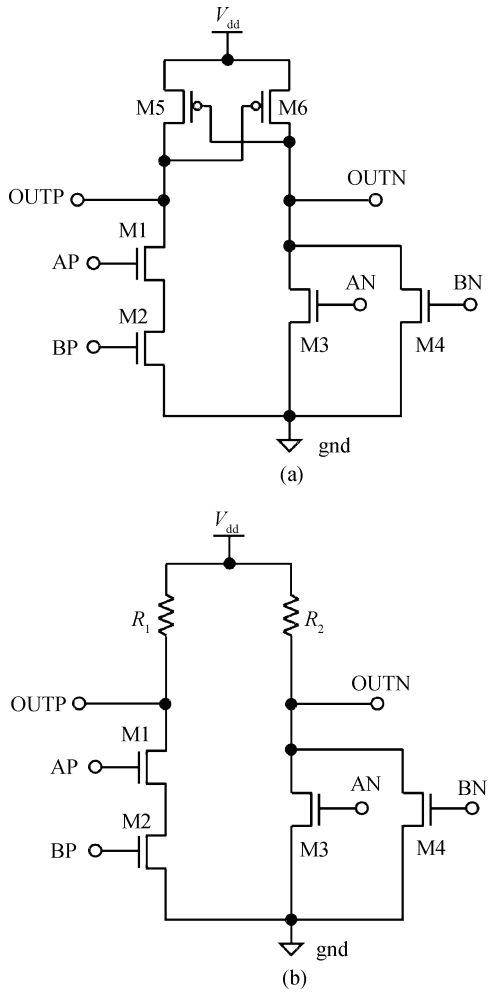

Fig. 7. (a) NAND gate operating at low frequency. (b) NAND gate operating at high frequency.

nals, the range of VCO frequency can cover the frequency 2.03 to 2.58 GHz.

Figure 10 shows the measured results of the transfer characteristics of the proposed VCO with different frequency-presetting signals C when the signal P[3:0] is set to '1000'. The transfer characteristics show that the VCO gain is about 60 MHz/V in the voltage range of 0.6 to 1.2 V which is a linear region due to the source follower in the presetting module. If the signal P is changed, we will get other groups of transfer characteristic curves which can cover the desired large frequency range.

After the synthesizer has completed the calibration mode, frequency hopping automatically between any two frequencies is performed randomly and continuously. The frequency hopping is measured by a high speed oscilloscope. Figure 11 shows a typical frequency hopping characteristic of the synthesizer. The dependence of the frequency on time shows the frequency hopped rapidly from 2.380 to 2.402 GHz at 105 μs. The lock-in time is less than 3 μs, which is much shorter than a synthesizer without the frequency-presetting function. Figure 12 shows the measured phase noise of the output signal. The

Table 1. Frequency synthesizer performance comparison.

Parameter	This work	Ref. [4]	Ref. [5]	Ref. [8]
Process	0.18 μm CMOS	0.35 μm CMOS	0.35 μm RF	0.18 μm CMOS
Chip core area (mm^2)	0.7	0.4	0.4	4.8
Supply voltage (V)	1.8	3.3	3.3	1.8
Current consumption (mA)	4	22	22	20.9
Frequency range (GHz)	2.03–2.58	0.56–0.82	2.39–2.6	2.4–2.5
Loop bandwidth (kHz)	< 100	< 100	< 100	> 730
VCO gain (MHz/V)	60	25	30	60
Phase noise (dBc/Hz)	–117 @ 3 MHz	–85 @ 10 kHz	–112 @ 600 kHz	–124 @ 3 MHz
Lock-in time (μs)	< 3	< 10	3	35
VCO type	LC	Ring	LC	LC

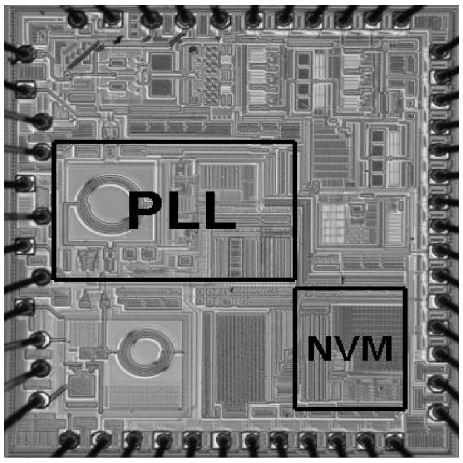

Fig. 8. Chip micrograph.

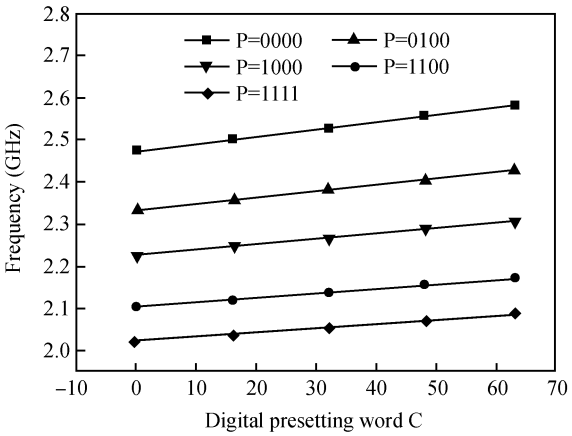

Fig. 9. Output frequency f_o versus presetting signal C[5:0].

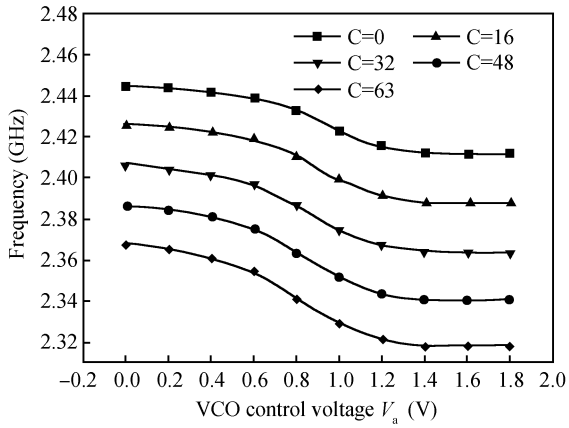

Fig. 10. Transfer characteristics of the proposed VCO.

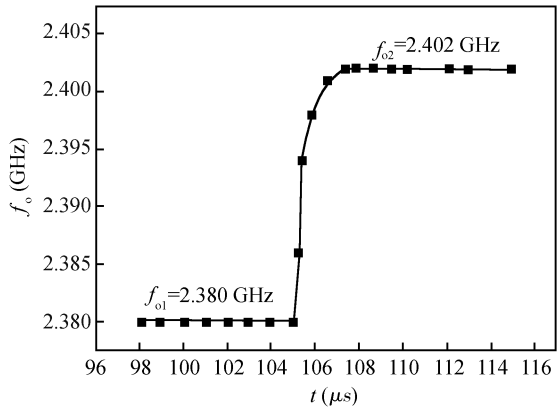

Fig. 11. Frequency hopping characteristic.

phase noise is –117 dBc/Hz at 3 MHz offset from the center frequency of 2.4 GHz. The phase noise is higher than Ref. [5] due to the following reasons: firstly, the power consumption of the mixed-signal VCO is lower than that of Ref. [5]; secondly, the VCO tuning range is larger than that of Ref. [5]; finally, in order to reduce the power of the presetting module, a large resistor is chosen which means that the presetting module will contribute more noise, therefore degrading the phase noise of the VCO. The total current consumption of the synthesizer is 4 mA including the NVM. The results indicate that the proposed synthesizer has a fast lock-in speed and reasonable noise performance even at low power consumption. A comparison of this synthesizer with the published literature is summarized in Table 1. The current consumption is very low compared with Refs. [4, 5] while achieving almost the same performance.

4. Conclusion

We have proposed a low power fast-settling frequency-presetting PLL frequency synthesizer. The technique accurately presets the frequency of a VCO with small initial frequency error and greatly reduces the lock-in time. The synthesizer with NVM avoids the calibration process case by case, which improves the efficiency of the frequency-presetting

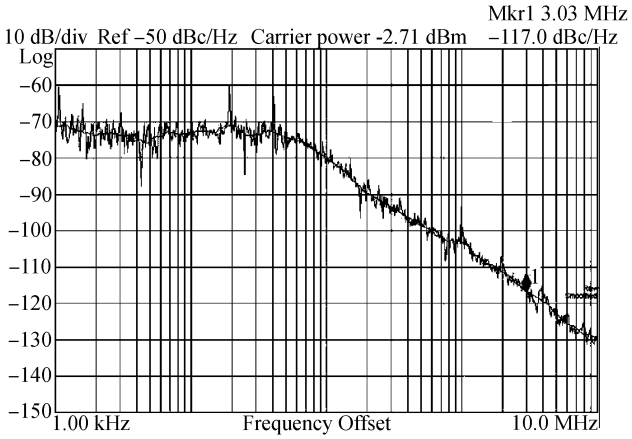

Fig. 12. Phase noise of the output signal.

method and greatly speeds up the lock-in process of the synthesizer. We implemented the synthesizer in a 0.18 μm CMOS process. The measured results showed that the frequency synthesizer has a fast lock-in speed and low power.

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