# DCM, FSM, dead time and width controllers for a high frequency high efficiency buck DC–DC converter over a wide load range*

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**Abstract:** This paper presents a width controller, a dead time controller, a discontinuous current mode (DCM) controller and a frequency skipping modulation (FSM) controller for a high frequency high efficiency buck DC–DC converter. To improve the efficiency over a wide load range, especially at high switching frequency, the dead time controller and width controller are applied to enhance the high load efficiency, while the DCM controller and FSM controller are proposed to increase the light load efficiency. The proposed DC–DC converter controllers have been designed and fabricated in the Chartered 0.35 $\mu$m CMOS process, and the measured results show that the efficiency of the buck DC–DC converter is above 80% over a wide load current range from 8 to 570 mA, and the peak efficiency is 86% at 10 MHz switching frequency.

**Key words:** buck DC–DC converter; dead time controller; discontinuous current mode; width controller; frequency skipping modulation

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## 1. Introduction

In today's battery-powered palm-size devices, such as cellular phones, PDAs, and MP3s, the low-voltage buck DC–DC converter as a power management unit has become an essential block for maximizing the system run time. The ever increasing scale of these portable systems drastically increases their power consumption during working mode, and makes the motherboards more and more crowded. As a result, two critical challenges have been presented to buck DC–DC converter designers. One is that the converter must maintain a high efficiency over a wide load range, especially at light load since the converter operates in stand-by mode most of the operating time. The other is that a higher switching frequency should be chosen to further shrink the volume of the on-board low-pass LC filter. Unfortunately, higher switching frequency deteriorates the power efficiency.

To improve the efficiency, a detailed analysis of various losses must be carried out. Generally speaking, the efficiency of a buck converter is mainly restricted by gate-drive loss, conduction loss, switching loss, and body-diode conduction loss[1]. Normally, the gate-drive loss is inversely proportional to the size of the power MOSFETs, while the conduction loss is proportional to it. As a result, an optimal size of power MOSFETs can be realized by the width control technique[2, 3]. At light load, gate-drive loss and switching loss are dominant, and both of them are proportional to the switching frequency. A common solution is to introduce the pulse-frequency modulation (PFM) mode[2, 4]. However, the converter output spectrum varies with the load current in PFM mode, which causes a supply-integrity problem in some spectrum-sensitive environments such as mobile communication systems. The gate voltage control technique[5] avoids this problem, and reduces the gate-drive loss to improve the light load efficiency. However, the gate voltage swing of power MOSFETs is difficult to control precisely, and, even worse, the on resistance of power MOSFETs is increased. Therefore, the frequency skipping modulation (FSM) technique can be a better solution[6]. When the load current is smaller than half the peak-to-peak inductance current ripple, the inductor current will become minus at some time of the switching cycle. This reverse current discharges the filter capacitor, and reduces the power efficiency. As a result, it is necessary to make the converter operate at DCM mode[7]. Finally, in order to avoid large short-through current between the power PMOSFET and NMOSFET, a long dead time (20 ns for a maximum load of 600 mA) margin is required for possible process and temperature variations. The body-diode conduction of the power NMOSFET during such a long time introduces large power consumption, especially at high load. Therefore, it is preferable to automatically adjust the dead time according to the load condition.

In this paper, an improved DCM controller is proposed to reduce the loss when the current of the inductor discharges the charge on the filter capacitor through the power NMOSFETs, and a novel dead time controller is given to adjust the dead time adaptively. Finally, a DCM controller, an FSM controller, a dead time controller and a width controller are proposed to implement a high efficiency and high frequency power converter over a wide load range.

## 2. The proposed controllers for the high efficiency high frequency buck DC–DC converter

As shown in Fig. 1, the architecture of the proposed controllers for the high efficiency buck DC–DC converter is described. It consists of a current sensing circuit, buffers, a width controller, a dead time controller, a DCM controller, an FSM

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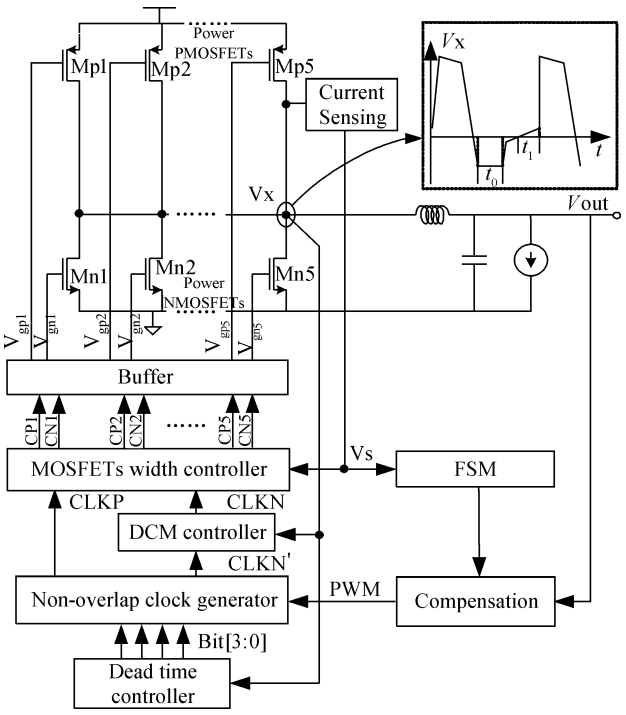



Fig. 1. Architecture of the proposed controllers for the buck DC–DC converter.

controller, etc.

A current sensing circuit is applied to sample the current of the power PMOSFET, which stands for the load current, and $V_s$ is in proportion to the with the load current[3] and the selected optimal size of power MOSFETs is based on $V_s$, which indicates the switching frequency of the buck DC–DC converter. At light load, low frequency can decrease the gate-drive loss and the switching loss. According to $V_s$, the switching frequency can be selectable among 10 MHz, 5 MHz and 1 MHz. The selected frequency is as an input of the non-overlap clock generator producing two non-overlap clocks, and the dead time is controlled by the dead time controller based on the voltage of $V_x$.

$V_x$ reflects the gate signals of the power MOSFETs, and explains whether the dead time of the gate signals of the power MOSFETs is long and the current of the inductor is minus or not. As shown in Fig. 1, the body-diode of power NMOSFETs is forward turned on in the stage of $t_0$, which illustrates that the dead time is long. In the stage of $t_1$, $V_x$ is larger than zero when the power NMOSFET is turned on, which indicates that the current of the inductor is minus. Therefore, the dead time controller and DCM controller are proposed to realize the ideal gate signals of the power MOSFETs. To improve the efficiency of the buck DC–DC converter over a wide load range, the width controller, dead time controller, DCM controller and FSM controller will be shown respectively.

### 2.1. Buffers, power MOSFETs and width controller

At high load, gate-drive loss (including buffer losses) and conduction loss of the power MOSFETs are the main losses as shown in Ref. [1]. These losses at fixed switching frequency depend on the load current, the tapering factor of the buffer, the power MOSFETs' size and other process-dependent factors[8, 9]. The common method of improving the efficiency is to adjust the power MOSFETs' size to compromise the gate-drive loss and the conduction loss. The relationship between the optimal power MOSFETs' size, the tapering factor of the buffer and load current can be achieved by optimizing the losses. According to Refs. [8, 9], the optimal power MOSFETs' size is as follows:

$$W_{\mathrm{p,op}} = \sqrt{\frac{R_{\mathrm{on,p}} I_{\mathrm{RMS,p}}^2}{f_s V_{\mathrm{DD}}^2} \left( \frac{(b+1)\, C_{\mathrm{inv,o}} + ap C_{\mathrm{inv,in}}}{ap - b - 1} \right)^{-1}}, \tag{1}$$

$$W_{\mathrm{n,op}} = \sqrt{\frac{R_{\mathrm{on,n}} I_{\mathrm{RMS,n}}^2}{f_s V_{\mathrm{DD}}^2} \left( \frac{(b+1)\, C_{\mathrm{inv,o}} + an C_{\mathrm{inv,in}}}{an - b - 1} \right)^{-1}}, \tag{2}$$

where $R_{\mathrm{on,p}} = L/(\mu_{\mathrm{p}} C_{\mathrm{ox}}(V_{\mathrm{GS}} - V_{\mathrm{TH,p}}))$, $I_{\mathrm{RMS,P}} = \sqrt{D(I_{\mathrm{load}}^2 + \Delta i^2/3)}$; $R_{\mathrm{on,n}} = L/(\mu_{\mathrm{n}} C_{\mathrm{ox}}(V_{\mathrm{GS}} - V_{\mathrm{TH,n}}))$, $I_{\mathrm{RMS,n}} = \sqrt{(1-D)\left(I_{\mathrm{load}}^2 + \Delta i^2/3\right)}$; $ap$ and $f_s$ are the tapering factor of the power MOSFET's buffer; $C_{\mathrm{inv,\,in}}$ and $C_{\mathrm{inv,\,o}}$ are the input and output capacitors of the standard inverter, respectively; $b$ is the ratio of the PMOS transistor's size and the NMOS transistor's size of the standard inverter; $W_{\mathrm{p}}$ and $W_{\mathrm{n}}$ are the width of the power PMOSFET. The PMOS transistor's size and NMOS transistor's size of the standard inverter are 3 $\mu$m/0.5 $\mu$m and 1 $\mu$m/0.5 $\mu$m, respectively.

According to Eqs. (1) and (2), the optimal power MOSFETs' size over the entire load range is proportional to the load current, and the relationship between optimal power MOSFETs and load current is shown in Table 1. Therefore, an accurate current sensing circuit is necessary to select the optimal power MOSFETs' size.

An improved current sensing circuit for the width controller is proposed in Fig. 2, which is different from the reported current sensing circuit[2, 10]. Mp$i$/Mn$i$ ($i$ = 1–5) is the power PMOSFET/NMOSFET, Ms$i$ is the sensing PMOS transistor. The ratio of Mp$i$'s size to Ms$i$'s is 800 : 1. The gates of every power PMOSFET (Mp$i$) and the corresponding sensing PMOS transistors (Ms$i$) are connected, so when the optimal power PMOSFETs' size increases with the rise of the load current, the sensing transistor's size increases too. The ratio of the power PMOSFETs' size to the sensing transistor's size is fixed when the optimal power PMOSFETs' size alters. The difference between the proposed current sensing circuit and the methods mentioned by Refs.[2, 10] is that the sensing transistors (Ms$i$) are connected to $V_{\mathrm{gp}i}$ not to ground. So Mp$i$ and Ms$i$ are matched well in layout for a better accuracy performance, and more easily keep the ratio of the PMOSFETs' size and the sensing transistor's size constant. The Me$i$ is used to isolate $V_{\mathrm{x}}$ and $V_{\mathrm{inn}}$, and Mc$i$, Md$i$ just make $V_{\mathrm{inn}}$, $V_{\mathrm{inp}}$ stay high when $V_{\mathrm{gp}i}$ is high. When $V_{\mathrm{gp}i}$ becomes low, the voltage of $V_{\mathrm{inp}}$ will follow that of $V_{\mathrm{inn}}$ very quickly, which is better for high frequency DC–DC converters. Due to the amplifier (A0), the voltage of $V_{\mathrm{inn}}$ can be identical to $V_{\mathrm{inp}}$, and the current of Ms$i$ is in proportion to the current of Mp$i$, which is the current of the inductor and stands for the load current. The size of the power MOSFETs and the switching frequency can be controlled by $V_s$, which is generated from a sample and

Table 1. Optimal power MOSFETs' size versus load current.

| Load current (mA) | Bit[3:0] | Power PMOSFETs' size (μm/μm) | Power NMOSFETs' size (μm/μm) |
|---|---|---|---|
| < 120 | 0000 | 7560/0.5 | 2520/0.5 |
| 120–240 | 0001 | 15120/0.5 | 5040/0.5 |
| 240–360 | 0011 | 22680/0.5 | 7560/0.5 |
| 360–480 | 0111 | 30240/0.5 | 10080/0.5 |
| > 480 | 1111 | 37800/0.5 | 12600/0.5 |

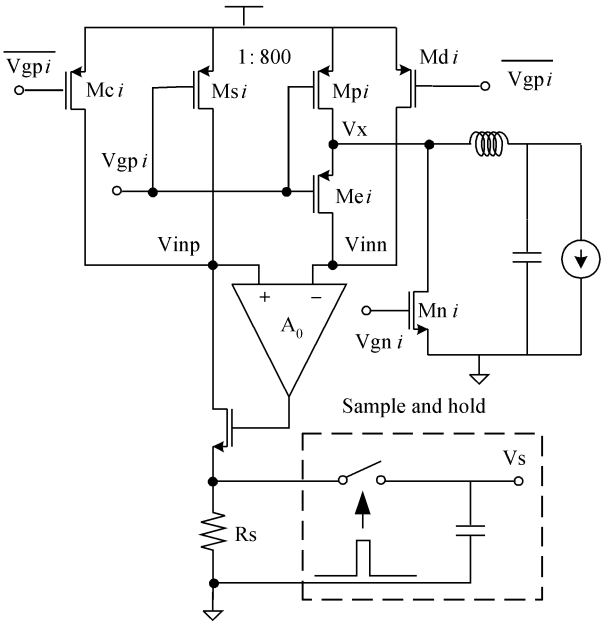



Fig. 2. An improved current sensing circuit for the width controller.

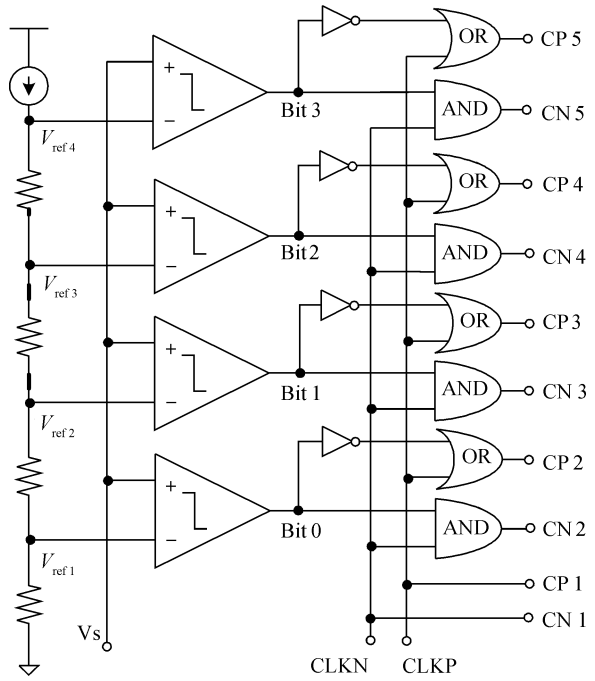



Fig. 3. Width controller for the power PMOSFET and NMOSFET.

hold circuit. Based on $V_s$, Figure 3 shows a width controller for the power MOSFETs. According to Figs. 2 and 3, $V_s$ and the voltage references are all directly related to the resistors, so changes of the resistors do not influence the comparative results of $V_s$ and the voltage references. Since the gate signals of the power MOSFETs are controlled by the comparative results, the optimal power MOSFETs' size can be scaled according to the load current. For example, when $V_s$ is larger than $V_{ref2}$ and smaller than $V_{ref3}$, CP3/CP2 and CN3/CN2 will follow the clock signals CLKP and CLKN respectively. But CP5/CP4 and CN5/CN4 are shielded by the comparators. CP5/CP4 stays high while CN5/CN4 keeps low. The power MOSFETs corresponding to these signals are always turned off at this load current. Adaptive adjustment of the power MOSFET size with the load current is realized.

### 2.2. Dead time controller

As the optimal dead time varies with the load current, a novel dead time controller is presented to realize optimal dead time at any load current, as shown in Fig. 4. When the dead time is long, the body-diode of the power NMOSFET is forward turned on leading to a $V_x$ voltage of about –0.7 V. The BJT of Mx in Fig. 4 will also be turned on because the forward voltage of the body-diode of the power NMOSFET and the $V_{be}$ of the BJT of Mx are the same, and then the voltage of $V_c$ is low. The BJT of Mx is comprised of bulk, drain and source of Mx. When the D flip-flop is triggered by CLKN, Q will be high. B[3:0] will be increased (for example 0010 → 0011), and $I_c$ in Fig. 4 will increase accordingly, so the dead time will become smaller. When the counter increases to 1111, the counter will stay in this state until Q is low and the next active clock edge arrives.

On the other hand, when the dead time is short, the body-diode of Mx cannot be turned on, $V_c$ will keep high, and Q will be low and B[3:0] will be decreased (for example 1011 → 1010); when the counter decreases to 0000, it will stay in this state, until Q is high and the next active clock edge arrives. Meanwhile, the dead time is the longest dead time and the time is 20 ns. So, finally, B[3:0] will stay in the state where the dead time is appropriate at any load condition and the body-diode loss is minimum. Some delay circuits are adopted to delay the time when CLKN arrives at the counter. The delayed CLKN triggers the counter after Q is steady.

### 2.3. DCM and FSM controllers

When the load current is light, it is possible for the current of the inductor to become minus. At this state, the charge in the filter capacitor will flow to ground through the inductor and power NMOSFET between $t_2$ as shown in Fig. 5, which is a loss for the DC–DC converter. To reduce this loss, the proposed DCM controller circuit is shown in Fig. 5.

As shown in Fig. 5, while the power NMOSFET is on,

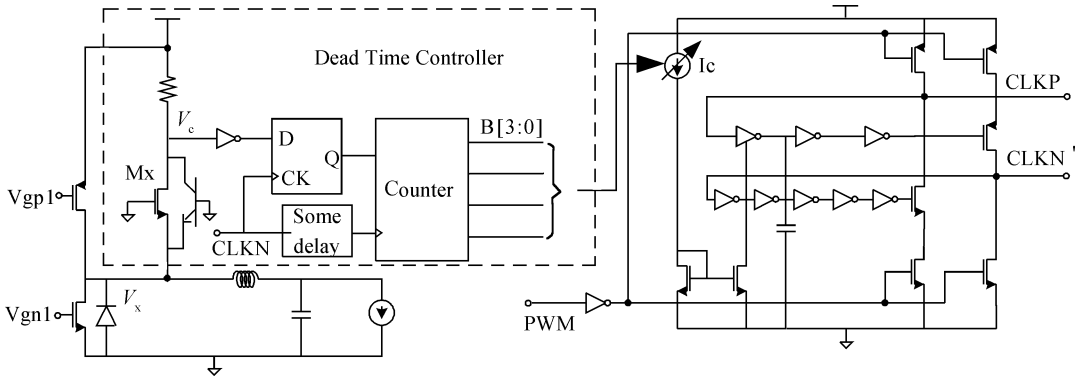



Fig. 4. A novel optimal dead time controller.

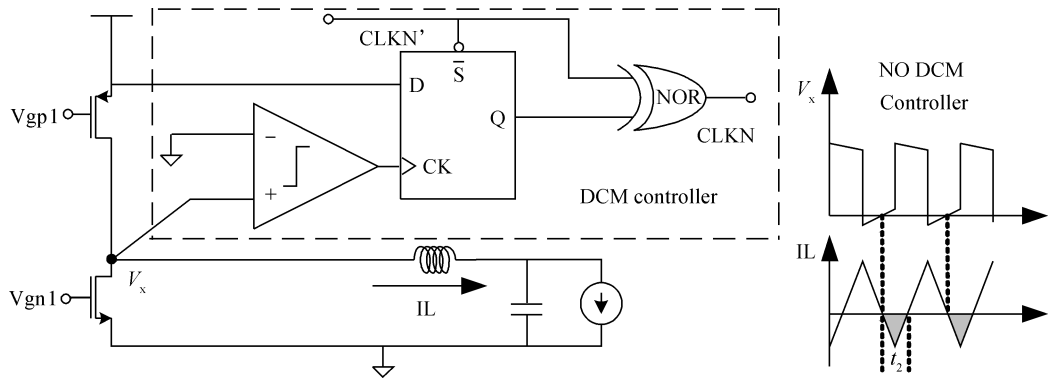



Fig. 5. DCM controller circuit and the waveform of Vx and IL without the DCM controller.

when the current of the inductor is plus, the voltage of $V_x$ is minus, but when the current of the inductor becomes minus, $V_x$ is plus. A comparator is adopted to differentiate this transformation. When the current of the inductor changes from positive to negative, a rising edge is sent to the D flip-flop. Then the output of the D flip-flop and the gate signal of the power NMOSFET act as the input of exclusive-OR gate. CLKN will become low, and the power NMOSFET will be turned off. The charge on the filter capacitor will not flow to the ground through the power NMOSFET. Thus, the loss is decreased.

Another way to improve the light-load efficiency of the buck DC–DC converter is FSM mode. At light load, the gate-drive loss and switching loss dominate the losses, and they are positively related to the switching frequency.

FSM can decrease the power losses and improve the light-load efficiency. The proper frequency is also selected by $V_s$. When the buck DC–DC converter works in DCM mode, the relation between $V_s$, the load current $I_o$ and the switching frequency $f_s$ is as follows,

$$V_s = \sqrt{\frac{R_s^2 2\,(V_{in} - V_{out})\,V_{out} I_o}{K^2 f_s L V_{in}}}, \tag{3}$$

where $V_s$ and $R_s$ are the output voltage and resistor of the current sensing circuit, $V_{in}$ and $V_{out}$ are the input and output voltages of the buck DC–DC converter, $f_s$ is the switching frequency, $L$ is filter inductor, $I_o$ is the load current, and $K$ is the ratio of the power PMOSFETs' size to the sensing transistor's size. According to Eq. (3), the output voltage ($V_s$) of the current sensing circuit is related to $I_o$ and $f_s$, so $f_s$ can be controlled by the current of the buck DC–DC converter.

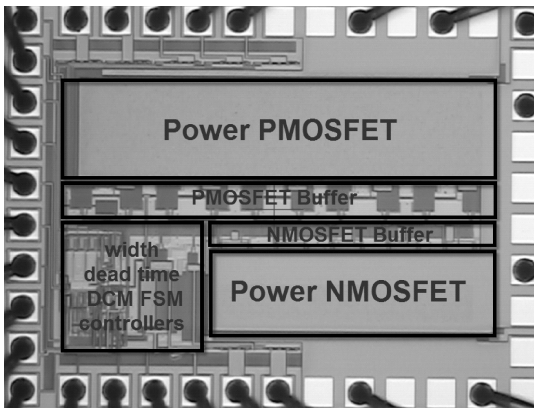
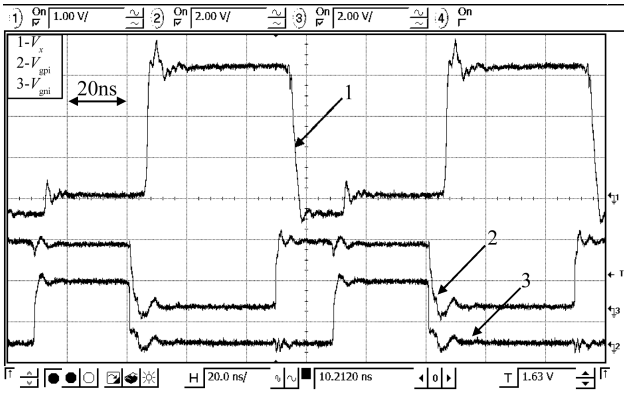



Fig. 6. Chip photograph.

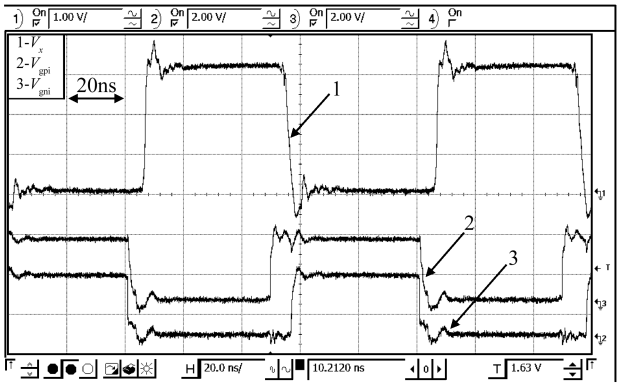
When the load current is larger than 100 mA, the buck DC–DC converter operates at 10 MHz. When the load current is larger than 50 mA and smaller than 100 mA, the converter works at 5 MHz, because when the load current is smaller than 100 mA, the converter begins to enter DCM mode at 5 MHz switching frequency. When the load current is smaller than 50 mA, it runs at 1 MHz. In this condition, the current of the inductor is minus almost half of one switching frequency, and DCM mode will improve the efficiency more apparently.

Table 2. Component parameter summary.

| Parameter | Value |
|---|---|
| Process | Chartered 0.35 $\mu$m CMOS process |
| $L$ | 0.47 $\mu$H |
| $C$ | 4.7 $\mu$F |
| Power NMOSFET size | 12600 $\mu$m/0.5 $\mu$m |
| Power PMOSFET size | 37800 $\mu$m/0.5 $\mu$m |
| Chip area | 1.4 mm$^2$ |




(a)




(b)

Fig. 7. Waveforms of $V_x$, $V_{gpi}$ and $V_{gni}$ (a) without optimal dead time adjustment and (b) with optimal dead time adjustment.

## 3. Measured results

The proposed buck DC–DC converter was implemented in the Chartered 2P4M 0.35 $\mu$m CMOS process and the area is about 1 × 1.4 mm$^2$. A chip photograph is shown in Fig. 6. The system component parameters are summarized in Table 2.

The width controller and dead time controller are two main techniques to improve the high-load efficiency. Figure 7 shows a comparison with and without optimal dead time adjustment. Figure 7(a) shows no dead time controller available, and the body-diode of the power NMOSFET is forward turned on. As the forward voltage is about 0.7 V, the voltage of $V_x$ is –0.7 V at the dead time. The current flow through the body-diode is the load current, and the loss is significant. It is helpful to utilize the optimal dead time controller to decrease it. Figure 7(b) is the waveform after the optimal dead time adjustment. The loss caused by the body-diode of the power NMOSFET is decreased greatly, so the efficiency of the buck DC–DC converter can be improved. An efficiency comparison with and without the dead time controller is shown in Fig. 8. Both of them use the width controller, and the results are measured under 3.6 V input and 1.8 V output at 10 MHz switching frequency. Figure 8 explains that the dead time controller can improve the efficiency 10% at 200 mA.

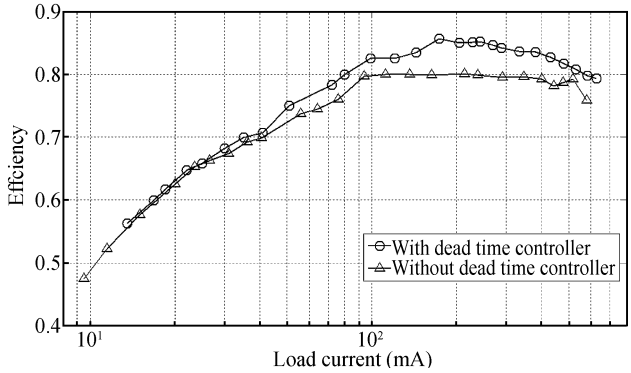



Fig. 8. Efficiency comparison with and without dead time controller.

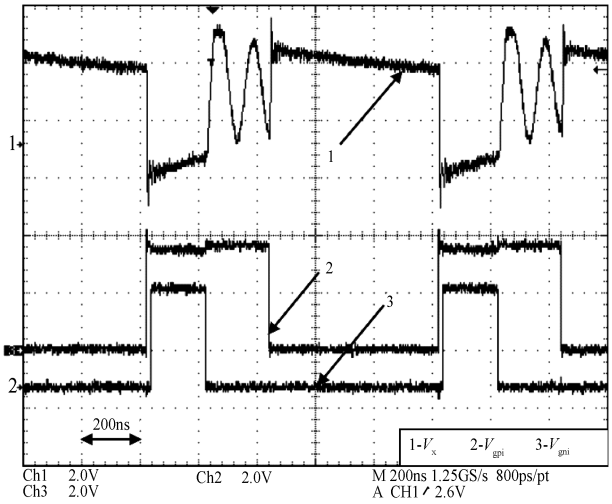



Fig. 9. Waveforms of $V_x$, $V_{gpi}$ and $V_{gni}$ at DCM mode.

At light load, the DCM controller and FSM controller are the main techniques to raise efficiency. Figure 9 shows the $V_x$ signal and the power MOSFET gate signals when the DCM controller is applied. When the current of the inductor becomes minus, the voltage of $V_x$ is larger than zero, and the DCM controller will make the gate signal of the power NMOSFET become "0". Because of the remaining charge on the filter capacitor, $V_x$ will oscillate due to the LC filter. Also, it is helpful to decrease the switching loss further, as $V_x$ is larger than zero when the power PMOSFETs are turned on. A comparison of the efficiency results of the buck DC–DC converter in DCM and CCM mode is shown in Fig. 10. It shows that at light load, DCM can improve the efficiency greatly.

The FSM controller is also used when the load current is lower than 100 mA, and the efficiency of the buck DC–DC converter is improved according to Fig. 10.

Figure 11 shows the improved efficiency by the proposed width controller, dead time controller, DCM controller and FSM techniques. Also, the efficiency of the buck DC–DC converter without any technique is presented. As shown in Fig. 11,

Table 3. Performance comparison between this work and reported literature.

| Parameter | Ref. [11] | Ref. [12] | Ref. [13] | Ref. [14] | This work |
|---|---|---|---|---|---|
| Topology | Buck | Buck | Buck | Buck | Buck |
| Year | 1997 | 2007 | 2008 | 2009 | 2010 |
| Process | 0.15 $\mu$m CMOS | 0.35 $\mu$m CMOS | 0.35 $\mu$m CMOS | 0.35 $\mu$m CMOS | 0.35 $\mu$m CMOS |
| $V_{in}$ (V) | 3.3 | 3.6 | 3.6 | 3 | 3.6 |
| $V_{out}$ (V) | 1.65 | 1.2 | 1.2 | 1.5 | 1.8 |
| $f_s$ (MHz) | 12.8 | 10 | 20 | 20 | 10 |
| $L$ ($\mu$H) | 0.1 | 1 | — | 0.421 | 0.47 |
| $C$ ($\mu$F) | 0.01 | 10 | — | — | 4.7 |
| Level of integration | External $L$, $C$ | External $L$, $C$ | External $L$, $C$ | External $L$, $C$ | External $L$, $C$ |
| Efficiency (%) | 75 | 78 | 72 | 82 | 86 |

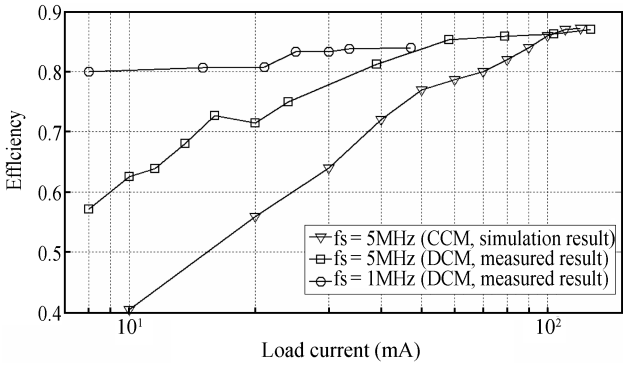



Fig. 10. Efficiency comparison between DCM and CCM ($V_{in}$ = 3.6 V, $V_{out}$ = 1.8 V).

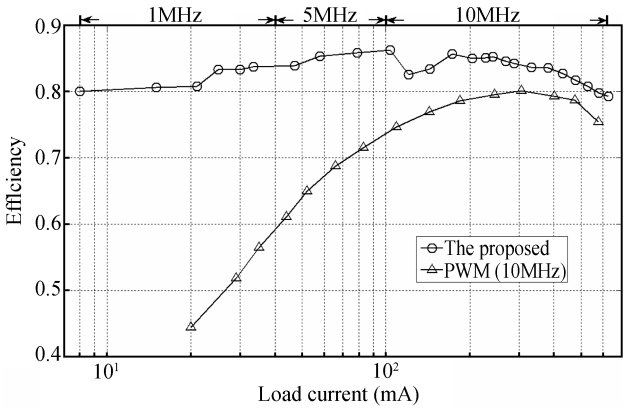



Fig. 11. Measured efficiency with and without proposed techniques ($V_{in}$ = 3.6 V, $V_{out}$ = 1.8 V).

the improvement efficiency is over 20% less than 50 mA and 4.5% larger than 100 mA.

Table 3 shows a comparison of previously reported DC–DC converters with tens of MHz switching frequency. It is obviously noted that the efficiency of 86% of this work is the highest in Table 3.

## 4. Conclusion

The analysis and design of a high frequency high efficiency buck DC–DC converter with a width controller, a dead time controller, a DCM controller and an FSM controller over a wide load range are discussed. The dead time controller can make the gate signals of the power NMOSFETs' dead time in proper time, and it can improve the efficiency of the high load more obviously. At different loads, the proposed buck DC–DC converter will be scalable in terms of the power MOSFETs' size and the switching frequency in the appropriate mode. Also, DCM will work when the current of the inductor becomes reverse. The efficiency of the proposed buck DC–DC converter is above 80% over a wide load range from 8 to 570 mA, and the peak efficiency of the buck DC–DC converter is 86% at 180 mA load current.

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