A 1.25 Gb/s laser diode driver with pulse width optimization*

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Abstract: A 1.25 Gb/s laser diode driver (LDD) with pulse width optimization has been implemented in a 0.6-μm BiCMOS process. This paper illustrates the relation between the pulse width distortion (PWD) of the output eye diagram and the driving amplitude from the second pre-amplifier. Also, a specific current setting circuit working together with an LDD is proposed to generate the optimum driving amplitude and to avoid device nonlinearity, temperature variation and process deviation. The measured results show a maximum crossing deviation of –3% and indicate the desired independence and stability.

Key words: LDD; PWD; crossing; BiCMOS
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1. Introduction

An LDD (laser diode driver) converts a current to an optical power together with an LD (laser diode) in optical communication systems. A typical LDD, shown in Fig. 1, includes two pre-amplifiers and an output stage. An eye diagram of the output current is always used to evaluate the LDD's performance. As is well known, PWD (pulse width distortion) will worsen the quality of the eye diagram, especially in a high speed data link. Among the factors leading to PWD, the most important one is the amplitude of the second pre-amplifier's output, marked v_{O2} in Fig. 1. The reason for this will be illustrated in the next section. The current source I_M, called the modulation current, is usually set by the user and has a typical range of 5–60 mA. So, the amplitude of v_{O2} should vary with different I_M to get a symmetric eye diagram and reduce PWD. To establish such a relation between v_{O2} and I_M, a general method is to make the driving current, marked I_D in Fig. 1, vary with different I_M[1−3]. The amplitude of v_{O2} should be large enough to switch the transistor M1 or M2 off. On the other hand, too large an amplitude will lead to serious PWD. Thus, the function between v_{O2} and I_M should be designed and optimized carefully. Unfortunately, such a relation always suffers from device nonlinearity, temperature variation and process deviation. The method of optimizing the function has not been presented in previous reports.

This paper illustrates the reason that PWD results from the mismatch between v_{O2} and I_M first. Then the mathematical relation between them is analyzed, and an appropriate expression is achieved to optimize the amplitude of v_{O2} according to different I_M. Based on such an expression, a novel circuit is proposed to generate the driving current I_D. It can guarantee that the amplitude of v_{O2} will be optimum at different I_M, regardless of device nonlinearity, temperature variation and process deviation. Such a circuit is adapted to implement a 1.25 Gb/s LDD, and the measured results are presented.

2. Circuit design

To find the reason why a large driving amplitude will lead to PWD, it is necessary to understand the characteristics of a differential amplifier. For convenient analysis, the output stage is simplified as shown in Fig. 2(a), where C_P is the parasitic capacitor and $v_{G1} - v_{G2} = v_{O2}$. It is supposed that the amplitude of v_{O2} is V_m, and its optimization value is $V_{m,opt}$. When $V_m = V_{m,opt}$, one transistor of the differential pair is switched on with an output current of I_M at $v_G = V_H$ while the other one is just switched off at $v_G = V_{L1}$. In this case, the rise and fall edges of the output current are synchronous and the waveforms are symmetric, as shown in Fig. 2(b). In particular, the crossing value of i_{O1} and i_{O2} is $0.5I_M$. In a high speed data link, crossing can indicate PWD to a certain extent. The condition of $V_m < V_{m,opt}$ is generally forbidden because the differential pair cannot be switched off. This working status will worsen the extinction ratio of output optical signals. If $V_m > V_{m,opt}$, on the other hand, the rise and fall edges of the output current become asynchronous and the waveforms are asymmetric, as shown in Fig. 2(c). Such asymmetry comes from the process as follows. It is supposed that the output high level of the second pre-amplifier remains constant with the value of V_H on different conditions. Therefore, the common-source voltage v_S holds at the same level even though the amplitude of v_{O2} increases,

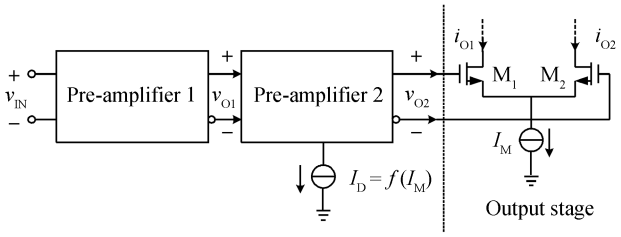

Fig. 1. Block diagram of a typical LDD.

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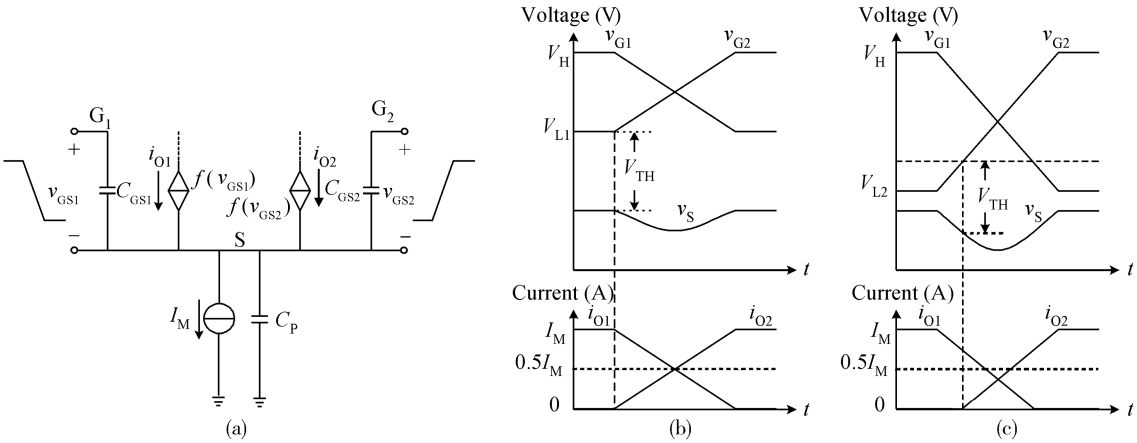

Fig. 2. (a) Simplified model of the output stage. (b) Waveforms when $V_m = V_{m,opt}$. (c) Waveforms when $V_m > V_{m,opt}$.

excluding the edge duration. Once v_{G1} falls, v_{GS1} decreases as well as i_{O1}. But i_{O2} remains at zero in spite of the increase of v_{GS2}. When v_{GS2} rises to V_{TH}, transistor M2 turns on and i_{O2} begins to rise. In the same way, transistor M1 is switched off before i_{O2} rises to I_M. Consequently, a large driving amplitude results in pulse asymmetry and crossing below 50%, which leads to undesired PWD. In addition, the presentation of C_P will worsen such asymmetry[4].

Apparently, an efficient means to achieve 50% crossing is to guarantee $V_m = V_{m,opt}$. It is known that the relation between the drain current i_D and the gate–source voltage v_{GS} of a MOSFET in saturation can be given by

$$v_{GS} = \sqrt{\frac{2i_D L}{\mu_n C_{OX} W}} + V_{TH}, \tag{1}$$

and v_{O2} in Fig. 1 can be expressed as

$$\begin{aligned} v_{O2} &= v_{GS1} - v_{GS2} \\ &= \sqrt{\frac{2L}{\mu_n C_{OX} W}}(\sqrt{i_{D1}} - \sqrt{i_{D2}}). \end{aligned} \tag{2}$$

If $i_{D1} = I_M$ and $i_{D2} = 0$, the optimum amplitude of v_{O2} is:

$$V_{m,opt} = \sqrt{\frac{2L}{\mu_n C_{OX} W} I_M} = V_{GS1} - V_{TH1}. \tag{3}$$

Obviously, $V_{m,opt}$ is nonlinear with I_M and is sensitive to temperature variation and process deviation. But Equation (3) also provides an approach to overcome these problems if a voltage directly proportional to $V_{GS1} - V_{TH1}$ can be achieved. To do this, a voltage generating circuit is proposed, shown in Fig. 3. If the transistors have the same geometric dimensions and R_S is sufficiently large, the generated voltage, marked V_O in Fig. 3, can be derived as follows:

$$V_O = V_{GS3} - V_{GS4} = V_{GS3} - V_{TH4}. \tag{4}$$

Comparing Eq. (4) with Eq. (3) yields $V_O \approx V_{m,opt}$ if the parameters, such as I_M/I_1 and $(W/L)_1/(W/L)_3$, are appropriate. However, the body-effects of M1 and M4 are different. Thus, the corresponding V_O should be revised to be:

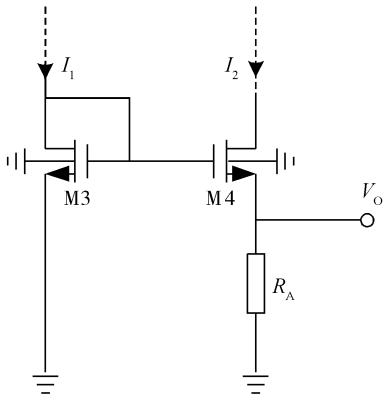

Fig. 3. Schematic of the circuit to generate $V_{GS1} - V_{TH}$.

$$\begin{aligned} V_O &= \sqrt{\frac{2I_1(L/W)_3}{\mu_n C_{OX}}} - \gamma(\sqrt{2|\phi_F| + V_{SB,M4}} - \sqrt{2|\phi_F|}) \\ &= \sqrt{\frac{2I_1(L/W)_3}{\mu_n C_{OX}}} - \Delta V_{TH}, \end{aligned} \tag{5}$$

where γ is the body-effect coefficient and ϕ_F is the surface potential in strong inversion. If $I_M/I_1 = (W/L)_1/(W/L)_3$, the generated V_O is therefore:

$$V_O = \sqrt{\frac{2(L/W)_1}{\mu_n C_{OX}} I_M} - \Delta V_{TH}. \tag{6}$$

Compared with Eq. (3), this expression indicates that the generated V_O is approximately equal to $V_{m,opt}$ with a mere error of ΔV_{TH}. Moreover, such an error can be compensated easily.

To achieve the pulse waveform $v_{O2,opt}$, an efficient approach is to convert the DC voltage V_O to a DC current first and then this current should be modulated by an input high-speed pulse. A current setting circuit, shown in Fig. 4, is proposed to implement the first conversion. According to the circuit, the output current I_D for the second pre-amplifier is given by

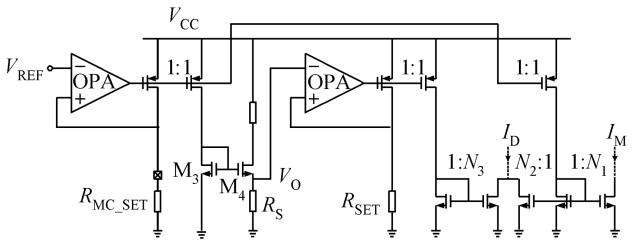

Fig. 4. Schematic of the current setting circuit.

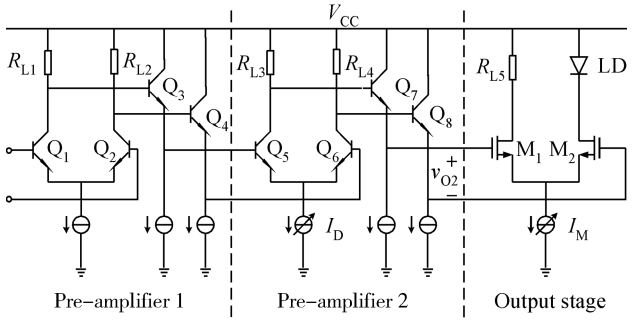

Fig. 5. Schematic of the LDD.

$$I_D = N_3\frac{V_O}{R_{SET}} + N_2\frac{V_{REF}}{R_{MC\_SET}} = N_3\frac{\sqrt{\dfrac{2(L/W)_1}{\mu_n C_{OX}}I_M} - \Delta V_{TH}}{R_{SET}} + \frac{N_2}{N_1}I_M. \quad (7)$$

The modulation is implemented by the LDD, shown in Fig. 5. The current sources I_D and I_M are set by the circuit shown in Fig. 4. If $R_{L3} = R_{L4} = R_{SET}/N_3$, the amplitude of v_{O2} can be expressed as

$$V_m = \sqrt{\frac{2(L/W)_1}{\mu_n C_{OX}}I_M} - \Delta V_{TH} + \frac{N_2 R_{SET}}{N_3 N_1}I_M. \quad (8)$$

Ultimately, the conclusion of $V_m \approx V_{m,opt}$ can be achieved just on the condition that

$$\Delta V_{TH} = \frac{N_2 R_{SET}}{N_3 N_1}I_M. \quad (9)$$

In fact, such a configuration compensates the different body-effects from M3 and M4 in Fig. 3.

To verify the above derivation, the amplitude of v_{O2} and its optimization value, expressed as V_m and $V_{m,opt}$ respectively, are simulated in SmartSpice. $V_{m,opt}$ is directly determined by the differential pair of the LDD's output stage. At different temperatures, the corresponding V_m and $V_{m,opt}$ according to different I_M are shown in Fig. 6. It is seen that the generated V_m through the accuracy current setting is nearly equal to the optimum value $V_{m,opt}$, required by the output stage. This conclusion is almost independent of temperature or I_M. Actually, it is also independent of process, which is not presented for the limited length.

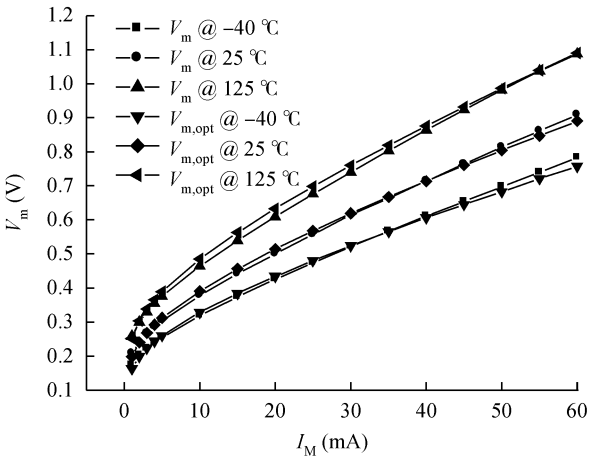

Fig. 6. Simulated V_m and $V_{m,opt}$ at different temperatures.

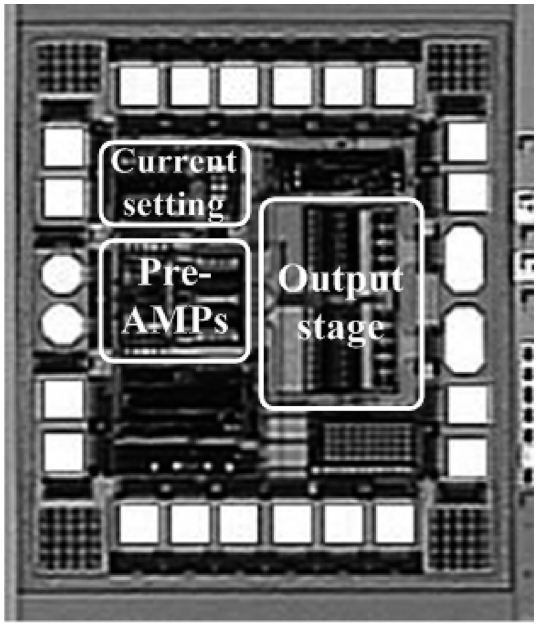

Fig. 7. Die photograph of the LDD.

3. Measured results

The proposed LDD with pulse width optimization has been implemented in a 0.6-μm BiCMOS process, operating up to 1.25 Gb/s. The die photograph is shown in Fig. 7. Such an LDD has been measured together with a transmitter optical subassembly (TOSA) and other off-chip components. With 3.3 or 5 V supply, the current consumption is 35–40 mA according to different I_M, excluding output modulation current.

Figure 8 is the measured crossing of the optical eye diagram. It shows a −3% deviation and represents the PWD. The upper current is less than 45 mA just for safety considerations. The output eye diagrams at different temperatures are presented in Figs. 9(a) and 9(b), respectively. The results show a 20%–80% rise time of about 280 ps, as well as the fall time. Thus, the PWD indicated by the crossing deviation is satisfied for most applications. The measurement at 85 ℃ is implemented together with on-chip automatic temperature compensation. So, the eye diagrams in Figs. 9(a) and 9(b) are achieved

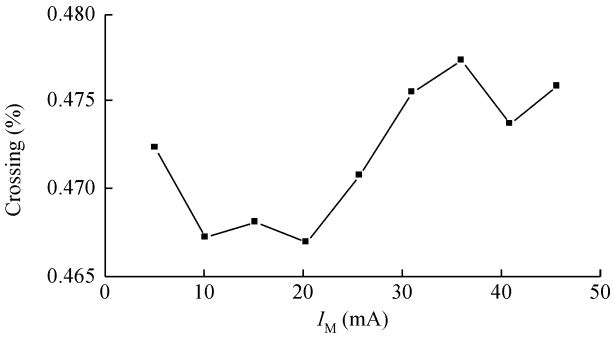

Fig. 8. Crossing of the optical eye diagram.

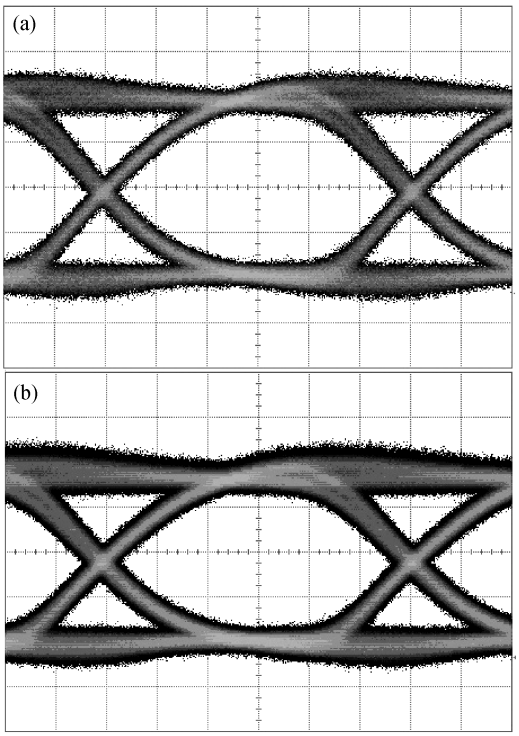

Fig. 9. (a) 1.25 Gb/s optical eye diagrams at 25 ℃, 99 μW/div, 132 ps/div. (b) 1.25 Gb/s optical eye diagrams at 85 ℃, 107 μW/div, 131 ps/div.

Table 1. Summarized performance of the LDD.

Parameter	Value	Condition
Supply range	3–5.5 V	
Current consumption	35–40 mA	R_{MC_SET} = 5–60 kΩ
Output current range	5–60 mA	R_{MC_SET} = 5–60 kΩ
Differential input voltage	0.3–2 V	
Rise time	280 ps	20%–80%
Fall time	280 ps	20%–80%
Crossing	47%	I_M = 18 mA, 25 ℃
Input impedance	5 kΩ	

with different I_M. The detailed performance is summarized in Table 1.

4. Conclusion

A 1.25 Gb/s LDD with pulse width optimization has been implemented in a 0.6-μm BiCMOS process. The optimization focuses on the relation between PWD and driving amplitude from the second pre-amplifier. Such an amplitude should vary with modulation current, temperature variation and process deviation. A specific current setting circuit is proposed to associate the driving current I_D with the modulation current I_M. Finally, the optimum driving amplitude is generated together with the high-speed modulator. The measured results show a maximum crossing deviation of –3% and indicate the desired independence and stability.

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