A 0.5–1.7 GHz low phase noise ring-oscillator-based PLL for mixed-signal SoCs

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Abstract: This paper describes the design of a fully integrated low phase noise CMOS phase-locked loop for mixed-signal SoCs with a wide range of operating frequencies. The design proposes a multi-regulator PLL architecture, in which every noise-sensitive block from the PLL top level is biased from a dedicated linear or shunt regulator, reducing the parasitic noise and spur coupling between different PLL building blocks. Supply-induced VCO frequency sensitivity of the PLL is less than 0.07%-f_{vco}/1%-V_{DD}. The design is fabricated in 0.13 μm 1.5/3.3 V CMOS technology. The in-band phase noise of –102 dBc/Hz at 1 MHz offset with a spur of less than –45 dBc is measured from 1.25 GHz carrier. The measured RMS jitter of the proposed PLL is 1.72 ps at a 1.25 GHz operating frequency. The total power consumption is 19 mW, and its active area is 0.19 mm^2.

Key words: phase-locked loop; phase noise; regulator; ring oscillator; CMOS
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1. Introduction

Phase-locked loops (PLL) are widely used in high performance mixed-signal systems ranging from clock generation to clock recovery and frequency synthesis. There are stringent requirements in timing jitter or phase noise in such applications. Moreover, small area is preferred. This makes the ring oscillator a perfect candidate. Its main advantages are a very small die area, which reduces the IC cost and also helps minimize the substrate noise and spur coupling, and a wide tuning range. The larger internal phase noise of a ring oscillator compared with its LC oscillator counterpart requires a higher loop bandwidth to comply with the stringent phase noise specifications.

VCO is one of the critical components in PLLs, and is becoming the bottleneck in the design of high performance PLLs. The fundamental limit on noise is thermal noise, but it is not the dominant source of noise in practical VCOs[1]. To achieve low phase noise performance, care must be taken to minimize the sensitivity of frequency to high frequency power supply variations. Two methods are usually used to improve the supply-noise rejection. The first method employs compensation[2, 3]. However, due to process variation and dependence of the compensation on the oscillation frequency, it is practically impossible to achieve accurate compensation. The other method employs voltage regulators[4, 5] at the cost of reduced voltage headroom, which could be overcome by making good use of dual gate oxide devices provided by modern deep-submicron CMOS processes. The present design takes advantage of both device types, accompanied with certain circuit techniques and power supply regulation methods for reducing the phase noise and spurious tones, to optimize the overall PLL phase noise performance.

2. PLL design

The PLL is based on the classic charge-pump topology. Two separate supplies are used to minimize the coupling between digital and analog building blocks. Figure 1 shows the PLL top level diagram with power supply partition and regulation. The charge-pump and VCO are biased from a high PSRR linear regulator which prevents supply spur coupling to the sensitive PLL nodes. The regulator works off a 3.3 V analog supply and produces a constant supply V_{Reg1} of approximately 2.5 V. So it can provide large VCO control voltage compliance, which helps reduce the VCO gain, and hence the reference induced spur. PFD and level-shifter are biased from a shunt regulator, which protects the analog supply contamination from large current spikes. The analog to digital interface is selected at the divider output node. The digital part works off 1.5 V supply as 1.5 V core transistors give the fastest switching speed which reduces the effects of both the device internal noise and the supply-injected noise in the dividers. By using differential current-steering charge-pump architecture[6], which gives a current switching time lower than 100 ps, the charge-pump transfer function is dead-zone free (verified by simulation). The charge pump current is adjustable and it follows the change of the reference frequency. As a result, an appropriate loop gain and bandwidth could be maintained. The reference spur has been reduced by using a third order loop filter and minimizing charge sharing and clock feed through in the charge pump. The output signal of the VCO passes through a low-to-full swing amplifier as proposed in Ref. [7], which generates single-end 50% duty cycle CMOS level clock signals and feeds back to the PFD through a frequency divider.

2.1. Phase-frequency detector and shunt regulator design

The PFD compares the phases of the reference and feedback clocks and then generates the UP/DOWN signals that switch the current of the charge pump. The ideal PFD's characteristic is linear in the entire range of input phase difference from -2π to 2π. So the frequency will monotonically approach the lock-in range during acquisition. However, due to the delay of the reset path, the linear range is less than 4π. How the

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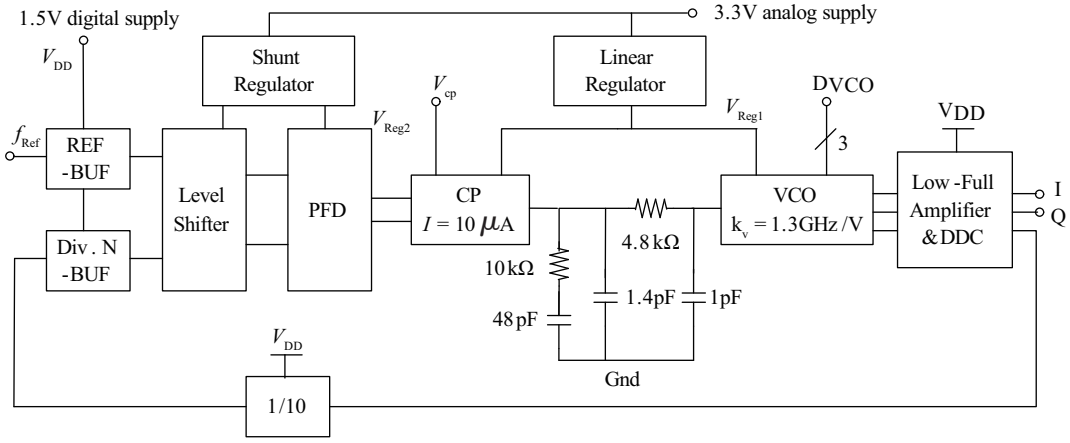

Fig. 1. PLL block diagram including supply partition and regulation.

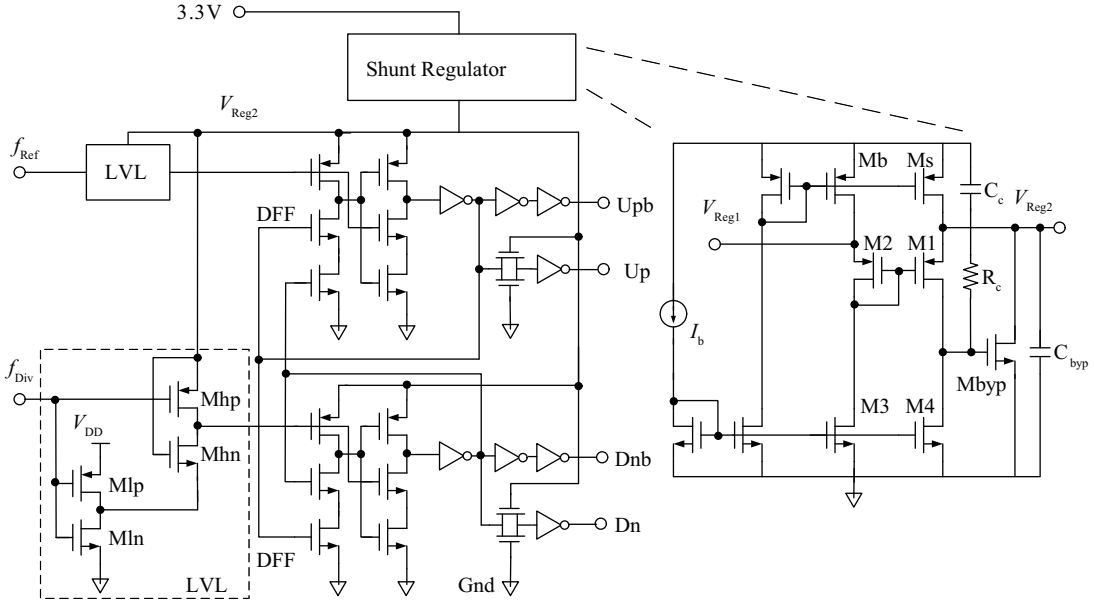

Fig. 2. Phase-frequency detector biased with shunt regulator.

nonideal effect influences frequency acquisition will be illustrated as follows. In the situation of the reference clock leading the feedback clock, a UP output is caused. As the input phase difference nears 2π, the next leading edge arrives before the DFFs are reset due to the finite reset delay. The reset overrides the new f_{Ref} edge and does not generate the UP signal, and the following feedback clock edge causes a DOWN signal. Because the nonideal PFD gives the wrong information periodically, the frequency will not monotonically approach lock-in range during acquisition. The acquisition slows by how often the wrong information occurs, which depends on t_{reset}/T_{Ref}[8]. On the other hand, the device noise current generated by the charge pump and supply injected noise only impacts the VCO control voltage when both UP/DOWN charge pump current are ON during each clock cycle. Therefore, the PFD needs to have a small reset delay, which requires minimum stages of logic gates in the PFD signal path. The PFD shown in Fig. 2 consists of two true single-phase clock (TSPC) D-flip-flops (DFFs) and feedback NAND gates, which are used to generate the reset signal and are merged in the DFF structure. This results in three gate delays in the reset path while the widely used seven-NAND implementation has a delay of seven gates' propagation time. A reset time of approximately 250 ps is achieved when using thick gate transistor DFFs.

Both the PFD input clocks and its internal signals are square waves with high edge slew rate, causing large supply current spikes. If the responded reference ripple is coupled in noise sensitive analog blocks, the PLL reference spur performance may seriously degrade. A shunt regulator is used as presented in Fig. 2. The shunt regulator acts as a constant current load of the analog supply. The current mirrors formed by transistors M1–M2 and M3–M4 force the output voltage V_{Reg2} to be equal to the charge pump supply voltage V_{Reg1}. Consequently, perfect digital logic signal level matching between the PFD and the charge pump is achieved. With the M1/Mbyp feedback loop, the regulated voltage V_{Reg2} remains constant on the appearance of load current spikes. When the load current becomes larger, the output voltage V_{Reg2} turns down, and the variance is amplified by M1, which is operating as a common-gate amplifier. So the gate–source voltage of Mbyp gets lower

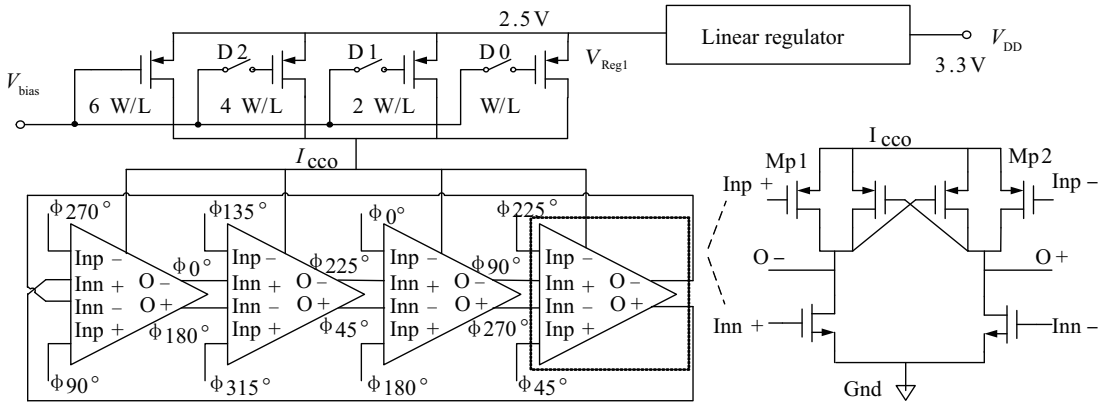

Fig. 3. Ring-oscillator structure with dual-delay paths.

and thus the transistor Mbyp consumes less current. As a result, V_{Reg2} goes back to its normal voltage level. An RC compensation circuit is adopted to maintain a good phase margin of the feedback loop. A local bypass capacitor is added to reduce voltage ripple introduced by high frequency switching of the digital load current.

2.2. VCO design

The VCO, which decides the out-band phase noise, is the most important component in a PLL. The proposed VCO is composed of a voltage to current (V–I) converter, a current controlled oscillator (CCO), and a high PSRR linear regulator as shown in Fig. 3. The V–I conversion is done by an NMOS transistor which has been linearized by the source-degeneration resistor. The CCO uses a dual-delay path scheme, including a negative skewed delay path and a normal delay path[9]. Therefore, high operating frequency and wide tuning range are achieved simultaneously. The delay cell of each stage is based on a cascade voltage switch logic (CVSL) differential inverter[10]. A pair of PMOS transistors, Mp1 and Mp2, is added to the PMOS load, which is used to take the negative skewed signals. Differential implementation is preferred for any analog circuit in a system-on-chip kind of environment. Supply, substrate or any other coupling noise are thought as common mode sources and have little effect on differential signals. Further power supply rejection is achieved by biasing the VCO from a high PSRR linear voltage regulator similar to that proposed in Ref. [11].

To verify the noise performance of the VCO, the dynamic response of VCO frequency to supply noise is simulated. The curves 1 and 4 (solid line) shown in Fig. 4 illustrate the transient frequency response of the VCO without and with the voltage regulator, when a –10%-V_{DD} step with 100-ps slope time is inserted at t = 5 ns. Adding the regulator to the VCO decreases the supply sensitivity of the VCO frequency (defined by Ref. [2]) from 0.43%-f_{VCO}/1%-V_{DD} to 0.07%-f_{VCO}/1%-V_{DD} for very high frequency noise. When increasing the slope time of the V_{DD} from 100 ps to 1 ns and 5 ns (curves 5 and 6), supply sensitivities of 0.07%-f_{VCO}/1%-V_{DD} and 0.06%-f_{VCO}/1%-V_{DD} are achieved respectively. Also, the static sensitivity is improved from 0.1%-f_{VCO}/1%-V_{DD} to 0.006%-f_{VCO}/1%-V_{DD}.

The VCO tuning gain plays a crucial role in a PLL. It should be as low as possible to reduce the noise contribution of the

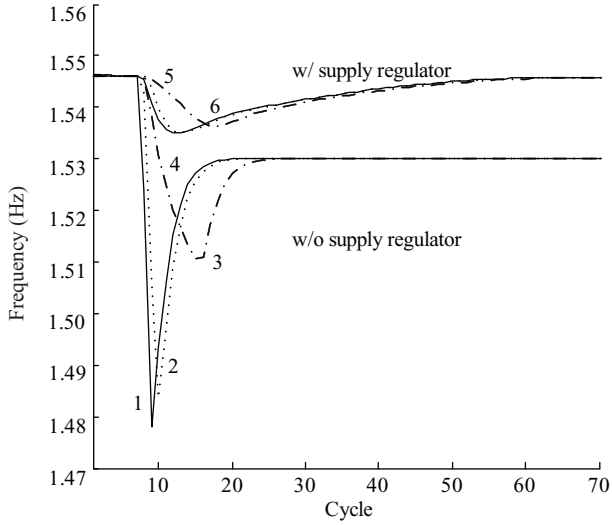

Fig. 4. VCO frequency response to –10%-V_{DD} step.

PLL front-end stages and coupled spurious tones. Otherwise, it needs to be large enough to cover the entire frequency range required by communication standards and to compensate for the process, temperature, and supply (PVT) variations. To optimize the PLL for low phase noise, the proposed VCO achieves a moderate average VCO gain of 1.3 GHz/V and a frequency range of 0.5–1.7 GHz by using an open loop digital calibration method as shown in Fig. 3. The simulated VCO frequency tuning range across the process corners is shown in Fig. 5, while the digital input D [2:0] is set to "010".

Table 1 is a summary of the performance comparison between the proposed multi-regulator PLL and prior state-of-the-art designs. The first two designs, by Ingino[4], are examples of supply regulated VCOs, whereas the designs by Mansuri[2] and Wu[3] are examples of noise compensation VCOs. The VCO proposed by Ingino achieves excellent dynamic supply sensitivity by coupling the V_{DD} to ground with a very large capacitor of 1.2 nF and higher power consumption. The design of Wu achieves a close to zero supply sensitivity by initial calibration after the system has powered up, but a temperature variation from 27 to 120 ℃ would worsen the supply sensitivity by –0.25%-f_{VCO}/1%-V_{DD}. Besides, this work achieves better static noise rejection than the VCO in Ref. [2].

Table 1. Performance comparison of the proposed PLL with prior state-of-the-art designs.

Parameter	Ingino, JSSC'01[4] 0.15 μm, 1.2/3.3 V	Mansuri, JSSC'03[2] 0.25 μm, 2.5 V	Wu, JSSC'07[3] 0.13 μm, 1 V	This work 0.13 μm, 1.5/3.3 V
Power (mW)	130 @ 4 GHz	10 @ 1 GHz	9.6 @ 1.4 GHz	19 @ 1.25 GHz
Active area (mm^2)	1.48	0.028	0.064	0.19
VCO frequency range (GHz)	0.8–4	0.2–2	0.5–2	0.5–1.7
Jitter w/o V_{DD} noise (ps)	49	28.89	30	11.11
P2P, rms (ps)	8.36	3.28	3.9	1.72
Static sensitivity (%-f_{VCO}/%-V_{DD})	0.007/1	0.03/1	Close to zero	0.006/1
Dynamic sensitivity (%-f_{VCO}/%-V_{DD})	0.007/1	0.07/1		0.07 / 1

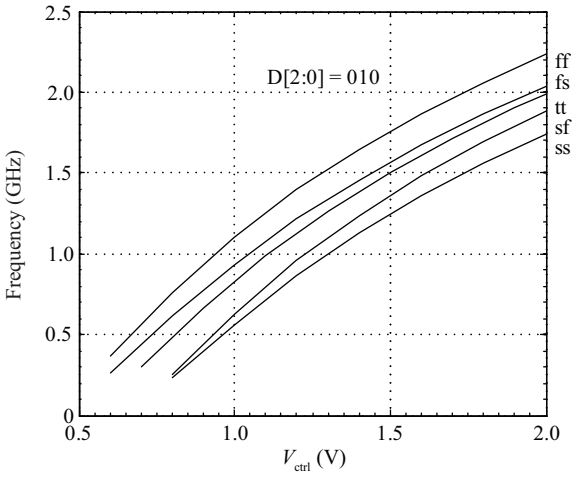

Fig. 5. Simulated VCO frequency characteristic.

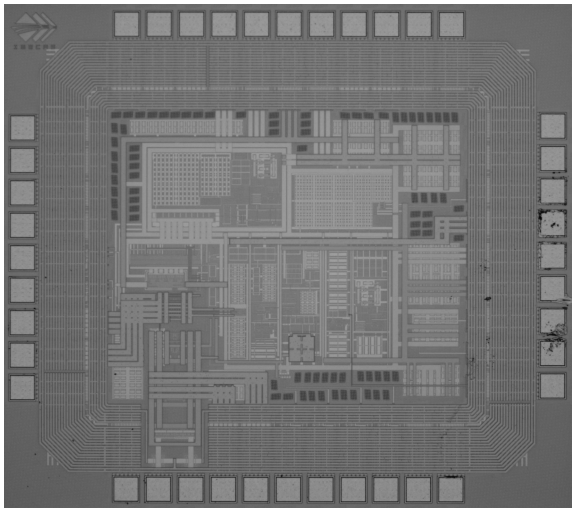

Fig. 6. Microphotograph of the PLL.

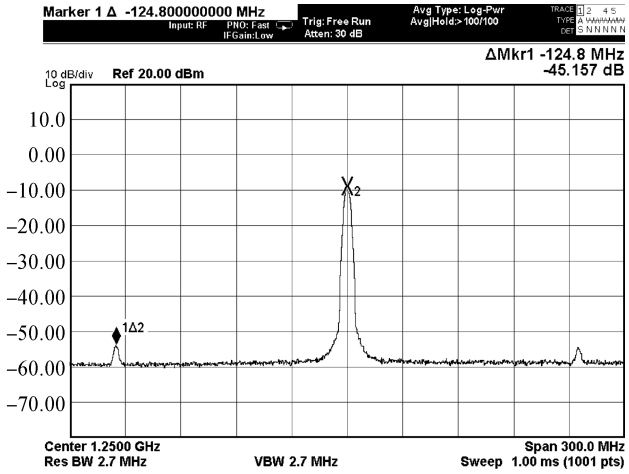

Fig. 7. Output spectrum of the PLL.

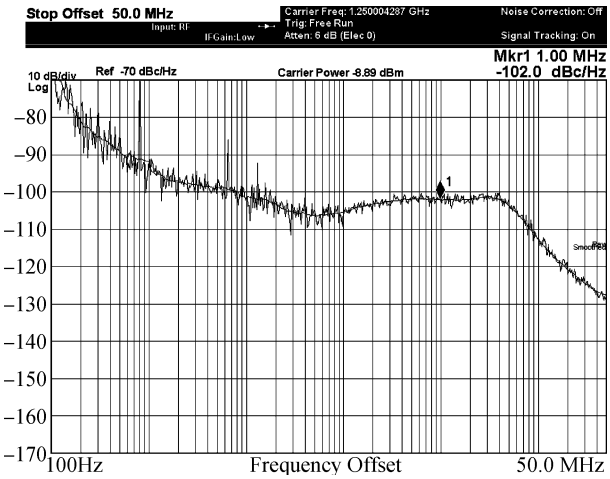

Fig. 8. Measured phase noise of the PLL.

3. Measurement result

The multi-regulator ring-oscillator-based PLL was fabricated in 0.13 μm CMOS technology. All capacitors, including regulator decoupling capacitors and the PLL's loop filter capacitors, are implemented with MOS capacitors. A microphotograph of the fabricated PLL is shown in Fig. 6. The active area is approximately equal to 0.19 mm^2. The prototype has been tested with input reference frequency of 62.5 MHz, 125 MHz and 156.25 MHz, while the loop multiplication factor is ten. The measured output spectrum of 1.25 GHz is shown in Fig. 7, which presents a reference spur level less than –45 dBc. Figure 8 shows the phase noise of the prototype. As mentioned before, the phase noise is –102 dBc/Hz at 1MHz offset from the 1.25 GHz carrier. The jitter performance of the PLL output at 1.25 GHz is demonstrated in Fig. 9. The jitter histogram measures the RMS jitter at 1.72 ps and peak-to-peak jitter at

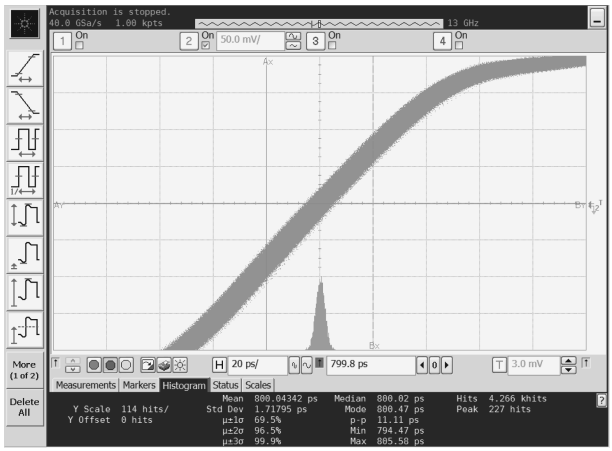

Fig. 9. PLL output jitter histogram at 1.25 GHz.

11.11 ps without supply noise. The power consumption excluding that of the output buffer is 19 mW. The power consumption and the area of the test chip are bigger than the design proposed in Refs. [2, 3], which is a common disadvantage of supply regulated VCOs as that of Refs. [4, 5]. Nevertheless, the compensation method used by Refs. [2, 3] suffers from strong dependence on oscillation frequency and PVT variations. The proposed method is more practical. In fact, most of the area is occupied by regulator decouple capacitors and loop filter capacitors. So the area could be sharply reduced by employing a capacitance multiplier technique in the loop filter design. Further simulation indicates that there is voltage headroom for the proposed circuit, and the power consumption of the circuit could be reduced by lowering the supply voltage.

4. Conclusion

This paper presents a multi-regulator PLL architecture aimed at supply noise and spur rejection, especially for a PLL in mixed signal SoCs. With the help of a shunt regulator, all supply current spikes generated by digital blocks are closed locally, while all sensitive analog blocks are biased from a high PSRR linear regulator to enhance noise rejection. Phase noise performance is further improved by using a full swing differential ring oscillator. A wide operating frequency range over all PVT is obtained by using a dual-delay path scheme and digital calibration techniques in the VCO. Experimental results demonstrate that the proposed PLL is a good solution to improve noise rejection.

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