Deep submicron PDSOI thermal resistance extraction*

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Abstract: Deep submicron partially depleted silicon on insulator (PDSOI) MOSFETs with H-gate were fabricated based on the 0.35 μm SOI process developed by the Institute of Microelectronics of the Chinese Academy of Sciences. Because the self-heating effect (SHE) has a great influence on SOI, extractions of thermal resistance were done for accurate circuit simulation by using the body-source diode as a thermometer. The results show that the thermal resistance in an SOI NMOSFET is lower than that in an SOI PMOSFET; and the thermal resistance in an SOI NMOSFET with a long channel is lower than that with a short channel. This offers a great help to SHE modeling and parameter extraction.

Key words: thermal resistance; self heating effect; PDSOI
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1. Introduction

Reduced body effects, freedom from latch-up, and excellent soft-error immunity have made silicon-on-insulator (SOI) technologies very attractive for future high-speed operation of complementary metal–oxide–semiconductor field effect transistors (CMOSFETs)[1]. SOI MOSFETs also offer significant power reduction as compared with bulk MOSFETs due to the reduced parasitic capacitance. Meanwhile, the low thermal conductivity of the thick buried oxide inhibits cooling of SOI devices, leads to the rise of the temperature, and causes a severe self-heating-effect (SHE)[2, 3]. This may degrade the carrier mobility, increase the junction leakage, enhance the impact ionization rate, and cause negative differential conductance in the saturation region[4]. It should be noted that SHE is significant in the DC characteristics when the device power dissipation is high, but it will disappear at high frequency. Therefore, we should extract the SHE parameters for accurate circuit simulation[5].

In BSIMSOI4.0, SHE is modeled by an auxiliary $R_{\rm th}C_{\rm th}$ circuit as shown in Fig. 1. The temperature node (T node) will be created in SPICE simulation if the self-heating selector shMod is ON and the thermal resistance ($R_{\rm th}$) is non-zero. The T node is treated as a voltage node and is connected to ground through a thermal resistance $R_{\rm th}$ and a thermal capacitance $C_{\rm th}$. Although an analytical model of $R_{\rm th}$ is provided by Ref. [6], $R_{\rm th}$ in fact strongly depends on technology and therefore needs to be characterized experimentally for each technology. There have been some methods to extract $R_{\rm th}$, such as using a polysilicon gate as a temperature-sensing resistor or PIV, and these methods need a new test structure or valuable test equipment. In this paper, $R_{\rm th}$ is extracted using the body-source diode as a thermometer. $R_{\rm th}$ of an SOI NMOSFET is compared with that of an SOI PMOSFET, and also that of SOI NMOSFETs with different channel lengths. Unfortunately, $C_{\rm th}$ is not referred to in this paper.

2. Experiment

PDSOI MOSFETs with H-gate were fabricated using the 0.35 μm SOI process developed by the Institute of Microelectronics of the Chinese Academy of Sciences (IMECAS). They were fabricated on UNIBOND SOI wafers. The thickness of the buried oxide, the top silicon film and the gate oxide is 400 nm, 175 nm and 13 nm, respectively. Local oxidation of silicon (LOCOS) was performed to fully consume the active silicon layer in the isolation region. Arsenic was implanted at an energy of 100 keV to form the source/drain. $TiSi_2$ was formed in the source/drain region.

The body-source diode is used as a thermometer to extract $R_{\rm th}$, and $R_{\rm th}$ is shown as[7]

$$R_{\rm th} = \frac{\Delta\text{Temperature}}{\Delta\text{Power}} = \frac{\mathrm{d}(\lg I_{\rm bs})/\mathrm{d}P}{\mathrm{d}(\lg I_{\rm bs})/\mathrm{d}T}. \quad (1)$$

Firstly, we test the current of the body-source diode ($I_{\rm bs}$) at different powers with the bias configuration presented in Fig. 2. To prevent the influence of the body-drain diode, the body-drain diode is backward biased. We can get linebreak $\mathrm{d}(\lg I_{\rm bs})/\mathrm{d}P$ from this test. Actually, the change of $I_{\rm bs}$ in this test is caused by the rise of temperature, which is the result of the low thermal conductivity of the thick buried oxide. Then, we test $I_{\rm bs}$ at different temperatures with the bias configuration presented in Fig. 3. Because the body-drain diode current also flows through the body, we measure $I_{\rm bs}$ from the source end. We can get $\mathrm{d}(\lg I_{\rm bs})/\mathrm{d}T$ from this test. Then $R_{\rm th}$ is calculated from Eq. (1). Normalized thermal resistance ($R_{\rm th0}$) can be found by $R_{\rm th0} = R_{\rm th}W$ based on BSIMSOI4.0. It should be no-

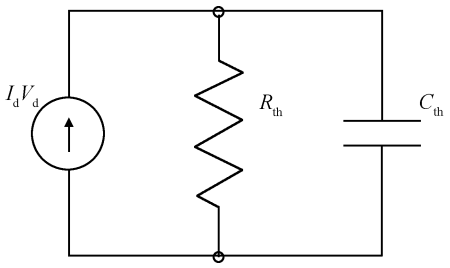

Fig. 1. Equivalent circuit for self-heating simulation.

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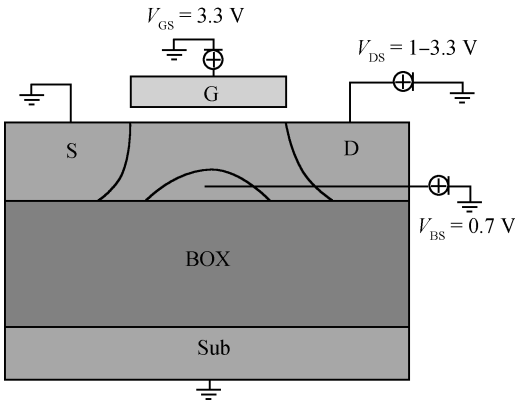

Fig. 2. Bias configuration for d(lg I_{bs})/dP.

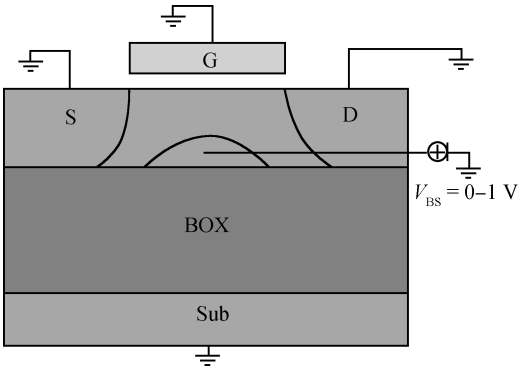

Fig. 3. Bias configuration for d(lg I_{bs})/dT.

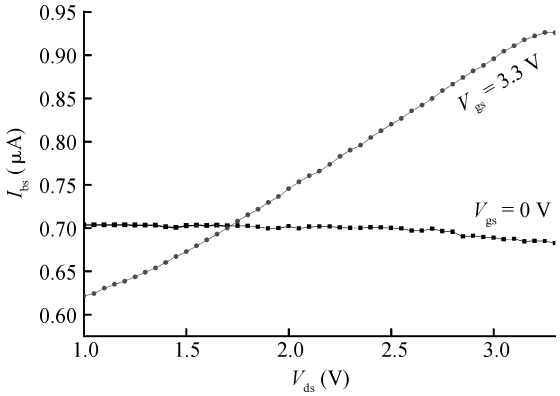

Fig. 4. I_{bs} at different V_{gs}.

ticed that the voltage between body and source (V_{BS}) should be the same in the calculations of d(lg I_{bs})/dP and d(lg I_{bs})/dT, and it is 0.7 V in this paper.

3. Results and discussions

If the device is biased as in Fig. 2, the parasitic BJT will work, and this will influence the measurement of I_{bs}. To prove that the change of I_{bs} is mainly caused by the power dissipation of the device, we compared I_{bs} between V_{GS} = 0 V and V_{GS} = 3.3 V, as shown in Fig. 4. This demonstrates that the parasitic BJT has little influence on I_{bs}. The reason that I_{bs} is higher at V_{GS} = 0 V than V_{GS} = 3.3 V when V_{DS} is low is that high V_{GS} degrades the carrier mobility.

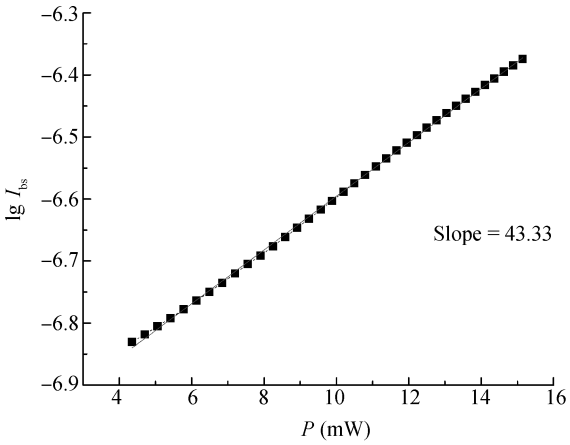

Fig. 5. I_{bs} at different powers.

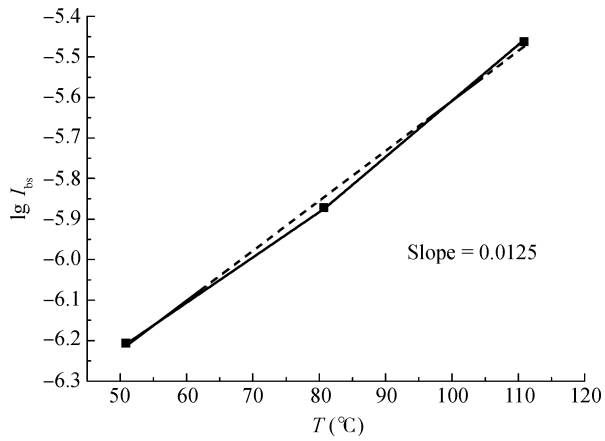

Fig. 6. I_{bs} at different temperatures.

Figure 5 shows the I_{bs} at different powers of an SOI NMOS, and the channel width and length are 20 μm and 0.8 μm, respectively. We can get d(lg I_{bs})/dP from the slope of this line. Figure 6 shows the I_{bs} at different temperatures, and then d(lg I_{bs})/dT is obtained from the slope of this line. From Eq. (1), we can figure out that R_{th} of this device is 3466.19 ℃/W, and R_{th0} based on this device is 0.0693 m℃/W. We have also extracted the R_{th} of an SOI PMOS with the same channel width and length. R_{th} is 3987.50 ℃/W and R_{th0} is 0.0798 m℃/W. So we can easily find that R_{th0} of NMOS is lower than PMOS. The reason for this is that the channel doping of NMOS is higher than PMOS. However, the power of NMOS is much higher in the saturation region than PMOS due to the high mobility of electrons, so the SHE of NMOS is much more severe than PMOS; this is tested by our experiments and is shown in Fig. 7.

Because $R_{th0} = R_{th}W$ in BSIMSOI4.0, it means R_{th0} has nothing to do with channel length. But that is not the case in our experiments. Table 1 shows the R_{th} and R_{th0} of devices with different channel lengths. It indicates that the longer the channel is, the lower the R_{th0} is. For the devices with H gate, the body contact provides a way to dissipate heat. The devices with longer channels have more body contacts, so the R_{th0} based on the devices with longer channels is lower. Therefore, it is essential to add the parameter L in the calculation of R_{th}, and this

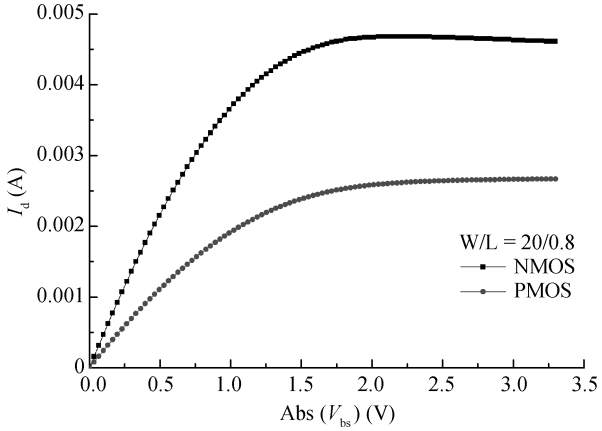

Fig. 7. SHE of NMOS and PMOS with the same W/L.

Table 1. R_{th} and R_{th0} based on devices with different channel lengths.

W/L	10/0.8	10/1.2	10/5
R_{th} (℃/W)	6396.80	2202.49	2047.06
R_{th0} (m℃/W)	0.0640	0.0220	0.0205

can be achieved in the model card by using the Macro model.

4. Conclusion

In this paper, R_{th} and R_{th0} of MOSFETs fabricated based on the 0.35 μm SOI process developed by IMECAS have been extracted by using the body-source diode as a thermometer. The results indicate that R_{th} of NMOS is lower than PMOS in our process, and R_{th} of devices with long channels is lower than those with short channels. This work offers a great help to SHE modeling and the extraction of SHE model parameters.

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