A reconfigurable OTA-C baseband filter with wide digital tuning for GNSS receivers*

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Abstract: The design of a digitally-tunable sixth-order reconfigurable OTA-C filter in a 0.18-μm RFCMOS process is proposed. The filter can be configured as a complex band pass filter or two real low pass filters. An improved digital automatic frequency tuning scheme based on the voltage controlled oscillator technique is adopted to compensate for process variations. An extended tuning range (above 8:1) is obtained by using widely continuously tunable transconductors based on digital techniques. In the complex band pass mode, the bandwidth can be tuned from 3 to 24 MHz and the center frequency from 3 to 16 MHz.

Key words: reconfigurable filter; wide tuning; digital frequency tuning
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1. Introduction

In recent years, research on global navigation satellite systems (GNSS) has seen rapid progress. There are four main satellite systems: GPS, Galileo, GLONASS and Chinese Compass. These four satellite systems have different carrier frequencies and signal bandwidths, and each system has its own narrowband signal for civilian use and wideband signal for military use. Developing a multimode configurable radio receiver that can receive signals from all the systems is the direction of the present research. A multimode configurable radio receiver demands a reconfigurable and widely tunable baseband filter which is described in this work.

In order to satisfy the increasing demands of low cost, low power and higher level of integration, the receiver is implemented in a 0.18-μm RFCMOS process. The receiver architecture in this work is a combined zero-IF/low-IF receiver architecture as this architecture is suitable for a highly adaptable and flexible radio[1]. This approach is based on the existence of common functional elements between the direct conversion and the low-IF architectures. The zero-IF receiver architecture is intended for wideband signals, and the low-IF architecture is intended for both narrowband signals and wideband signals. Apart from a different local oscillator frequency, the relevant difference between the two architectures is in the IF filtering stage: a pair of low-pass filters are needed for the zero-IF and a complex band pass filter are required for the low-IF. Incorporating the constructive units of the two low-pass filters to construct a complex band-pass filter offers the advantage of reusing common hardware elements and leads to a highly adaptable circuit structure.

Section 2 presents the design of a reconfigurable OTA-C filter. The filter needs an adaptable bandwidth and center frequency to cover multiple specifications. Section 3 addresses this issue by proposing a widely continuously tunable transconductor. Section 4 describes an automatic frequency tuning scheme. Experiment results are shown in section 5 to validate the design. Finally some conclusions are drawn in section 6.

2. Reconfigurable OTA-C filter

System level simulations show that a sixth-order complex band pass/low pass filter may be sufficient to achieve the required selectivity. The sixth-order filter consists of two third-order complex band pass/low pass filters cascading together. Figure 1 shows a block diagram of the entire complex band pass/low pass filter. Due to the tough noise requirement on the filter, a 10-dB gain stage is placed at the filter input.

The third-order complex band pass/low pass filter is depicted in Fig. 2. It is based on two third-order Butterworth OTA-C low pass filters. A third-order complex band pass filter is constructed by coupling the two Butterworth low pass filters with the three gyrators which perform the linear frequency translation[2–4]. When the gyrators are active the filter works as a complex band pass filter, and when the gyrators are turned off the filter works as two low pass filters. The bandwidth and center frequency of the third-order filter are given by two equations below.

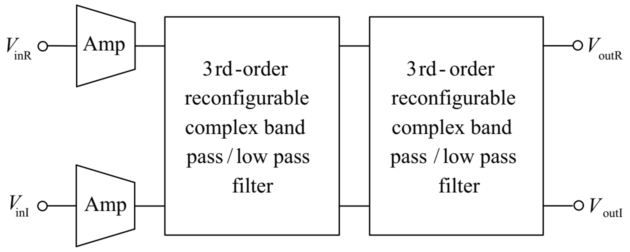

Fig. 1. Block diagram of the six-order filter.

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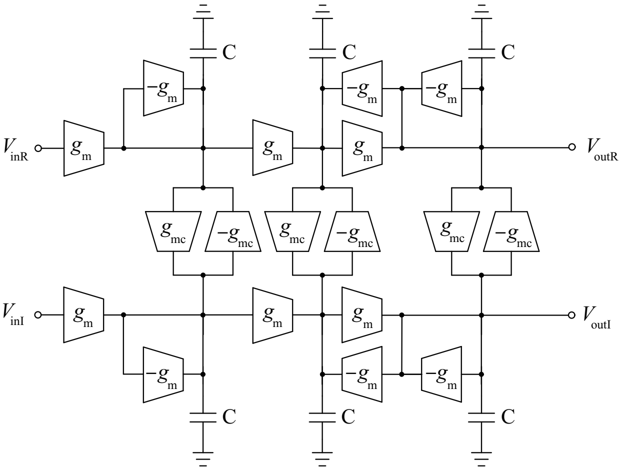

Fig. 2. Third-order complex band pass/low pass filter circuit.

$$\mathrm{BW}=\frac{g_{\mathrm{m}}}{C},\tag{1}$$

$$f_{\mathrm{c}}=\frac{g_{\mathrm{mc}}}{C}.\tag{2}$$

3. Widely tunable OTA design

According to the signal spectrum of each system and frequency planning of the receiver, the frequency response of the reconfigurable filter must be widely tunable. In the OTA-C filter, making the frequency response tunable can be achieved by tuning the transconductors or by tuning the capacitors. The former approach can obtain optimized power dissipation and the latter can obtain optimized noise performance but at the cost of large capacitor area[5]. So this paper focuses on the former approach.

Since the filter's cut-off frequency tunability ratio has to be about 10, we take process and temperature variations into account. The tunability requirement of the transconductor is obviously stringent. To reach a large tuning range without degrading its linearity and wasting power is still a challenge. So it is necessary to introduce another parameter to achieve this aim.

In this work a widely continuously tunable transconductor based on a digital technique is proposed, as depicted in Fig. 3. It is built around a differential pair without special linearization. This is found to be the best choice for the combination of distortion, noise and power specifications we intend to meet. Three groups of switches: {S50, S51, ..., S5n}, {S30, S31, ..., S3n} and {S10, S11, ..., S1n} are introduced. The transconductance tuning is made by switching, at the same time, input transistor widths and bias currents. The switching is realized by putting in parallel transistors inserted by digitally controlled MOSFET switches. By the proposed tuning scheme it is possible to make the transconductor tunable in a large range step by step and to keep the gate overdrive voltage of the input transistors constant. In this way the linearity performance remains constant and no useless current is dissipated. The tuning is coarse tuning; fine tuning is realized by the bias reference current $I_{\mathrm{ref\_f}}$ which comes from the fine tuning module depicted in Fig. 4.

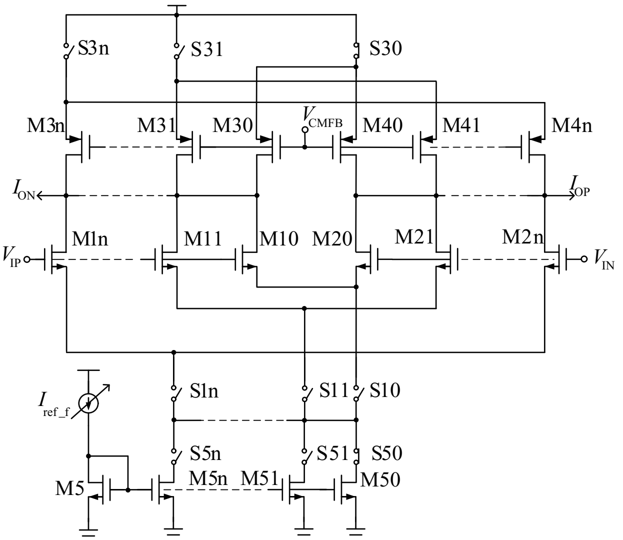

Fig. 3. Widely continuously tunable OTA circuit.

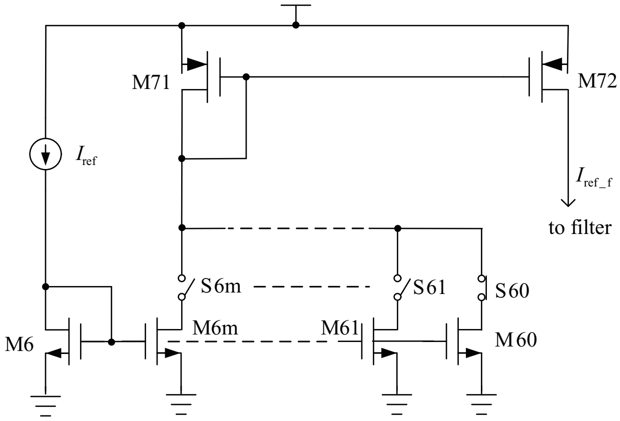

Fig. 4. Bias current generator circuit.

In Fig. 4, I_{ref} is a stable reference current. Switches {S60, ..., S6m} are introduced to tune the bias current $I_{\mathrm{ref\_f}}$ which is passed to the transconductor's bias circuit in Fig. 3. These switches make the current $I_{\mathrm{ref\_f}}$ change bit by bit, and then the transconductor is tuned bit by bit, and the transconductance can cover the part between two adjacent steps. The coarse tuning and fine tuning are combined, making the transconductance continuously tunable in a large range without heavily sacrificing linearity and power performance.

The proposed continuous-time CMFB circuit is a two stage differential difference amplifier CMFB as shown in Fig. 5. The CMFB circuit is tuned the same way as the transconductor to keep the CMFB loop stable.

In this work, $n=7, m=63$.

4. Automatic frequency tuning scheme

An automatic frequency tuning scheme is required to compensate for process variation[2−8]. In the OTA-C filter designed above, frequency tuning is achieved by tuning the transconductors with digital control signals. So the digital frequency tuning scheme is adopted. Figure 6 shows the frequency tuning circuit designed in this paper.

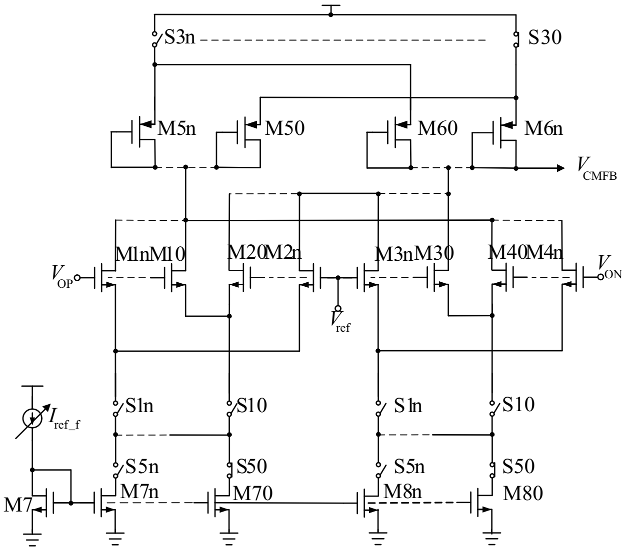

Fig. 5. Common-mode feedback circuit.

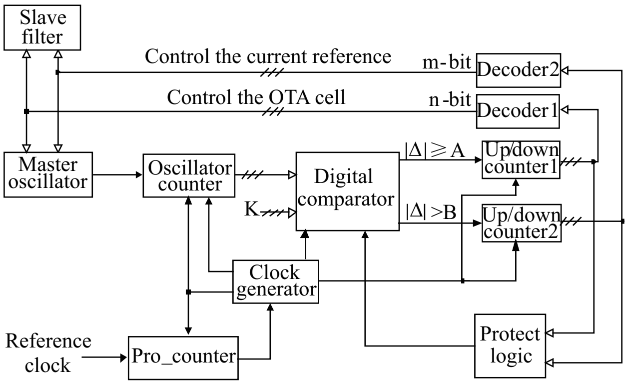

Fig. 6. The proposed digital frequency tuning circuit.

The master oscillator is a second-order harmonic oscillator based on the same OTA architecture used in the filter[7–9]. The oscillation frequency f_{ref} is linearly proportional to the filter cut-off frequency f_{c}. Supposing the desired filter cut-off frequency is f_{c}, then the oscillation frequency of the oscillator is given by

$$f_{\text{osc}} = Pf_{\text{c}}, \tag{3}$$

where P is a positive real number.

After system reset, the oscillator counter starts counting the oscillation frequency of the master oscillator. Under nominal conditions, in a specific time of K/f_{OSC}, where K is a positive integer, the count value of the oscillator counter should be K. If it is not K, it indicates that the oscillation frequency deviates from the expected value. The digital comparator compares the content of the oscillator counter with the constant K. If the absolute value of the difference between the two numbers is greater than A (A is a positive integer), the up/down counter 1 is clocked to count up or down accordingly, which makes the oscillation frequency move rapidly to the desired oscillation frequency step by step. This is coarse tuning. As long as the absolute value of the difference is greater than B (B is a positive integer too and it is less than A) the up/down counter 2 is clocked to count up or down accordingly, making the oscillation frequency move gradually to the desired frequency; this is fine tuning. The contents of the two up/down counters are then decoded respectively by two decoders to control the frequency of the oscillator. The same control signals are sent to the filter too to tune the cut-off frequency. When the absolute value of the difference is equal to or less than B, the two up/down counters freeze indicating that the oscillation frequency is equal to the desired frequency. The clock generator generates all the necessary clocks for the whole circuit, and the protect logic module prevents the two up/down counters overflowing. In this design, K is 128, A is 48 and B is 1.

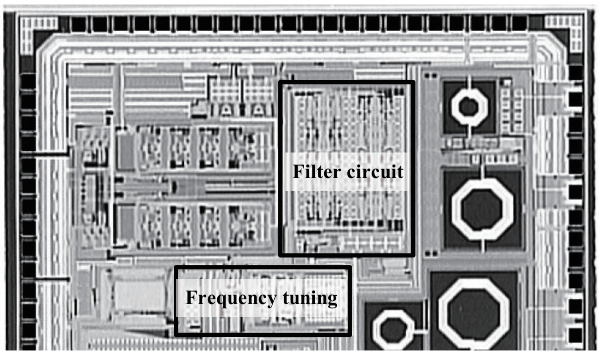

Fig. 7. Photomicrograph of the whole circuit.

The specific time K/f_{OSC} is provided by the programmable counter (pro-counter) that counts a reference frequency f_{ref}. So the pro-counter should count J cycles, and J can be described as

$$J = \frac{f_{\text{ref}}K}{f_{\text{OSC}}} = \frac{Kf_{\text{ref}}}{Pf_{\text{c}}}. \tag{4}$$

Equation (4) indicates two things. The first one is that the reference frequency f_{ref} is changed, the pro-counter can still provide the same time by changing J. The second is that when J is changed, the cut-off frequency of the filter is changed, meaning tuning the filter frequency response can be done by changing J.

5. Experiment results

The filter and the frequency tuning circuits have been implemented in a 0.18 μm RFCMOS process. The chip micrograph is shown in Fig. 7. The areas occupied by the filter and the tuning circuit are 0.9×0.6 mm^2 and 0.8×0.28 mm^2, respectively. The simulation results of the filter are summarized in Table 1.

Figure 8 shows the measured frequency response of the filter working as a complex band pass filter. Figure 8(a) shows the variable bandwidths with a constant center frequency. Figure 8(b) shows the variable center frequencies with a constant bandwidth.

To measure IMRR, quadrature sinusoidal signals are required. In this work, these signals are obtained by mixing the RF signal with the quadrature LO signals. Figure 9 shows the filter frequency response for the signal and image sides in a typical application condition. The figure shows that the image

Table 1. Summarized filter simulation results.

Parameter	Value	
Operating mode	Complex band pass	Real low pass
Supply voltage (V)	1.8	1.8
Filter current drain (mA)	0.8–3.2	1.1–2.3
Center frequency, f_c (MHz)	3–16	0
–3 dB bandwidth, BW (MHz)	3–24	8–15
Pass band gain (dB)	10	10
Image rejection when f_c = 4 MHz, BW = 4 MHz (dB)	–50 @ –4 MHz	—
In band –1 dB compress point (dBm)	–15	–15
Output noise power spectral density (nV/$\sqrt{\text{Hz}}$)	50–220	65–130

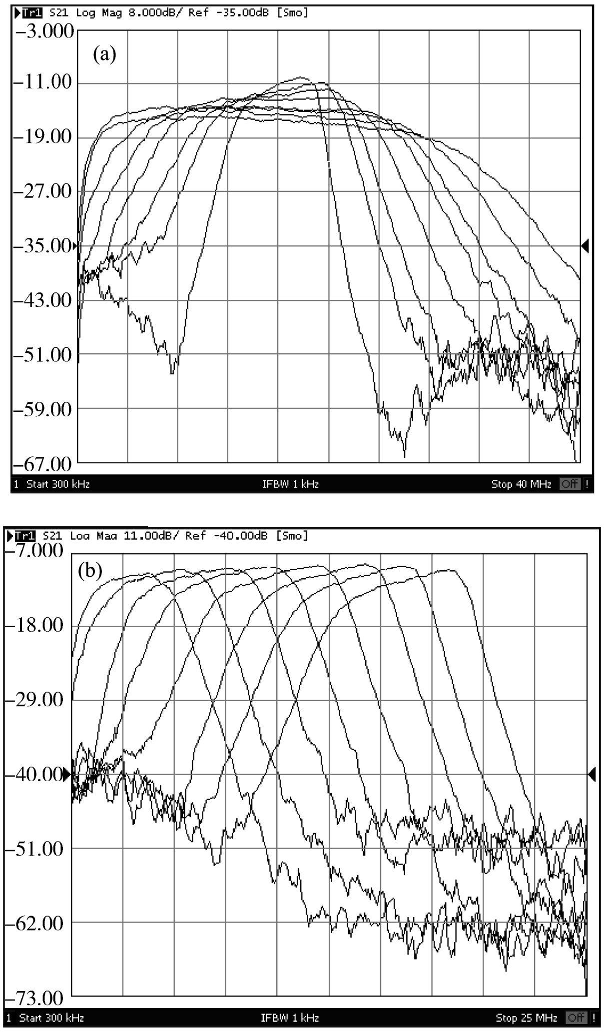

Fig. 8. Measured transfer functions of the tunable filter in complex band pass filter mode. (a) Variable bandwidths with a constant center frequency. (b) Variable center frequencies with a constant bandwidth.

rejection ratio is more than 34 dB, which is enough for system specifications.

Figure 10 shows the tunable frequency response of the filter working as a low pass filter. Owing to the equipment limitations the very low frequency response is suppressed.

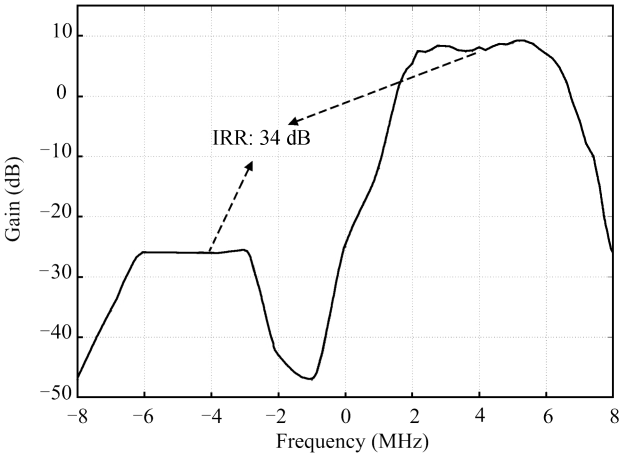

Fig. 9. Measured frequency response at signal and image sides.

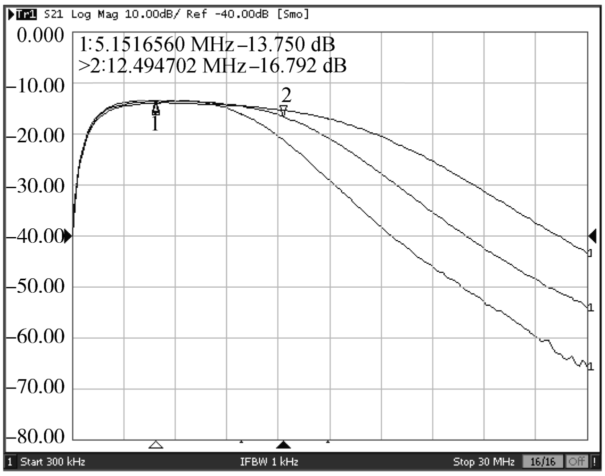

Fig. 10. Measured transfer functions of the tunable filter in real low pass filter mode.

6. Conclusion

A sixth-order reconfigurable OTA-C filter with widely continuously tunable transconductors based on the digital technique is presented. The bandwidth can be tuned from 3 to 24 MHz and the center frequency from 3 to 16 MHz in complex band pass mode. The bandwidth in real low pass mode is also tunable from 8 to 15 MHz. The proposed tuning scheme combines tuning for satisfying different system standards and tuning for compensating for process variations, achieving optimized linearity and power performance. The tuning scheme can also work at different reference frequencies.

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