Two-dimensional pixel image lag simulation and optimization in a 4-T CMOS image sensor*

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Abstract: Pixel image lag in a 4-T CMOS image sensor is analyzed and simulated in a two-dimensional model. Strategies of reducing image lag are discussed from transfer gate channel threshold voltage doping adjustment, PPD N-type doping dose/implant tilt adjustment and transfer gate operation voltage adjustment for signal electron transfer. With the computer analysis tool ISE-TCAD, simulation results show that minimum image lag can be obtained at a pinned photodiode n-type doping dose of 7.0×10^{12} cm^{-2}, an implant tilt of –2°, a transfer gate channel doping dose of 3.0×10^{12} cm^{-2} and an operation voltage of 3.4 V. The conclusions of this theoretical analysis can be a guideline for pixel design to improve the performance of 4-T CMOS image sensors.

Key words: image lag; two-dimensional simulation; doping dose; implant tilt; CMOS image sensor
DOI: 10.1088/1674-4926/31/9/094011 **EEACC:** 1205; 2550X; 7230G

1. Introduction

In recent years, great effort has been put into the development of CMOS image sensors (CIS) owing to their many advantages over CCD, such as low cost, low power consumption, system integration and compatibility with the CMOS process[1, 2]. Moreover, with the introduction of the pinned photodiode (PPD)[3], CIS is thought to be more promising and is expected to become a future choice[4, 5]. However, the existence of image lag in pinned photodiode pixels causes the quality of the reproduced pictures to deteriorate[6], particularly for capturing the image of a moving object. Thus, if the image lag is eliminated, applications of CIS can be widely extended and then high-quality CIS images can be comparable to those of CCD. Previous work on reducing image lag has been done either by improving the charge transfer efficiency from the photodiode (PD) to floating diffusion (FD) or optimizing the PPD structure and transfer gate[7–10].

In this paper, pixel image lag in a two-dimensional model is simulated and optimized with the computer analysis tool ISE-TCAD. Strategies of reducing image lag are discussed from transfer gate (M_{TG}) channel threshold voltage V_t doping adjustment, PPD N-type doping dose/implant tilt and M_{TG} operation voltage for signal electrons transfer. With these simulation results, the optimal process and operation condition is obtained.

2. Image lag mechanism and theoretical model

Image lag is a phenomenon in which some of the signal electrons cannot be transferred completely to the storage node and remain in the photodiode region. The residual electrons are transferred in the subsequent frames as image lag[11]. A schematic view of a 4-T CIS pixel cell is shown in Fig. 1, where the pinned photodiode (PPD), transfer gate (M_{TG}) and floating diffusion (FD) are included. The corresponding ideal potential profiles of PPD, M_{TG} and FD are shown in Fig. 2(a).

Theoretically, the signal electrons can be transferred completely to FD if the potential well bottom of the PPD is sufficiently higher than M_{TG} and FD. However, the power supply voltage in CIS is much lower than CCD and a low-voltage transfer pulse may cause incomplete charge transfer in CIS[12]. In addition, doping profile, trap level or potential variance in the PPD and M_{TG} channel originating from crystal defects or contamination in the pixel fabrication process[9, 13] can introduce a potential barrier in the boundary between the PPD and M_{TG}. Taking these into account, the real potential diagram could be non-ideal as shown in Fig. 2(b). When signal charges are transferred, residual electrons will be left in the PPD region

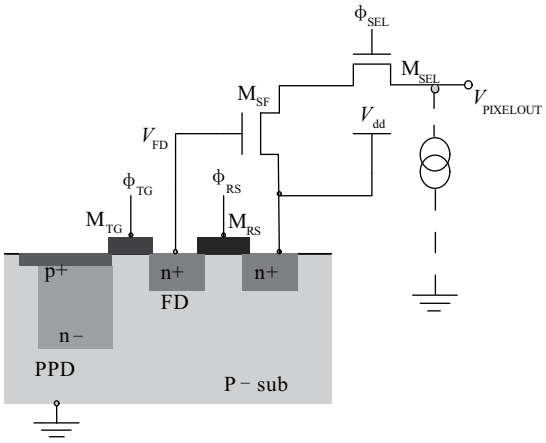

Fig. 1. Schematic view of a 4-T CIS pixel cell.

* Project supported by the National Natural Science Foundation of China (Nos. 60806010, 60976030) and the Tianjin Innovation Special Funds for science and Technology, China (No. 05FZZDGX00200).
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Received 15 March 2010, revised manuscript received 10 April 2010

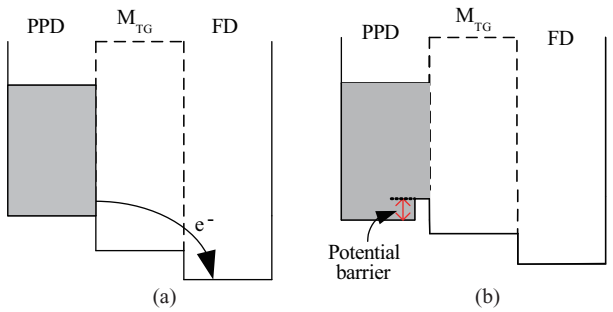

Fig. 2. Potential diagram of PPD, TG and FD. (a) Ideal. (b) Non-ideal.

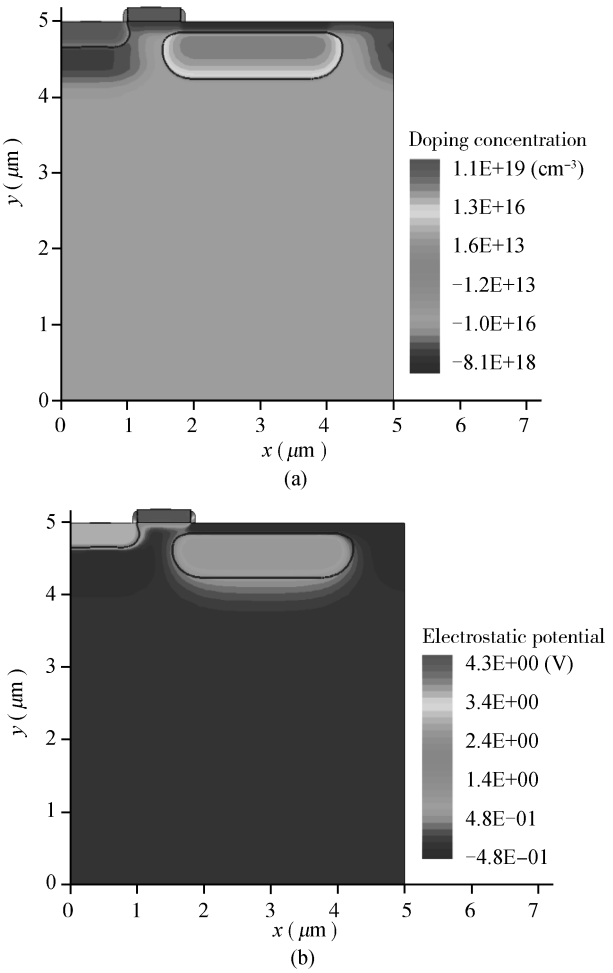

Fig. 3. Cell structure diagram. (a) Doping profile. (b) Potential profile.

due to the existence of the potential barrier, which behaves as image lag in the reproduced images.

So, in order to reduce the potential barrier in the 4-T pixel, the pixel design in both the photodiode structure and M_{TG} channel and its operation condition should be optimized.

3. Simulation results and analysis

A pinned photodiode is a buried channel device with at least two implants: surface P layer boron and buried N layer arsenic on a p-type boron doped substrate. M_{TG} and FD are formed with the conventional CMOS process. Figure 3 shows the cell structure diagram with ISE-TCAD simulation, where

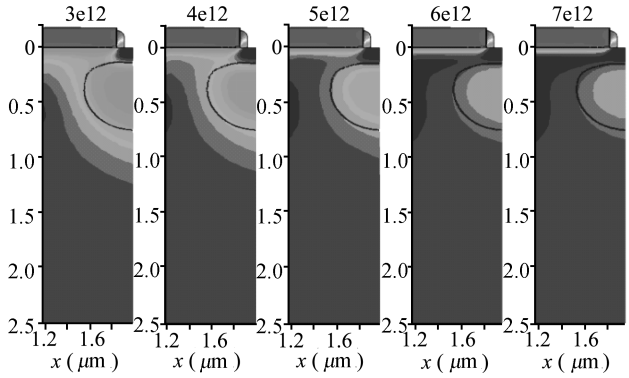

Fig. 4. Potential diagram between PD and TG channel for M_{TG} channel V_t doping optimization.

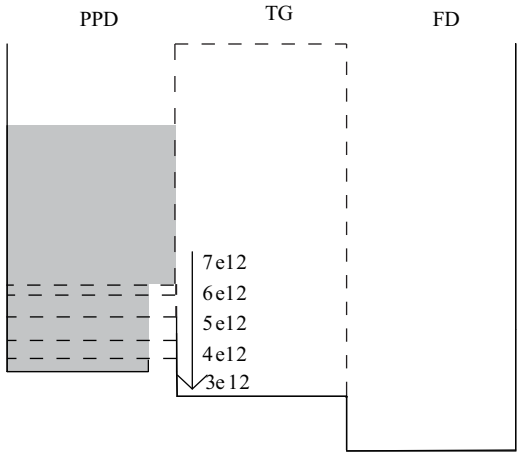

Fig. 5. Diagram for the potential profile.

(a) is the doping profile and (b) is the potential diagram.

3.1. M_{TG} channel V_t doping optimization

In order to find the relationship between image lag and M_{TG} channel doping for threshold voltage V_t tuning, different V_t adjustment implant doses with boron at 3.0×10^{12}, 4.0×10^{12}, 5.0×10^{12}, 6.0×10^{12} and 7.0×10^{12} cm^{-2} are simulated respectively. Potential diagrams between the PD and M_{TG} channel are obtained as shown in Fig. 4.

From left to right, the corresponding channel boron implant doses are 3.0×10^{12}, 4.0×10^{12}, 5.0×10^{12}, 6.0×10^{12} and 7.0×10^{12} cm^{-2}. The potential barrier can be seen between the M_{TG} channel and PPD region from simulation results. The two-dimensional potential distribution diagram also shows that reducing the M_{TG} channel implant dose within a specified process range can reduce the potential barrier. However, the minimum dose should be maintained to ensure that there is no drain-induced barrier lowering (DIBL) effect. Figure 5 shows an abstract one-dimensional diagram for the potential profile. Dotted lines represent different M_{TG} channel V_t doping levels respectively: the upper one is 7.0×10^{12} followed by 6.0×10^{12}, 5.0×10^{12} cm^{-2}, 4.0×10^{12} and 3.0×10^{12}. The potential barrier becomes higher with higher doping dose. The relationship between the above doping dose and the PD potential diagram across the photodiode center region after electron transfer is shown in Fig. 6. The maximum potential voltage in the PD can

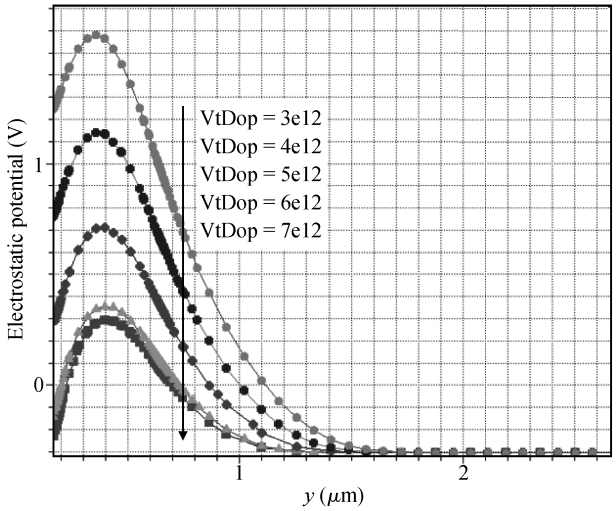

Fig. 6. PD potential diagram after electron transfer.

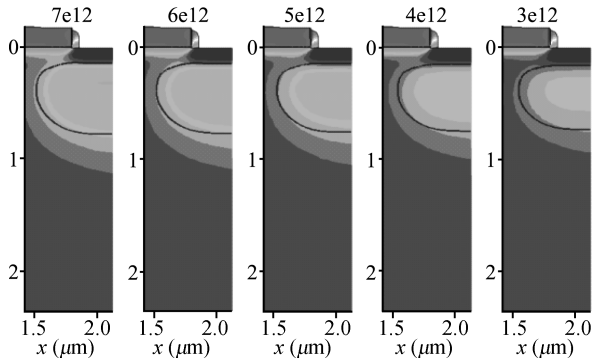

Fig. 7. Potential diagram between PD and M_{TG} channel for PD n-type region doping optimization.

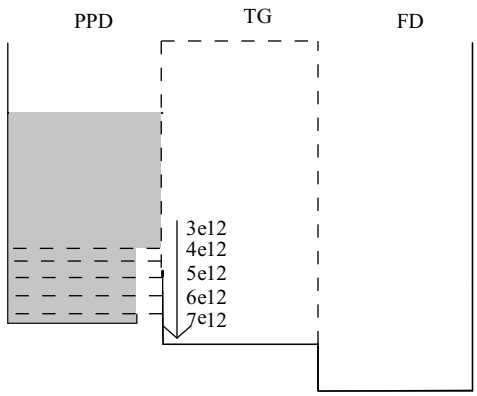

Fig. 8. Diagram for the potential profile.

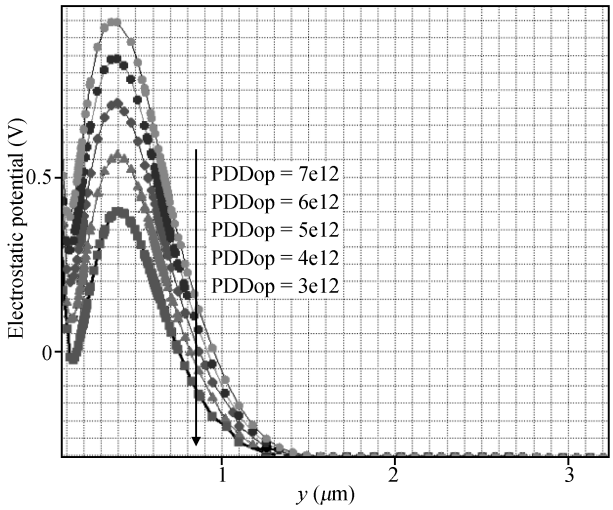

Fig. 9. PD potential diagram after electron transfer.

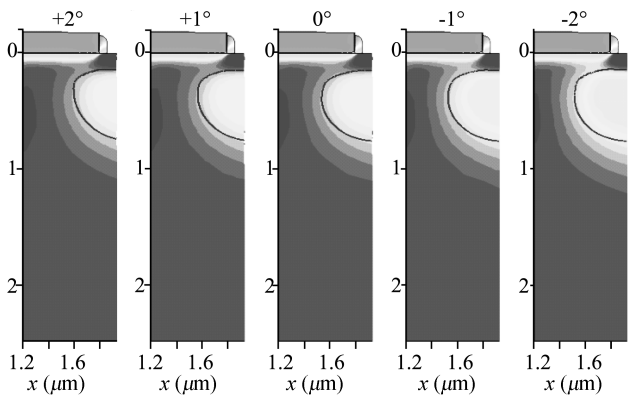

Fig. 10. Potential diagram between PD and M_{TG} channel for PD n-type region doping optimization.

be concluded to be: $V_{3.0e+12} > V_{4.0e+12} > V_{5.0e+12} > V_{6.0e+12} > V_{7.0e+12}$. More residual electrons in the PD correspond to a lower potential voltage. This result is consistent with the potential barrier level in Fig. 4.

3.2. PD n-type region doping optimization

3.2.1. Implant dose adjustment

The formation of the PPD is controlled elaborately with implant dose and energy; also, RTP (rapid thermal annealing) is a necessary process step to drive arsenic laterally under the edge of the transfer gate and deeper into the substrate. Simulation results with different PD implant doses are shown in Fig. 7.

The corresponding doses are 7.0×10^{12}, 6.0×10^{12}, 5.0×10^{12}, 4.0×10^{12} and 3.0×10^{12} cm^{-2}. Simulation results show that within a specified process range, the higher doses can lead to a lower potential barrier. Figure 8 shows the abstract one-dimensional potential profile. Dotted lines represent different PD n-type doping levels respectively: the upper one is 3.0×10^{12} followed by 4.0×10^{12}, 5.0×10^{12} cm^{-2}, 6.0×10^{12} and 7.0×10^{12}. Figure 9 shows the corresponding PD potential across the photodiode center region after electron transfer. From the potential diagram, it is concluded that for different PD doping doses, the higher n-type doping causes fewer residual electrons. However, with a high implant dose, the PD depletion layer width reduces and well capacity becomes smaller. In order to reduce image lag and also retain sufficient well capacity, PD n-type doping should be increased with a specified range.

3.2.2. Implant tilt adjustment

The potential barrier behavior with PD n-type impurity implant tilt adjustment is also simulated. Figure 10 illustrates the simulated potential barrier results for tilt = +2°, +1°, 0°,

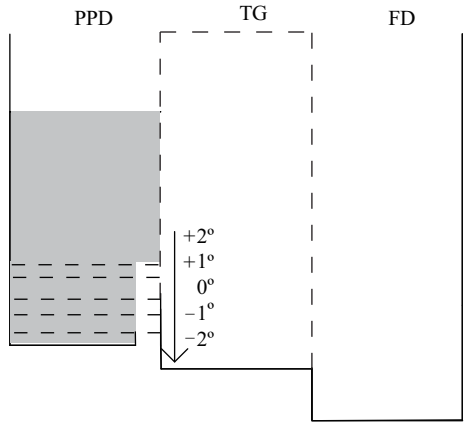

Fig. 11. Diagram for the potential profile.

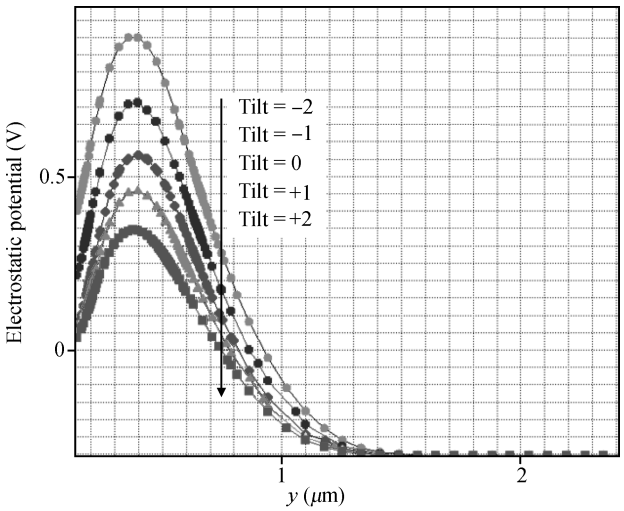

Fig. 12. PD potential diagram after electron transfer.

–1°, –2° and it is found that with tilt = –2° the potential barrier reaches its smallest value. The corresponding abstract one-dimensional potential diagram and PD potential across the photodiode center region after electron transfer are shown in Figs. 11 and 12. If the implant tilt is adjusted to a larger negative value, PD well capacity will decrease for a shallower n-type impurity implant depth. It can be concluded that with a small implant tilt adjustment, the image lag in the 4-T pixel can be optimized to a lower level.

3.2.3. M_{TG} operation voltage optimization

The signal charge transfer efficiency is strongly related to the transfer voltage of the transfer transistor. In this simulation analysis, with different bias conditions, that is, V_{TG} = 3.0, 3.2, 3.3 V, improvements of image lag are illustrated in Fig. 13. Simulation results show that increasing the gate voltage can reduce the potential barrier. Figures 14 and 15 show the corresponding abstract one-dimensional potential diagram and PD potential across the photodiode center region after electron transfer. It can be concluded that with V_{TG} = 3.3 V, the optimum image lag performance is obtained.

However, it is not always the case that the larger the M_{TG} operation voltage is, the fewer residual electrons are left in PD region. A larger M_{TG} operation voltage also can involve elec-

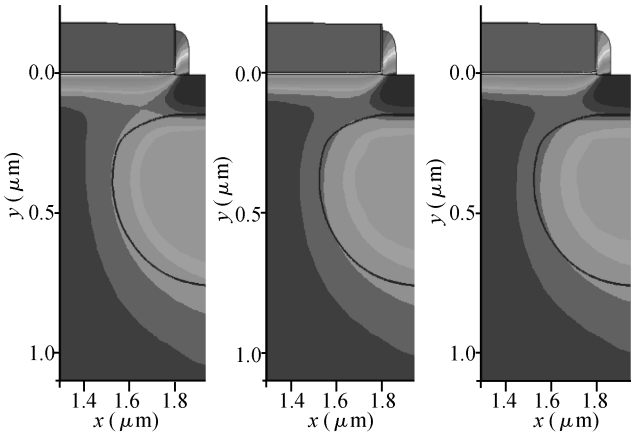

Fig. 13. Potential diagram between PD and M_{TG} operation voltage optimization.

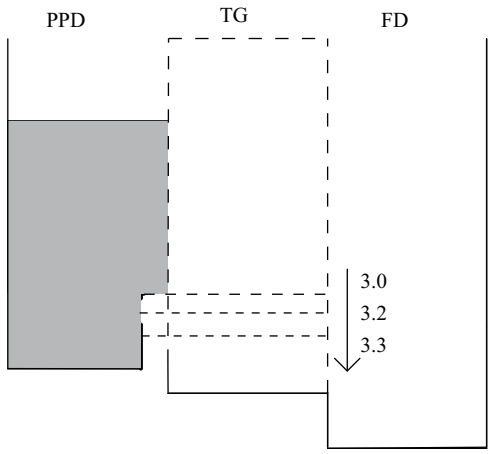

Fig. 14. Diagram for the potential profile.

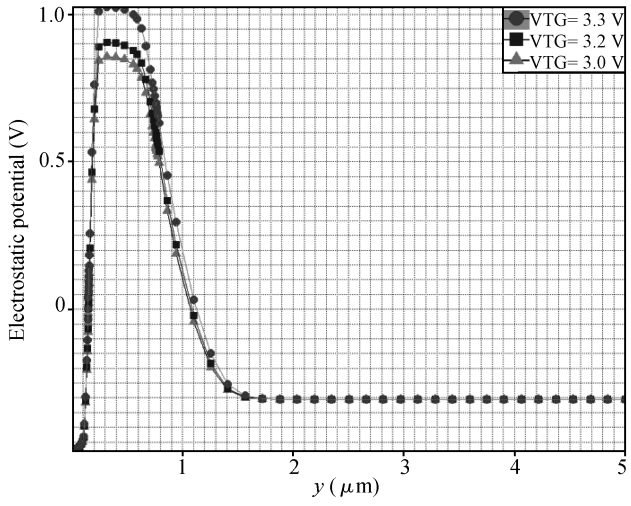

Fig. 15. PD potential diagram after electron transfer.

tron injection from FD to the M_{TG} channel, which will degrade the pixel's noise performance. Potential barriers between the PD and M_{TG} channel for V_{TG} = 3.4, 3.5 and 3.6 V are also simulated. Figure 16 shows the PD potential diagram after electron transfer for all simulated V_{TG} operation levels. It can be con-

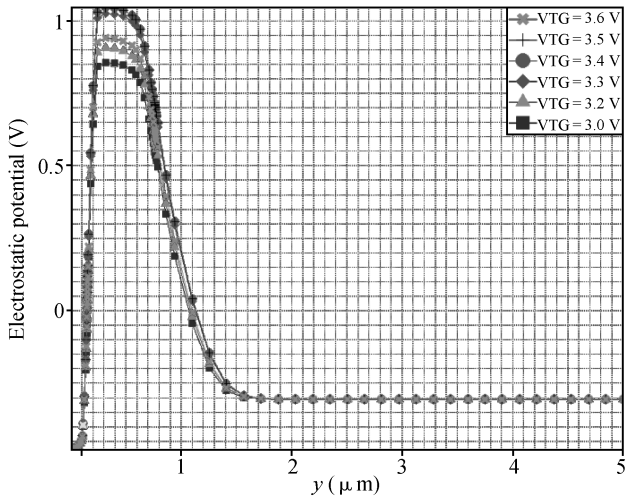

Fig. 16. PD potential diagram after electron transfer.

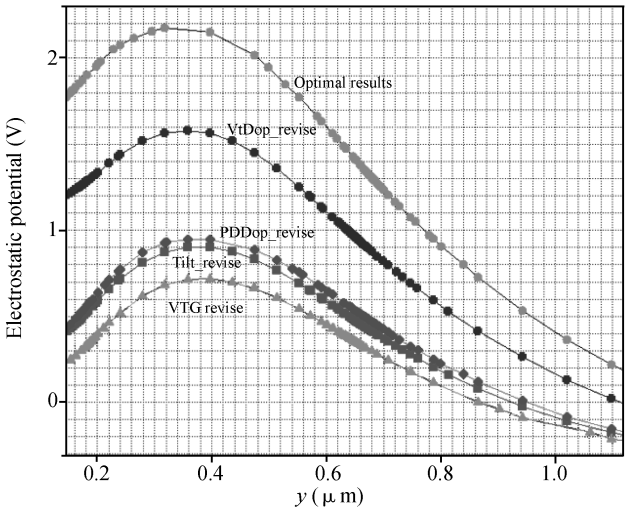

Fig. 17. Simulation results of image lag optimization considering all process parameters versus separate revised process parameters.

cluded that V_{TG} = 3.4 V is the optimum M_{TG} operation condition to effectively reduce the image lag for the given pixel.

Finally, the simulation results of image lag for all optimized parameters and the optimal simulation result considering all process parameters are shown in Fig. 17. It can be concluded that, with the given process conditions, minimum image lag can be obtained at a pinned photodiode n-type doping dose of 7.0×10^{12} cm^{-2}, an implant tilt of –2°, a transfer gate channel doping dose of 3.0×10^{12} cm^{-2} and an operation voltage of 3.4 V.

4. Conclusion

Image lag in 4-T CIS is simulated based on the pixel fabrication process and pixel operation condition with the ISE-TCAD tool. The optimal conditions for reducing image lag are also obtained. These simulation results provide a predictive method to assist optimization of pixel image lag in 4-T CMOS image sensors.

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