A 1.2-V 19.2-mW 10-bit 30-MS/s pipelined ADC in 0.13-μm CMOS*

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Abstract: A 10-bit 30-MS/s pipelined analog-to-digital converter (ADC) is presented. For the sake of lower power and area, the pipelined stages are scaled in current and area, and op amps are shared between the successive stages. The ADC is realized in the 0.13-μm 1-poly 8-copper mixed signal CMOS process operating at 1.2-V supply voltage. Design approaches are discussed to overcome the challenges associated with this choice of process and supply voltage, such as limited dynamic range, poor analog characteristic devices, the limited linearity of analog switches and the embedded sub-1-V bandgap voltage reference. Measured results show that the ADC achieves 55.1-dB signal-to-noise and distortion ratio, 67.5-dB spurious free dynamic range and 19.2-mW power under conditions of 30 MSPS and 10.7-MHz input signal. The FoM is 0.33 pJ/step. The peak integral and differential nonlinearities are 1.13 LSB and 0.77 LSB, respectively. The ADC core area is 0.94 mm^2.

Key words: analog-to-digital converter; pipelined; sampling capacitor; two-stage op amp compensation; linearity of analog switch; sub-1-V bandgap voltage reference

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1. Introduction

As device dimensions shrink, operating voltages reduce proportionally to guarantee long-term reliability. Therefore, lower voltage design is becoming a more and more important issue for analog integrated circuits expected to operate around 1-V supply voltage. When the device dimensions shrink from 0.5, 0.35 to 0.25 μm, 0.18 μm, the corresponding supply voltages are also reduced from 5, 3.3 to 2.5 V, 1.8 V. For analog design, this development trend poses little difficulty[1]. Firstly, there is sufficient voltage headroom for V_{DD} to reduce in most op amp topologies, including cascode schemes. As a result, signal amplitude is not reduced significantly. Second, a conventional bandgap voltage reference (BVR) generating about 1.25-V reference voltage is able to be used in 1.8-V or above supply voltage. As device dimensions further shrink to 0.13 μm, or even 90 nm, 65 nm, the supply voltages are reduced to around 1 V. Due to the system-on-a-chip (SoC) integration, the analog supply voltage is forced to be lower than that of the digital circuit. This development trend gives rise to more challenges for analog design. Circuits with topologies sacrificing the voltage margin like cascode circuits have difficulty in achieving required specifications while maintaining the former signal swing. Cascode op amps have little actual dynamic range and suffer from gain loss due to their shorter channel length, making it increasingly difficult to meet higher performance expectations. The increasing ratio of signal swing to supply voltage deteriorates the linearity of analog switches, and the conventional BVR is unable to be used because 1.25 V exceeds the supply voltage.

In this paper, a 10-bit 30-MSample/s pipelined ADC operating at 1.2-V supply voltage in the 0.13-μm CMOS process is presented. The problems encountered in the around 1-V supply voltage and the deep sub-micron process are analyzed and design approaches are demonstrated. Also, the ADC architecture is presented, the challenges associated with the deep sub-micron process and the around 1-V supply voltage are described and the approaches are also demonstrated.

2. ADC architecture

This ADC, which is illustrated in Fig. 1, consists of a sample/hold amplifier (SHA) and nine stages, the last of which is the 2-bit-flash-ADC. A 1.5-bit/stage architecture with RSD digital correction is chosen in the design due to its relatively simple structure, the great tolerance of the comparator offset and high conversion speed. The front-end SHA is used to re-

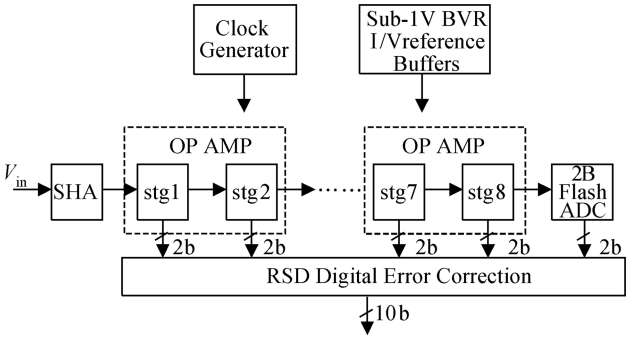

Fig. 1. ADC architecture.

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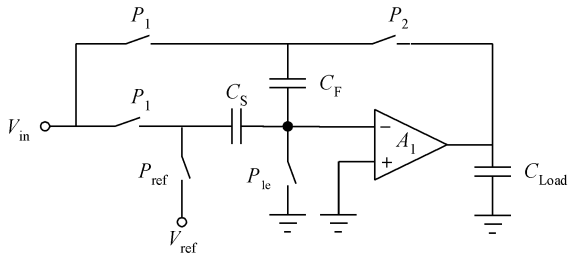

Fig. 2. MDAC architecture.

duce the aperture error. For the sake of lower power and area, the 1st to 8th stages are scaled in area and current, and op amps are shared between the successive stages. The sub-1-V BVR and I/V reference buffers are both embedded in the chip. The clock generator is also illustrated in the figure.

3. Circuit design

In a pipelined ADC, the error sources fall into three categories: noise, static error and dynamic error. The noise is mainly thermal noise which is derived from op amps and switch-on-resistance. The static errors include comparator offsets, voltage reference error and finite DC gain error. The dynamic errors include incomplete settling of the op amp and the nonlinearity of the sample switch. The comparator offsets can easily be tolerated for 1.5-bit/stage resolution by employing the RSD digital correction, and the rest of the sources are discussed. Section 3.1 focuses on the thermal noise. Section 3.2 focuses on finite gain error and incomplete settling of the op amp. Section 3.3 focuses on the nonlinearity of sampling switches. Section 3.4 describes the internal I/V reference buffers based on the sub-1-V BVR to suppress the voltage reference errors.

3.1. Choice of sampling capacitance

Despite dimension scaling, the signal-to-noise ratio (SNR) should remain constant. SNR is proportional to $(V_{\text{signal}})^2/(kT/C)$, where V_{signal} is the actual signal amplitude, and C is the capacitance. From the point of view of power, V_{signal} is preferred so that C can be reduced. But considering the linearity of the switch and the choice of op amp, a smaller V_{signal} is preferred. So, there is a tradeoff between power and linearity.

In switch capacitor (SC) circuits, the sampling capacitor is mainly determined by two factors, mismatching error between the sampling capacitances and the kT/C noise. The impact of the first factor is reduced for advanced processes while the impact of the second factor is increased for reduced actual dynamic amplitudes.

Considering other noise sources including quantization noise and thermal noise, the relationship between SNR, C and V_{signal} is derived. Figure 2 illustrates a 1.5-bit/stage MDAC architecture. The total loading capacitance of op amp A_1 is given as

$$C_{\text{total}} = C_{\text{load}} + C_{\text{par.out}} + (1-f)C_{\text{f}}, \tag{1}$$

$$f = \frac{C_{\text{f}}}{C_{\text{f}} + C_{\text{s}} + C_{\text{par.in}}}, \tag{2}$$

where C_{s} is the sampling capacitance, $C_{\text{f}} = C_{\text{s}}$ is the feedback capacitance, $C_{\text{par.in}} = C_{\text{s}}/2$ is the input parasitic capacitance of the op amp, therefore, $f = 0.4$ is the feedback factor of the MDAC, $C_{\text{load}} = (2 \times 0.7) \times C_{\text{s}}$ is the next stage capacitance load derived from the stage scaling factor of 0.7, and $C_{\text{par.out}} = 0.4C_{\text{s}}$ is the op amp output capacitance. Therefore, $C_{\text{total}} = 2.4C_{\text{s}}$.

The single input-referred noise including kT/C noise of switch-on-resistance and the op amp can be described[2] in Eqs. (3) and (4), respectively.

$$\overline{V}^2_{\text{in.noise.kT/C}} = \frac{kT(C_{\text{s}} + C_{\text{f}} + C_{\text{par.in}})}{C_{\text{s}} + C_{\text{f}}} = \frac{5}{8}\frac{kT}{C_{\text{s}}}, \tag{3}$$

$$\overline{V}^2_{\text{in.noise.opamp}} = kT\gamma(1+F)\frac{1}{f}\frac{1}{C_{\text{total}}}\left(\frac{C_{\text{f}}}{C_{\text{s}} + C_{\text{f}}}\right)^2 = \frac{25}{144}\frac{kT}{C_{\text{s}}}, \tag{4}$$

where $k = 1.38 \times 10^{-23}$ J/K is the Boltzmann constant, $T = 400$ K is absolute temperature, $F = 1$ is the noise factor for the op amp, and $\gamma = 2/3$ is the noise factor.

Considering differential-input application of the ADC and op amp sharing in the successive stages, the ADC's total input-referred noise including SHA can be described in Eq. (5) for 0.7 scaling in successive stages.

$$\begin{aligned}\overline{V}^2_{\text{in.noise.total}} &= 2\left(\sum \overline{V}^2_{\text{in.noise.kT/C}} + \sum \overline{V}^2_{\text{in.noise.opamp}}\right) \\ &= 2\left[\overline{V}^2_{\text{in.noise.kT/C}}\left(1 + \sum_{k=0}^{3}(0.7^2)^k\right)\right. \\ &\quad \left. + \overline{V}^2_{\text{in.noise.opamp}} \times \left(1 + \sum_{\text{k=0}}^{7}(0.7)^k\right)\right] \\ &\approx 6\frac{kT}{C_{\text{s}}}.\end{aligned} \tag{5}$$

SNR is calculated in Eq. (6).

$$\begin{aligned}\text{SNR} &= 10\lg\frac{\frac{1}{2}\left(\frac{2^n\Delta}{2}\right)^2}{\overline{V}^2_{\text{quantizition}} + \overline{V}^2_{\text{in,noise.total}}} \\ &= 10\lg\frac{\frac{1}{2}\left(\frac{2^n\Delta}{2}\right)^2}{\frac{\Delta^2}{12} + 6\frac{KT}{C_{\text{s}}}},\end{aligned} \tag{6}$$

where $\Delta = V_{\text{LSB}} = V_{\text{signal}}/2^n$ is the least significant bit and n is the ADC resolution. Let $n = 10$ in Eq. (6); the SNR versus C_{s} and V_{signal} is illustrated in Fig. 3. Given the specification SNR = 60 dB for this ADC, there are different combinations of C_{s} and V_{signal} which are shown in Fig. 2. The V_{signal} is determined by op amp architecture and the decision will be made in Section 3.2.

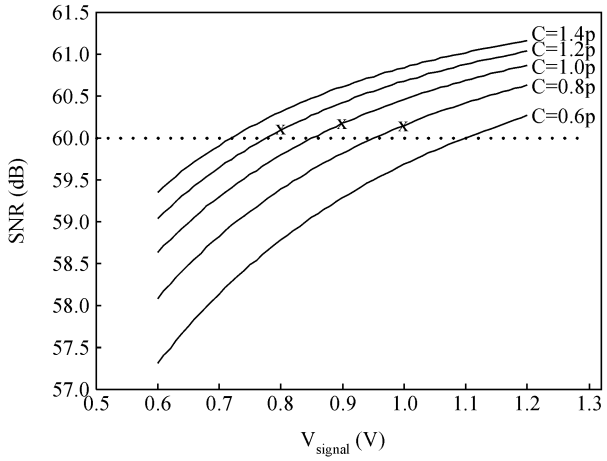

Fig. 3. SNR versus sampling capacitance C_s, signal amplitude V_{signal}.

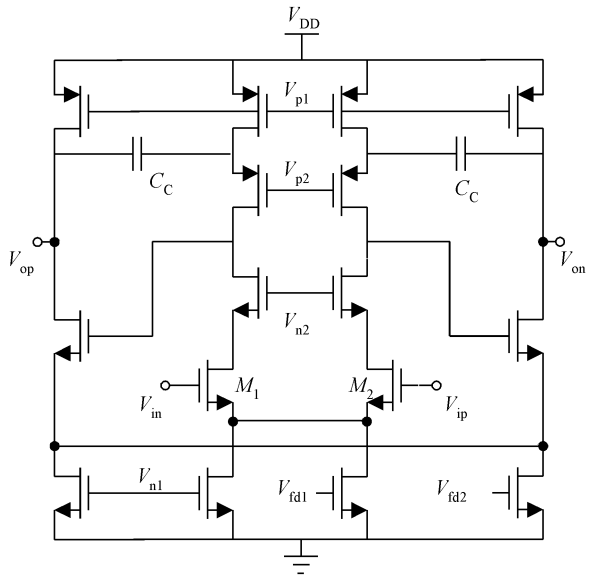

Fig. 4. Two-stage op amp with improved Ahuja compensation.

3.2. Choice of op amp

The op amp architecture based on a gain-boosting folded cascode or telescopic[3] architecture op amp is often preferred in 1.8-V or above supply voltage applications for adequate signal amplitude. Suffering from lower signal swing and gain loss, those single stage cascode op amps are not fit to be used here. As described in Section 3.1, smaller V_{signal} needs larger C and consumes more power. In order to ensure the ADC has a large output swing and high DC gain, a two-stage op amp is chosen in the design, which is illustrated in Fig. 4. V_{signal} = 1.0 V and C_s = 0.8 pF are given in the design.

The settling error mainly includes ε_{gain} and ε_{settle} at the output of the op amp,

$$\varepsilon_{gain} = \frac{1}{A_0 f} < \frac{1}{2}\text{LSB} = \frac{1}{2^{n+1}}, \quad (7)$$

$$\varepsilon_{settle} = e^{-\frac{T}{3}\omega_{-3dB}} = e^{-\frac{GBW\times f}{3F_s}} < \frac{1}{2}\text{LSB} = \frac{1}{2^{n+1}}, \quad (8)$$

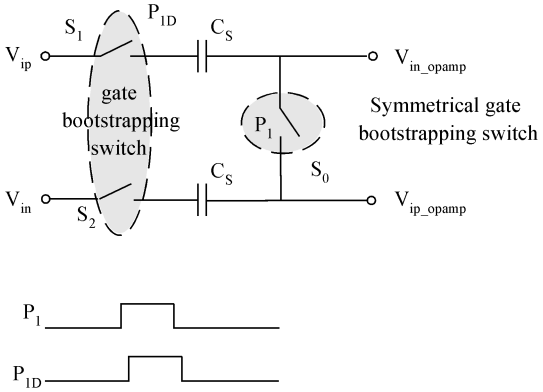

Fig. 5. Sampling net of the front-end SHA.

where ε_{gain} is the gain error resulting from the finite open loop DC gain A_0, ε_{settle} is the incomplete settling error caused by the finite unit gain-bandwidth (GBW) of the op amp, f = 0.4 is the feedback factor of the MDAC obtained from Section 3.1, and n = 10 is the ADC's resolution. F_s = 30 MSPS is the sampling rate of the ADC. The specifications of the op amp can be calculated. The minimum values of A_0 and GBW are 74 dB and 306 MHz, respectively. Therefore, let A_0 = 80 dB, GBW = 350 MHz.

The op amp circuit is illustrated in Fig. 4. It consists of a telescopic stage and a class A amplifier as an output stage. The first stage aims to achieve high DC gain and the second stage aims to achieve large swing. Improved Ahuja compensation is used in the op amp, and its advantage is that it eliminates the RHP zero[4]. Two separated SC common-mode feedback circuits (SC-CMFBs, not shown in Fig. 4) are used to generate control voltage V_{fd1}, V_{fd2}. The common-mode level of the differential output is determined by the two SC-CMFBs.

3.3. Gate bootstrapping switch

Switch linearity degeneration and large on-resistance are serious phenomena in the around 1-V supply voltage analog circuit design. The increased ratio of V_{signal} to supply voltage deteriorates the linearity of analog switches and relatively large V_{signal} results in large on-resistance. The CMOS switch has less on-resistance than the MOS switch and is used with the purpose of shorting its input and output when it is on. However, it is not appropriate to be used as a sampling switch in the high band input application due to its poor linearity. The clock boosting scheme is an effective way to enhance the switch linearity with a high gate voltage by keeping the gate–source voltage of the analog switch constant while remaining independent of the input signal, which, however, is contrary to the trend of a lower gate breakdown voltage in the advanced CMOS process.

The sampling net of the front-end SHA is illustrated in Fig. 5. A bottom sampling technique is used to eliminate the source error of charge injection of S_1 and S_2, when the switches turn off. It is required that S_0, which is controlled by P_1, turns off earlier than S_1, S_2, which are controlled by P_{1D}.

The gate bootstrapping scheme is adopted in S_0, S_1 and S_2 for the sake of smaller on-resistance and less distortion. The schematic of S_1 and S_2 is shown in Fig. 6(a). The working principle can be explained as below. When the clk is from high to low, the boosting capacitor C_b is charged to the supply volt-

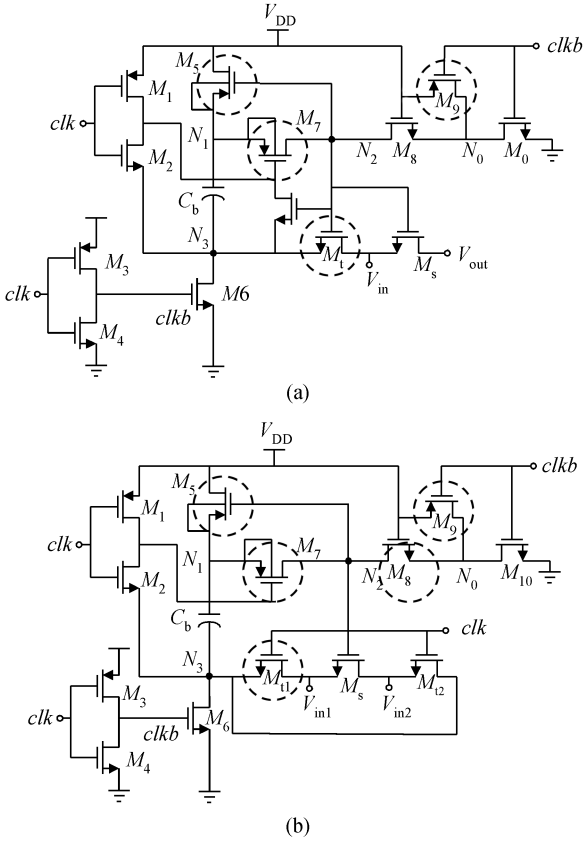

Fig. 6. (a) Gate-bootstrapping switch used for input sampling. (b) Symmetrical switch used for bottom sampling.

age V_{DD} as M5 and M6 turn on. When the clk is from low to high, M5 and M6 turn off while M7, Mt turn on, the gate-source voltage of switch transistor $V_{gs,Ms}$ is constant V_{DD} ignoring the parasitic capacitance in node N_1, C_{N1} and N_2, C_{N2}, and the on-resistance of Ms is reduced while the linearity is increased.

Considering the parasitic capacitance in node N_1 and N_2, the actual $V_{gs,Ms}$ is not equal to V_{DD}. Due to charge conservation, the $V_{gs,Ms}$ is given by

$$\begin{aligned} V_{gs,M_s} &= V_{N2} - V_{in} \\ &= V_{DD}\frac{C_b + C_{N1}}{C_b + C_{N1} + C_{N2}} - V_{in}\frac{C_{N1} + C_{N2}}{C_b + C_{N1} + C_{N2}}. \end{aligned} \quad (9)$$

From Eq. (9), it is obvious that the circuit's long term reliability is guaranteed since $V_{gs,Ms}$ never exceeds V_{DD}[5] . The larger C_b is preferred for larger $V_{gs,Ms}$. From the second term in Eq. (9), smaller parasitic capacitance C_{N1} and C_{N2} are preferred for increasing the linearity. M9 is added in order to turn off M8 when clk is high for the purpose of reducing the parasitic capacitance $C_{p,N0}$[6]. The substrate of M5 and M7 should connect to the node N_1. That is because node N_1 is higher than V_{DD} once clk is from low to high and it can ensure that the substrate is the highest voltage in those two pMOS transistors.

A symmetrical gate bootstrapping switch is used in S_0 as illustrated in Fig. 6(b). The amount of the released charge could be reduced if the transistors Mt1 and Mt2 could turn off slightly before the switch transistor Ms, and is realized by connecting the gates of Mt1 and Mt2 to CLK instead of node N_0[8].

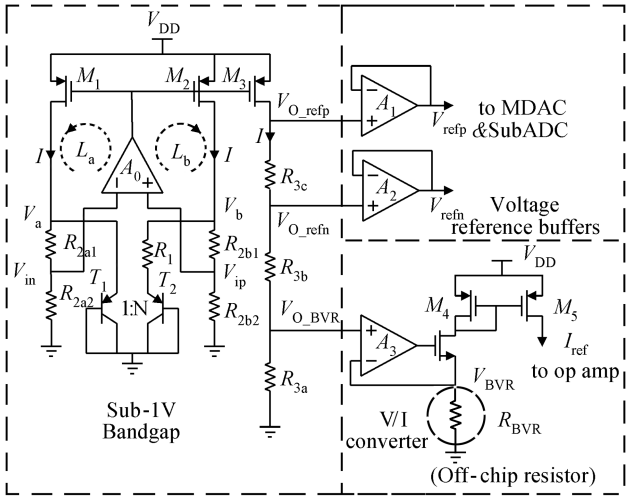

Fig. 7. I/V reference buffers with sub-1-V bandgap voltage reference.

3.4. *I/V* reference buffers with sub-1-V bandgap voltage reference (BVR)

Internal voltage reference is needed in the ADC for MDAC and subADC and an internal voltage reference buffer is used for smaller reference voltage error. Both of those need a temperature and supply voltage insensitive output voltage which is provided by BVR. The internal I/V reference buffers used in the ADC are illustrated in Fig. 7 including three parts: BVR[9], voltage reference buffers and V/I converter.

Since the conventional BVR output voltage is about 1.25 V, which is even larger than the supply voltage of the ADC, it is not suitable for this application. A sub-1-V BVR is adopted in the design. One of the limitations of implementing an op amp based on sub-1-V BVR circuits arises from the limitation imposed by the input common mode voltage of the op amp. In our design, the adopted BVR provide a fraction of the BVR output voltage by means of resistive division to reduce the input common mode voltage requirement of the op amp A_0. The pMOS input stage is used in this op amp and therefore, did not require low threshold transistors. A further observation of sub-1-V BVR is illustrated in Fig. 7, node V_a and V_b are virtual short and enforced to be the same potential, where $R_{2a1} = R_{2b1}$ and $R_{2a2} = R_{2b2}$. Therefore, the current (I) is given by

$$I = \frac{V_{EB2}}{R_2} + \frac{V_T \ln N}{R_1}, \quad (10)$$

$$V_{O\_BVR} = \frac{R_{3a}}{R_2}\left[V_{EB2} + \left(\frac{R_2}{R_1}\ln N\right)V_T\right]. \quad (11)$$

The sub-1-V BVR output voltage (V_{O_BVR}) is proportional to the ratio of R_3 ($R_3 = R_{3a}$) and R_2 ($R_2 = R_{2a1} + R_{2a2}$, or $R_{2b1} + R_{2b2}$. It is set to 0.2 V here.

Special attention should be paid to the connection of the op amp and vertical BJT. The inverting input of the op amp V_{in} should be connected to the T_1 side and the non-inverting input V_{ip} should be connected to the T_2 side, not vice versa. This is because there are two signal loops in the sub-1-V BVR, L_a and L_b. The loop gain of L_b is larger than that of L_a in that the impedance of V_b is larger than that of V_a. Therefore, L_a and L_b

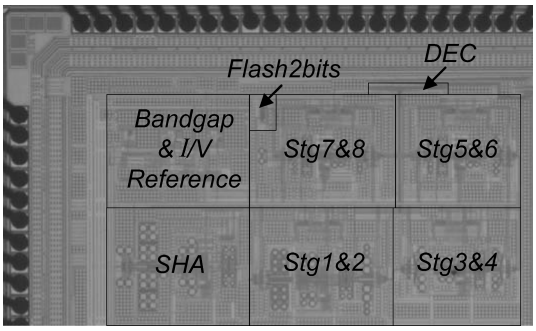

Fig. 8. Photomicrograph of the chip.

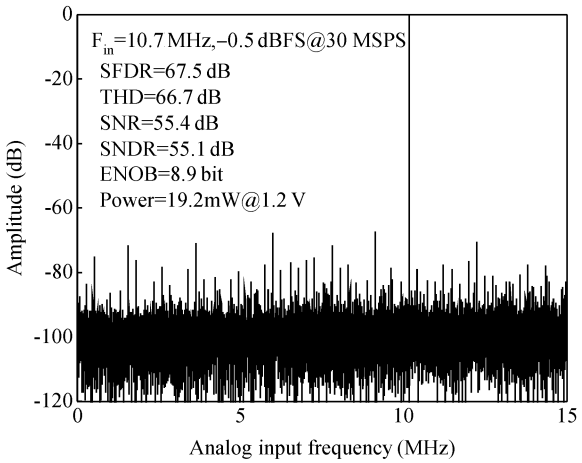

Fig. 9. Measured output spectrum for F_s = 30 MS/s and F_{in} = 10.7 MHz, –0.5 dBFS.

should be positive and negative feedback loops, respectively, with a view to stability.

Then the sub-1-V BVR is connected to the V/I converter and voltage reference buffers. The bias current to the op amp is controlled by an off-chip resistor R_{BVR} and the reference voltages connect to MDAC & sub ADC through voltage reference buffers. In particular, V_{o_refp} and V_{refp} have the same potential, and $V_{o_refn}$and V_{refn} have the same potential, and they are set to 0.9 V and 0.4 V, respectively, in this application. Although using the sub-1-V BVR, the supply voltage is limited by V_{o_refp} + $V_{dsat,\,M3}$, which is about 1.1 V theoretically. This is will be verified in the measured result in Section 4.

4. Implementation and measurement

The chip, a photomicrograph of which is shown in Fig. 8, was fabricated in a 0.13-μm 1-poly 8-copper CMOS process. The core area is 0.94 mm^2, and the maximum input swing is 1.0 V_{pp} differentially. The power dissipation of the ADC is 19.2 mW, and the sub-1-V BVR including I/V reference buffers is 3 mW operating at 1.2-V supply voltage. Figure 9 shows the measured output spectrum for an input frequency of 10.7 MHz under the condition of 30 MSPS, and the peak SNDR is 55.1 dB and peak SFDR is 67.5 dB where F_{in} = –0.5 dBFS. A further observation has been made in the dynamic range plot. In Fig. 10, the SNDR versus input amplitude V_{signal} is almost a straight line and extrapolated to near 0 dB. In Fig. 11,

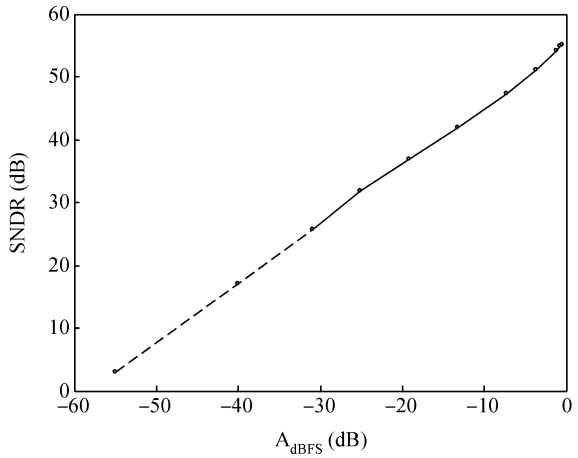

Fig. 10. SNDR versus A_{dBFS} @ 30 MS/s.

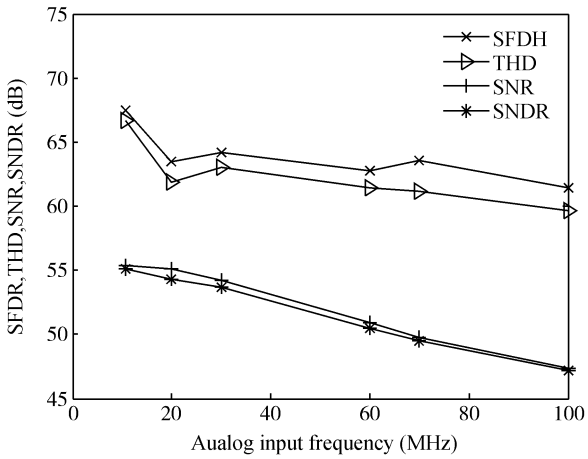

Fig. 11. Dynamic performance @ 30 MS/s.

conditions are the peak SNDR, SNR, total harmonic distortion (THD), SFDR versus input frequency from 10 to 100 MHz. It is observed that SNDR still maintains at 50 dB until 60-MHz input signal that corresponds to 8-bit ENOB and SFDR maintains at 62 dB until 100-MHz input signal that corresponds to 10-bit. As for static linearity, the peak INL is 0.77 LSB and the peak INL is 1.13 LSB as shown in Figs. 12(a) and 12(b), respectively. The measured result of the BVR and I/V reference is illustrated in Fig. 13. The differential voltages of V_{ref} and V_{refn} ($V_{refp-refn}$) and V_{BVR} for the supply voltage from 0.5 to 2 V are shown. The $V_{refp-refn}$ is 0.504 $\pm$ 0.004 from 1.2 to 2.0 V supply voltage and V_{BVR} = 0.210 $\pm$ 0.003 V where the voltage resolution in the measurement is 0.001 V. The reference voltages begin to drop below 1.1-V supply voltage which was explained in Section 3.4.

Table 1 summarizes the performance of this design. The figure-of-merit (FoM) is widely used to show the power efficiency of the ADC[10]. In this ADC, P = 19.2 mW is the power dissipation, effective number of bit (ENOB) = 8.9 bit is effective resolution, and ERBW = 60 MHz is effective resolution bandwidth.

$$\mathrm{FoM} = \frac{P}{2^{\mathrm{ENOB}} \times 2\mathrm{ERBW}} = 0.33\ \mathrm{pJ/step}. \qquad (12)$$

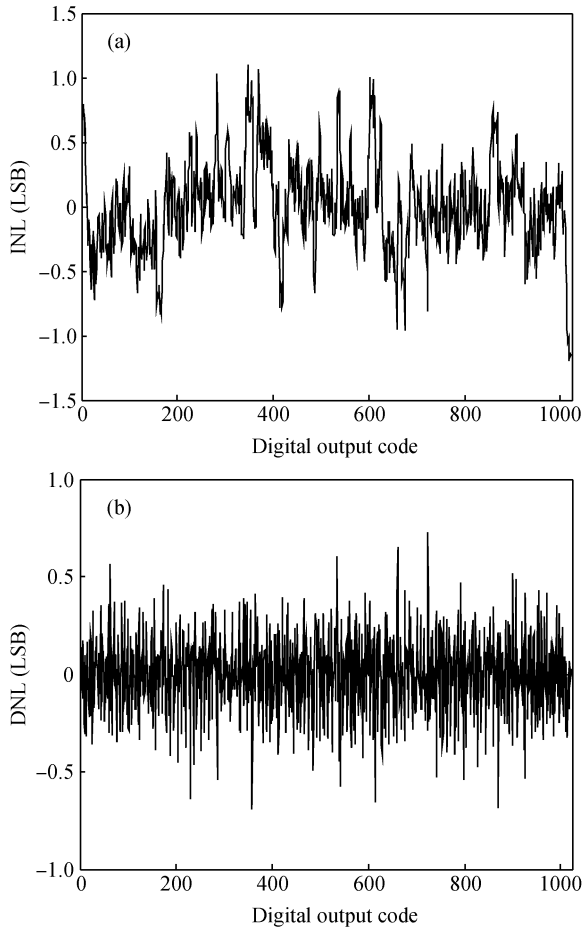

Fig. 12. (a) INL. (b) DNL.

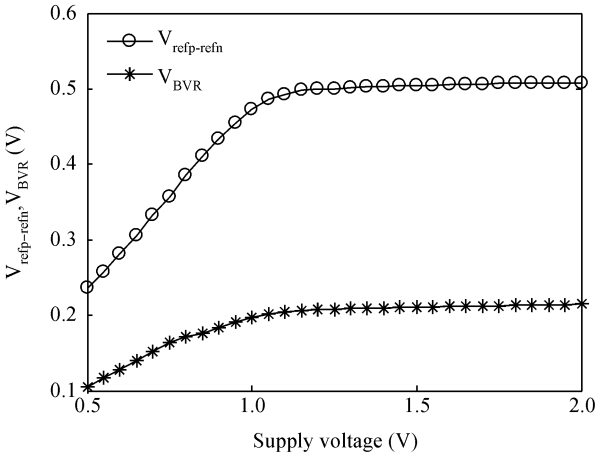

Fig. 13. Measured characteristics of the BVR and I/V reference buffers.

The FoM is 0.33 pJ/step. The measured FoM compared to previously published 10-bit ADCs is shown in Table 2.

5. Conclusion

The paper demonstrates the design approaches for low supply voltages in a deep-submicron CMOS process through a 1.2-V supply voltage 10-bit 30-MSample/s pipelined ADC in the 0.13-μm CMOS process. The challenges associated with this choice of supply voltage and process were overcome, such as limited dynamic range, poor analog characteristic devices, the limited linearity of analog switches and the embedded sub-1-V BVR. The solution includes: analyzing the relationship between the SNR, sampling capacitance and signal amplitude to achieve the specification; using a two-stage op amp to satisfy the large DC gain and signal amplitude with proper compensation, adopting boosting schemes to enhance the linearity of the switch, designing I/V reference buffers with embedded sub-1-V BVR. The measured results are presented and several previously published ADCs with similar specifications are compared.

Table 1. ADC performance summary.

Parameter	Value		
Resolution (bit)	10		
Input voltage range (Vpp)	1.0		
Sampling rate (MSPS)	30		
Technology	0.13 μm 1 Poly 8 Copper CMOS process		
Power (mW)	19.2 @ 1.2 V		
FoM (pJ/step)	0.33		
Area (mm^2)	0.94		
Peak INL (LSB)	1.13		
Peak DNL (LSB)	0.77		
F_{in} (MHz)	10.7	30	60
ENOB (bit)	8.9	8.6	8.1
SNDR (dB)	55.1	53.7	50.5
SNR (dB)	55.4	54.2	50.9
SFDR (dB)	67.5	64.2	62.8
THD (dB)	66.7	63.0	61.4

Table 2. Comparison with previously published work.

Reference	Sampling rate (MS/s)	Power (mW)	Process (μm)	SNDR (dB)	FoM (pJ/step)
JSSC 2003[11]	25	21	0.35	48.0	4.1
ESSCRIC 2005[12]	30	60	0.25	56.5	0.71
CICC 2007[13]	30	17	0.13	51.6	1.8
JoS 2008[14]	20/50	34/42	0.35	48.4/45.7	8.0/5.3
JoS 2008[15]	40	78	0.18	56.2	3.5
This work	30	19.2	0.13	55.1	0.33

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