A novel high voltage start up circuit for an integrated switched mode power supply

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Abstract: A novel high voltage start up circuit for providing an initial bias voltage to an integrated switched mode power supply (SMPS) is presented. An enhanced mode VDMOS transistor, the gate of which is biased by a floating p-island, is used to provide start up current and sustain high voltage. An NMOS transistor having a high source to ground breakdown voltage is included to extend the bias voltage range to the SMPS. Simulation results indicate that the high voltage start up circuit can start and restart as designed. The proposed structure is believed to be more energy saving and cost-effective compared with other solutions.

Key words: high voltage start up circuit; floating p-island; field ring
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1. Introduction

A high voltage start up circuit is required in an integrated switched mode power supply (SMPS) to provide an initial bias voltage to the control integrated circuits (ICs)[1, 2]. The high voltage current source allows low voltage control ICs to operate directly off rectified AC lines of up to 400 V. A start threshold voltage larger than their operating voltage is provided to the control ICs. The output voltage $V_{\rm D}$ of the high voltage start up circuit, which is also the supply voltage of control ICs, is monitored internally so that the high voltage start up circuit turns off when $V_{\rm D}$ increases above an internally set voltage $V_{\rm off}$. An external auxiliary voltage is generated and applied to $V_{\rm D}$ while the high voltage start up circuit is off. If $V_{\rm D}$ falls below a lower set voltage $V_{\rm reset}$, the high voltage start up circuit turns back on. This allows the start up circuit to reset itself when the SMPS's auxiliary voltage does not power up properly.

A resistor in series with a Zener diode is used to provide bias voltage for control ICs in Refs. [3, 4]. Enough current must be supplied through the resistor. The resistor must be of a high-wattage type because of the large voltage drop on it. Unfortunately, the waste of power is continuous even after the control ICs are started. Additionally, external components will increase the cost of the SMPS. A depletion mode MOS transistor or JFET is used in Refs. [5, 6]. This requires an additional mask to form these devices, which will also increase the cost of the SMPS. In Ref. [7] a floating p-region is used close to a source-body region of an n-VDMOS; the voltage of this floating region is used as a primary power-supply of a gate of a cell of an n-VDMOS. This idea is primarily proposed in Ref. [8]. However, once the floating p-island is grounded, the voltage can hardly re-build up as the leak current for an anti-biased PN junction is very small. This means the start up circuit in Ref. [8] cannot reset itself, which is needed for a start up circuit as mentioned above.

A novel high voltage start up circuit is presented in this paper. An enhanced mode VDMOS transistor, which has the same structure as the main power transistor in the SMPS, is used to provide the start up current and sustain high voltage. Its gate is biased by a floating p-island. This means that neither an additional mask nor external components are required, which makes the high voltage start up circuit more cost effective. An NMOS transistor having a high source to ground breakdown voltage is included to extend the bias voltage range to the SMPS. The high voltage start up circuit is switched off while the control ICs are working and consumes little energy. In section 2 the structure and operation of the proposed structure are illustrated. Section 3 presents simulation results by MEDICI[9] and discussions.

2. Structure and operation

Figure 1 shows a schematic cross-section of the proposed novel high voltage start up circuit, and Figure 2 illustrates its equivalent circuitry. The high voltage start up circuit includes a VDMOS transistor M1, a diffused resistor R1, NMOS transistors M2 and M3. The VDMOS transistor M1 is an n-channel, enhancement mode VDMOS transistor, with its source shorted to its substrate formed by a p-well and p-bury layer to eliminate the substrate bias effect. The gate of M1 is connected to a floating p-island, the drain is connected to the same terminal as the drain of the main power transistor in the SMPS at which a line voltage is applied, and the source is connected to the drain of NMOS transistor M2 and the first terminal of diffused resistor R1. The NMOS transistor M2 is an n-channel, enhancement mode MOS transistor, with its substrate grounded and gate connected to the second terminal of diffused resistor R1. N-wells are used to form the drain and source diffusion of M2 to sustain several dozen voltages. The breakdown voltage at the source of M2 must exceed 60 V to support a wide bias supply voltage range so a field plate is used. The diffused resistor R1 provides bias current to turn on M2. The bias current is kept small since it is conducted from the line voltage through M1 after the high voltage start up circuit is turned off. NMOS M3 shorts the gate of M2 to ground in order to turn the high voltage start up circuit off when $V_{\rm D}$ exceeds $V_{\rm off}$. V_1–V_4 are used in Fig. 2 to represent the node voltages for the convenience of illustration.

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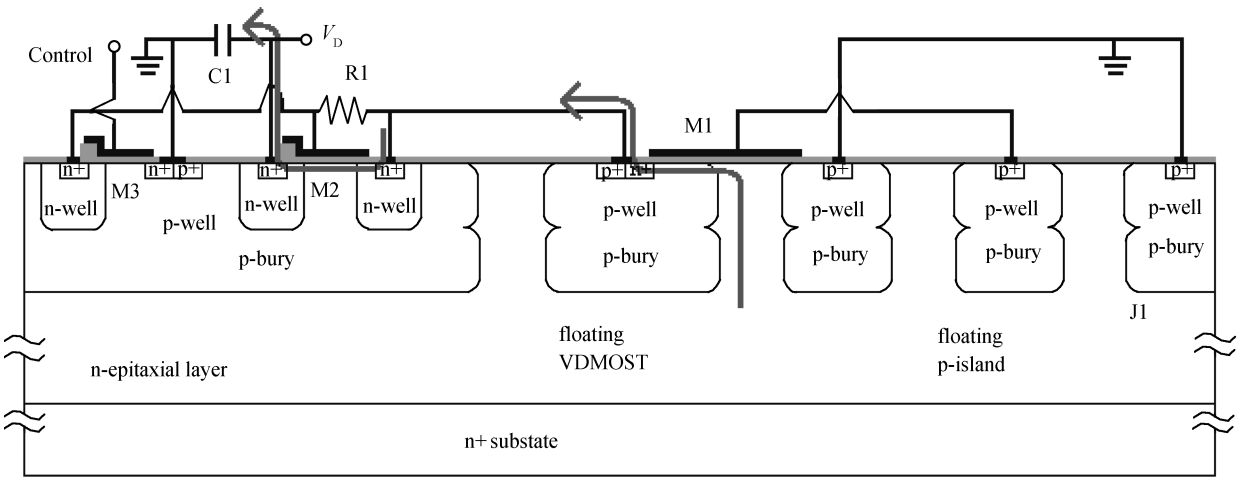

Fig. 1. Structure of the proposed high voltage start up circuit; the gray line represents current flow during start up.

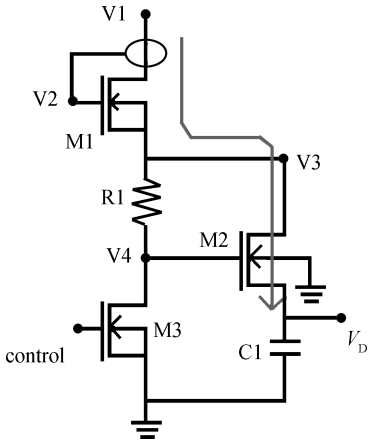

Fig. 2. Equivalent circuitry of the proposed structure; the gray line represents current flow during start up.V_1–V_4, V_D and "control" are the node voltages of the devices.

When the rectified line voltage is applied to the drain of VDMOS transistor M1, its body is fully depleted with its gate biased at a voltage of several dozen volts. M1 operates in its current saturation region. Since the source voltage of M1 is limited by its gate voltage provided by the floating p-island, most of the line voltage is dropped across the body of M1 thereby providing a buffer from the line voltage. This protects the NMOS transistor M2 and diffused resistor R1 connected to this node. The floating p-island works as a field limiting ring. The voltage of the floating p-island increases with the drain voltage of M1 at the beginning. When the drain voltage of M1 is large enough so that the depletion region of the anti-biased PN junction J1 near the floating p-island reaches the floating p-island, holes in the floating p-island will flow into the grounded p-region nearby. The field generated by the remaining negative charge will stop the voltage of the floating p-island increasing. If the drain voltage of M1 continues to increase, the n-region below the p-island will deplete and sustain the rest of the voltage. The punch-through voltage between the floating p-island and J1, which is also the gate voltage of M1, is calculated by Eq. (1) considering J1 as an abrupt junction[10].

$$V_{\mathrm{FP}} = \frac{qN_{\mathrm{B}}}{2\varepsilon_{\mathrm{S}}}\left[(r+d)^2\left(\ln\frac{r+d}{r}-\frac{1}{2}\right)+\frac{r^2}{2}\right], \quad (1)$$

where N_{B} is the doping concentration of the n-epitaxial layer, ε_{S} is the dielectric constant of silicon, r is the curvature radius of PN junction J1, and d is the distance between J1 and the floating p-island.

Once the gate–source voltage of M1 exceeds its threshold voltage, M1 turns on. The current flows through M1 and M2 to charge the capacitor C1 as indicated by the gray line shown in Figs. 1 and 2. When V_{D} is below V_{off}, the signal at the control terminal is logical low and the high voltage start up circuit is on, providing a high breakdown voltage and a high current. Once V_{D} exceeds V_{off}, the control signal applied at the gate of M3 will become logical high. M3 turns on then and shorts the gate of M2 to ground, thereby providing high impedance between the drain of M1 and the output of the high voltage start up circuit. If V_{D} drops down below V_{reset} for some reason after start up, the control signal will become logical low and turn off M3, reinitiating the start up sequence.

3. Simulation results and discussion

The distance d between J1 and the floating p-island should be carefully designed according to Eq. (1) so that the voltage of the floating p-island is larger than the sum of V_{off}, the threshold voltage of M1 and M2, ensuring a large enough output voltage V_{D}. Figure 3 shows the voltage of the floating p-island V_{FP} versus the drain voltage V_{drain} of M1 in the range of 0 to 400 V under different d. The voltage of the floating p-island increases when d increases, the same as indicated by Eq. (1). In this design $d = 4\ \mu$m is chosen to ensure a large enough output voltage but not too much to exceed the breakdown voltage of the gate oxide. V_{FP} is 20 V under V_{drain} = 100 V and 30 V under V_{drain} = 400 V. V_{FP} is not the same under different V_{drain} because in our technology PN junction J1 is not strictly an abrupt junction but a graded junction.

Figure 4 shows the start up and re-startup sequence of the high voltage start up circuit under a rectified line voltage of 300 V. 0–0.2 s is the start up phase, 0.2–0.3 s is when the control ICs are working and 0.3–0.5 s is the re-startup phase. A

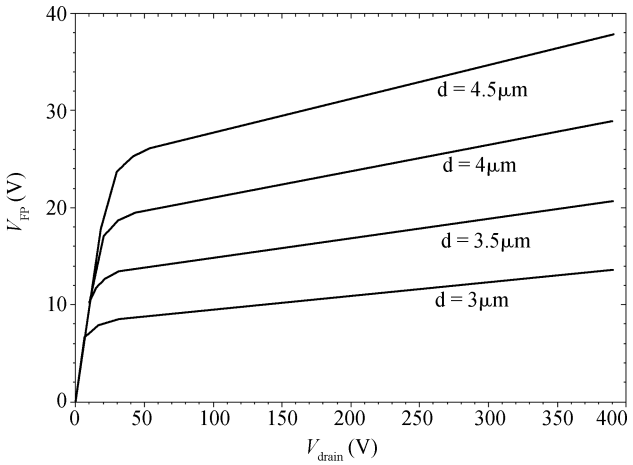

Fig. 3. Voltage of the floating p-island V_{FP} versus the drain voltage V_{drain} of M1 in the range of 0 to 400 V under different d, which is the distance between J1 and the floating p-island in Fig. 1.

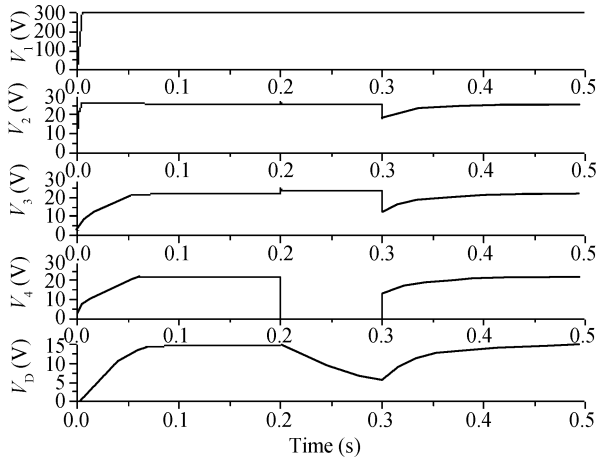

Fig. 4. Node voltages of the high voltage start up circuit shown in Fig. 2 during the start up and re-startup phases. 0–0.2 s is the start up phase, 0.2–0.3 s is when the control ICs are working, and 0.3–0.5 s is the re-startup phase.

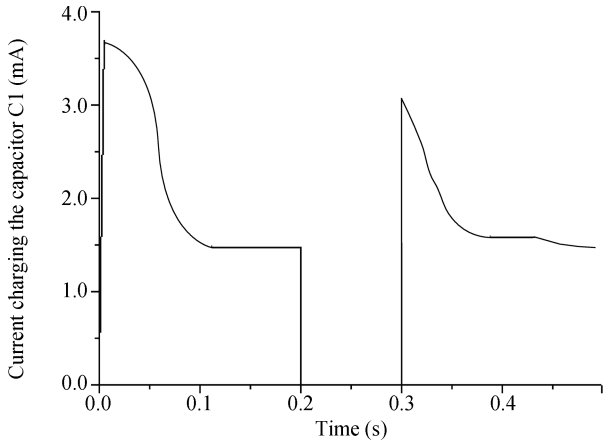

Fig. 5. Current charging the capacitor C1 during the startup and re-startup phases. A current larger than 1 mA is provided during the start up and restart phases. 0–0.2 s is the start up phase, 0.2–0.3 s is when the control ICs are working, and 0.3–0.5 s is the re-startup phase.

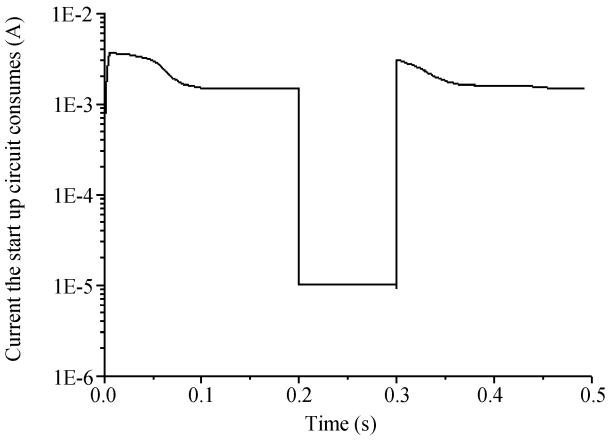

Fig. 6. Current that the high voltage start up circuit consumes. Little current is consumed when the control ICs are working. 0–0.2 s is the start up phase, 0.2–0.3 s is when the control ICs are working, and 0.3–0.5 s is the re-startup phase.

capacitor C1 of 10 μF and a resistor of 10 kΩ are connected to the source terminal of M2. The resistor is used to simulate the current consumed by the control ICs. The rectified line voltage, which is also the drain voltage V_1 of M1 as shown in Fig. 2, is set to increase from 0 to 300 V in 5 ms. The gate voltage V_2 of M1, which is also the voltage of the floating p-island V_{FP}, increases from 0 to 25 V along with the rectified line voltage as shown in Fig. 4. The voltages of other nodes increase slowly because of the large capacitance of C1. The control NMOS transistor is turned on at t = 0.2 s to turn off the high voltage start up circuit and turned off at t = 0.3 s to simulate the re-startup phase. The gate of M2 is shorted to ground when M3 turns on, shown as V_4 in Fig. 4. The voltage on the capacitor C1, which is also the output voltage V_D of the high voltage start up circuit, falls when M3 turns on because there is no charging current from M2. The step up of V_3 at t = 0.2 s is illustrated below. At t = 0.2 s M2 turns off and requires no current from M2. The gate-source voltage of M1 will decrease because there is no need for large current. Because the gate voltage of M1 is fixed at V_{FP}, which is a certain value under a certain rectified line voltage, the source voltage V_3 of M1 has to increase. At t = 0.3 s, M3 turns off, the gate of M2 is charged up by R_1 as shown in Fig. 4 and M2 turns on again. The high voltage start up circuit enters the re-startup phase and the output voltage V_D starts to increase. The drop of V_2 and V_3 is because the large current to charge C1 is needed again.

Figure 5 shows the current of the source terminal of M2, which is the charging current to the capacitor C1. A current larger than 1 mA is provided during the start up and restart phases. It can be adjusted to fulfill the demands of the control ICs by changing the gate width of M1 and M2. The current is the largest at the beginning of each phase because the gate-source voltage of M1 decreases gradually during the start up and re-startup phases due to the charging of the capacitances. Figure 6 shows the drain current of M1, which is the current that the high voltage start up circuit consumes. When the control ICs are working, the high voltage start up circuit is off. The current it consumes is determined by the resistance of the diffused resistor R1 and is very small as shown in Fig. 6.

4. Conclusions

A novel high voltage start up circuit is presented in this paper. An enhanced mode VDMOS transistor is used to provide the start up current and sustain high voltage. Its gate is biased by a floating p-island. An NMOS transistor having a high source to ground breakdown voltage is included to extend the bias voltage range to the SMPS. Simulation results by MEDICI indicate that the circuit can start and restart as designed. The novel structure presented is believed to be more cost effective and energy saving compared to other solutions.

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