A dual-band frequency synthesizer for CMMB application with low phase noise

Yu Peng(于鹏)[1,†], Yan Jun(颜峻)[1], Shi Yin(石寅)[1], Dai Fa Foster(代伐)[2]

(1 Institute of Semiconductors, Chinese Academy of Sciences, Beijing 100083, China)
(2 Department of Electrical & Computer Engineering, Auburn University, Auburn, AL 36849-5201, USA)

Abstract: A wide-band frequency synthesizer with low phase noise is presented. The frequency tuning range is from 474 to 858 MHz which is compatible with U-band CMMB application while the S-band frequency is also included. Three VCOs with selectable sub-band are integrated on chip to cover the target frequency range. This PLL is fabricated with 0.35 μm SiGe BiCMOS technology. The measured result shows that the RMS phase error is less than 1° and the reference spur is less than –60 dBc. The proposed PLL consumes 20 mA current from a 2.8 V supply. The silicon area occupied without PADs is 1.17 mm^2.

Key words: CMMB; PLL; frequency synthesizer; phase noise; sigma–delta modulator
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1. Introduction

China Mobile Multimedia Broadcasting (CMMB) is a mobile television and multimedia standard developed and specified in Mainland China by the State Administration of Radio, Film, and Television (SARFT). It has been described as being similar to Europe's DVB-H standard for digital video broadcast from satellites to handheld devices. The CMMB standard specifies two bands of frequencies which are 2.6 GHz (S-band) and 474–858 MHz (U-band), together constituting a satellite and terrestrial complementary network. The S-band signal is received directly from satellites, and the U-band signal is broadcasted terrestrially in hundreds of cities throughout the country. This complementary network structure provides both high quality signal in urban areas and good signal coverage in a wide range of rural areas. As a result, anyone equipped with a CMMB terminal device can enjoy the program service wherever he or she goes in China.

Despite the advantage of the two-band network structure, it makes it harder to satisfy the frequency specification with an on-chip phase-lock-loop (PLL). To cover the widely separated two-band, a frequency plan should be considered carefully to minimize current consumption and silicon area. In this RFIC, both frequency dividing and polyphase filter techniques are used so that a continuous VCO frequency strategy can be applied. Three VCOs with the same circuit structure can be divided-by-4 for the U-band frequency or fed through a polyphase filter for the S-band frequency. Phase noise is another important parameter for the high performance RFIC because it degrades the carrier-to-noise ratio (C/N or CNR) of a receiver. Both integer-N and fractional-N techniques are used in this work to take advantages of each structure. A hybrid multi modulus divider (MMD) with a large range of division ratio is introduced along with an integrated $\Sigma\Delta$ modulator. A fast reset phase frequency detector (PFD) is described cooperating with the fast switching charge pump (CP) to minimize in-band phase noise and reference spurious. The architecture of this PLL is illustrated in Fig. 1.

This paper discusses the frequency plan for the wide-band PLL and phase noise requirement, and highlights the block feature.

2. PLL design issue

2.1. Frequency plan

Modern RFICs receive and down-convert RF signals by mixing with a quadrature local oscillator (LO). A common way to generate a quadrature LO is to divide the voltage controlled oscillator (VCO) frequency by an even order while the in-phase/quadrature output of the LO is drawn with equidistance in the delay-latch loop. This approach is operational for the U-band frequency. For the S-band frequency, however, it will consume more current if divided-by-2 from 5.2 GHz VCO due to the process limitation, and this is therefore inappropriate for low power applications, such as CMMB hand-held devices. The solution to this issue lies in not dividing but filtering the VCO frequency through a polyphase filter. The narrow S-band frequency (2635–2660 MHz) is also suitable for such an operation to guarantee the magnitude matching between IQ LO outputs. The most important advantage for this approach is the frequency continuity, so that the U-band VCO can be reused for the S-band frequency. Before being divided-by-4, the original frequency range for the U-band VCO should be 1896–3432 MHz which happens to include the S-band frequency. The

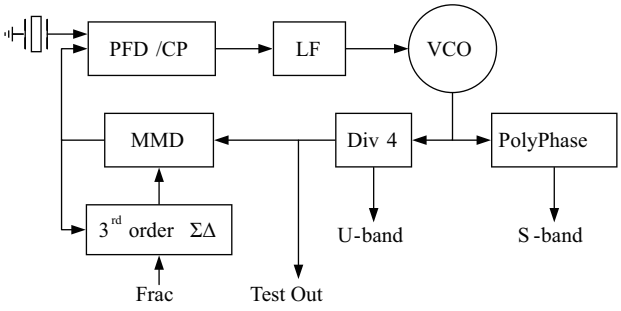

Fig. 1. Block diagram of the PLL.

† Corresponding author. Email: pyu@sci-inc.com.cn
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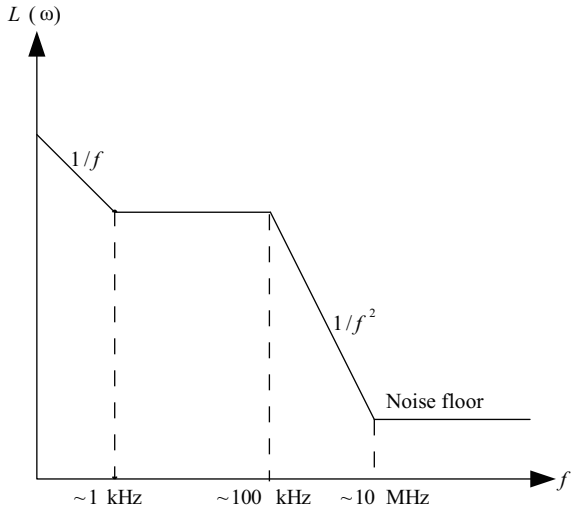

Fig. 2. Phase noise spectrum in locked PLL.

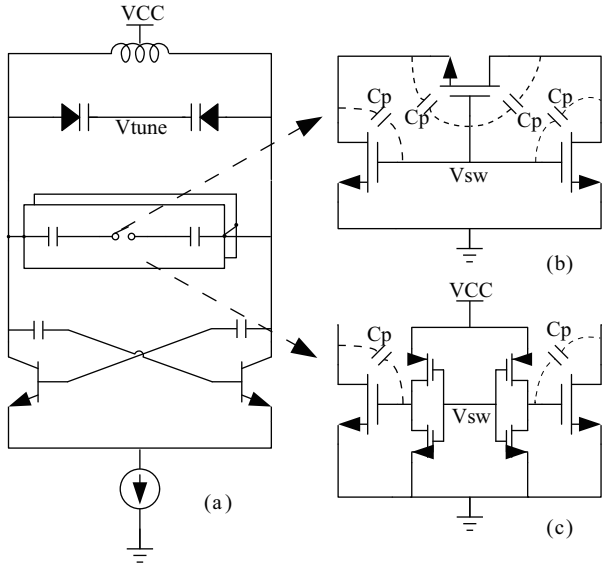

Fig. 3. (a) VCO architecture. (b) Conventional switch with large parallel parasitic capacitance C_p. (c) Proposed switch with small size inverters to isolate parasitic coupling.

absence of a high-frequency separated-band VCO could save both area and power. Being divided-by-4 could also benefit the phase noise performance by reducing the VCO phase noise by an amount of $20\lg N$ dBc/Hz, where N is 4 in this situation.

2.2. Phase noise requirement

Orthogonal frequency division multiplexing (OFDM) has been widely applied in wireless communication/broadcasting systems such as digital video broadcasting (DVB-T/H), digital audio broadcasting (DAB), and CMMB due to its ability to combat impulsive noise and multipath effects and make better use of the system available bandwidth. Phase noise must be carefully considered when dealing with any of these communication systems since an accurate prediction of the tolerable phase noise can allow the system and RF designers to relax the specifications. Phase noise requirements come from two considerations: (a) interferer strength and (b) CNR degradation duo to phase noise. For the highest data-rate, the standard uses 16QAM with OFDM in an 8 MHz channel bandwidth[1]. Assuming there is an adjacent interferer 37 dB stronger than the desired channel and the minimum CNR is 11.3 (Rayleigh channel)[2], we therefore have:

$$\begin{aligned} L(8\text{MHz}) &= -\text{CNR} - [10\lg(8\,\text{MHz}) + 37] \\ &= -117.3\ \text{dBc/Hz}. \end{aligned} \tag{1}$$

A typical phase noise spectrum is shown in Fig. 2. If we make the contribution of noise floor obsolete, the PSD is:

$$S_\phi(f) \approx P_c A \frac{f_a^2}{f^2}, \tag{2}$$

where P_c is the average power of the oscillator, f_a is the frequency offset in the $1/f^2$ region of the spectrum, and A is the phase noise at that spot frequency. This is a conservative estimate since the phase noise in the $1/f$ and flat regions is smaller than in Eq. (2). The maximum noise-to-carrier ratio (NCR) of a single subcarrier introduced by phase noise is:

$$\begin{aligned} \text{NCR}_{\max} &= \frac{1}{\text{CNR}_{\min}} = \int_{-\infty}^{+\infty} \left(1 - \sin c^2 \frac{f}{f_U}\right) S_\phi(f) \\ &= P_c A f_a^2 \int_{-\infty}^{+\infty} \left[1 - \sin c^2\left(\frac{f}{f_U}\right)\right] \frac{1}{f^2} \mathrm{d}f \\ &= \frac{2}{3} \frac{P_c A f_a^2}{f_U} \pi^2, \end{aligned} \tag{3}$$

where $f_U = 2.441$ kHz is the subcarrier spacing in CMMB. Assuming P_C we can derive that the phase noise should be lower than –86 dBc/Hz @ 100 kHz and –106 dBc/Hz @ 1 MHz.

3. Circuit design

3.1. VCO circuits

To extend the frequency range while keeping K_{VCO} small, we propose a digital split-tuned LC-VCOs architecture. The concept is to coarsely tune the VCO with a bank of switched capacitors, while finely tuning it with varactors. The VCO frequency tuning range is targeted at 1896–3432 MHz. To save chip area, each of the three VCOs contains a symmetric inductor together with a bank of switched capacitors compositing the resonator tank. Two cross coupled NPN-transistors provide the negative G_m with a current consumption of 6 mA. A commonly used capacitor switch is shown in Fig. 3(b). To minimize the flicker noise contribution to phase noise, the size of the NMOS should be large enough, which, on the other hand, limits the available tuning range because of the added parasitic capacitance. This contradiction can be solved by using switches shown in Fig. 3(c). In each branch of the switched capacitor path, a large NMOS can be completely turned off by a small inverter which isolates the coupling between the positive and negative sides of the tank.

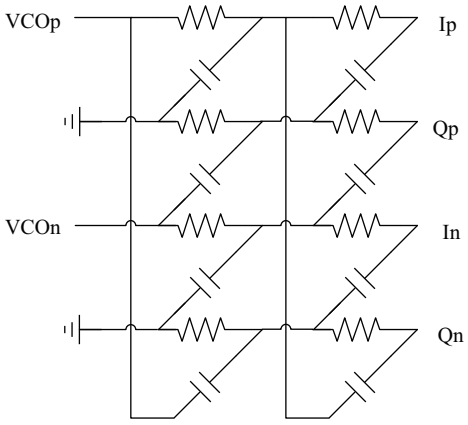

Fig. 4. Second-order polyphase filter.

3.2. LO generator

The output of the VCO is fed to the LO generator and thereby converted to the U-band or S-band IQ frequency. For U-band, a divided-by-4 divider is applied by cascading 4 current mode logic (CML) latches in a loop. The CML circuitry is preferred for its advantages of high speed, low voltage swing and differential operation over the CMOS competitor. For the S-band, the VCO frequency passes through a second-order polyphase filter as shown in Fig. 4. A first-order polyphase filter has exactly the same magnitude response between the I-branch and the Q-branch at one specific frequency spot, while a second-order filter has two spots. This means that the second-order polyphase filter has almost the same I/Q magnitude response for narrow band applications and good quadrature phase matching. The polyphase filter does not degrade the phase noise performance since the resistors are chosen to be small.

3.3. MMD

Compared with the NPN device in 0.35 μm technology, the MOSFET devices show a disadvantage in terms of operation speed. While the CML circuit can work at several GHz, the CMOS logic circuit can only run under 300 MHz. On the other hand, the CML circuit consumes more current than CMOS. To utilize the advantages of both approaches, a hybrid MMD built up with CML and CMOS is developed to provide the desired speed capability and to save current. Each stage of MMD consists of D-latches and AND-gates. In this work, a novel D-latch with integrated AND operation is proposed. There is already a traditional D-latch with the same function as shown in Fig. 5(a). The limited headroom in the 2.8 V supply voltage prevents the D-latch in Fig. 5(a) being used. We can reconstruct the D-latch by relocating Q_A and Q_B from the vertical to the horizontal and save V_{BE} headroom as shown in Fig. 5(b). When A_P and B_P are both high, I_N is larger than I_P, and therefore V_P is larger than V_N. Notice that $I_N - I_P$ decreases as R_E increases, so the value of R_E should be small. When either A_P or B_P is high, $I_P - I_N$ increases as R_E increases. So R_E should be large to keep the difference between V_P and V_N large. This contradiction indicates that the value of R_E should be chosen carefully to meet the requirements of both conditions. Since the resistors R and R_E are implemented by using an accurate polysilicon resistor and the tail current I is biased by the bandgap reference source, the proposed approach is process-voltage-temperature (PVT) tolerant. Figure 6 shows the transient simulation result of the proposed D-latch which can be functional under input clock up to 2 GHz. The CMOS dividers working at low frequency provide a large range of division ratio.

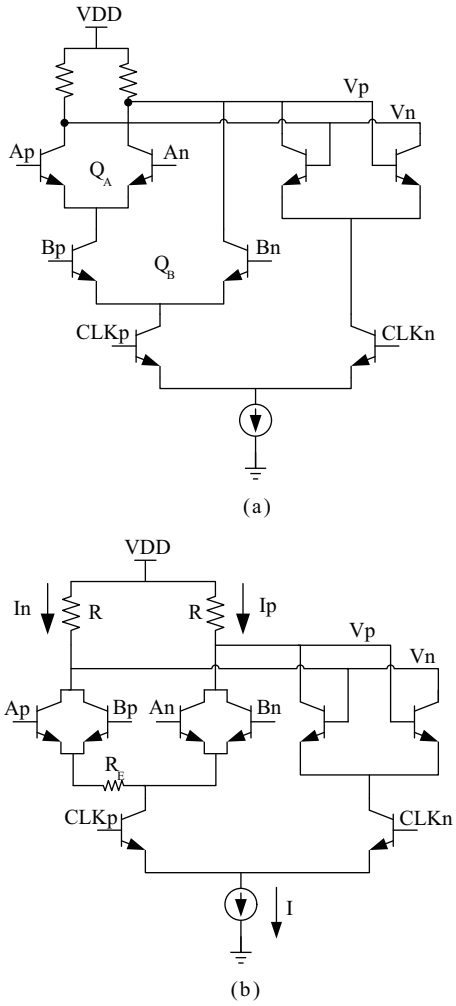

Fig. 5. (a) Conventional-latch with AND function. (b) Proposed D-latch with AND function.

3.4. ΣΔ modulator

A third-order multi stage noise shaping (MASH) ΣΔ modulator has a better in-band noise shaping effect compared to a third-order single stage multiple feed-forward (SSMF) structure, while MASH brings in more quantization noise out-of-band. Moreover, MASH has a wide spread output bit pattern that tends to increase the CP turn-on time making Vtune more sensitive to substrate noise and injected current[3, 4]. Consequently, the SSMF approach is a more suitable candidate than MASH.

3.5. PFD and CP

The characteristics of PFD and CP influence the PLL in-band noise dramatically. The reset time of the PFD should be short enough to cut off the current in CP from injecting into the loop filter. In this work, a TSPC DFF based PFD is utilized and the simulation result indicates that the reset time is

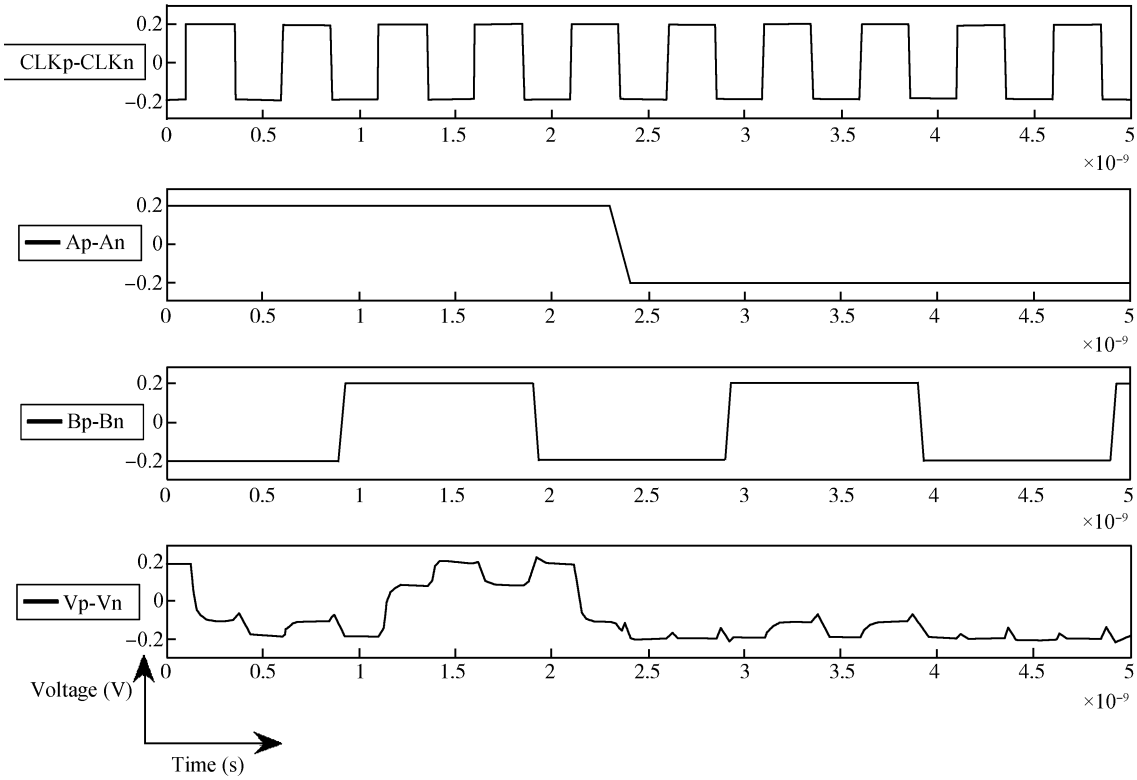

Fig. 6. Timing diagram of the proposed D-latch.

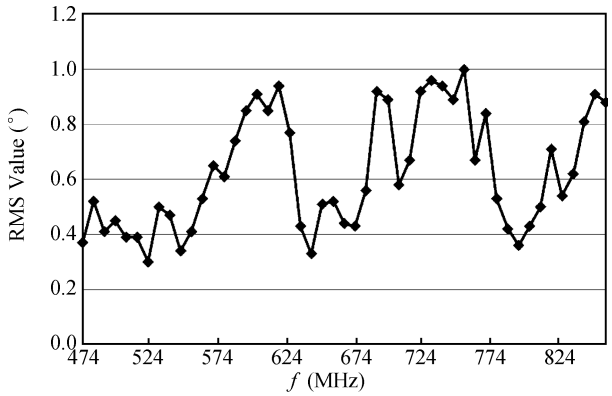

Fig. 7. RMS phase error.

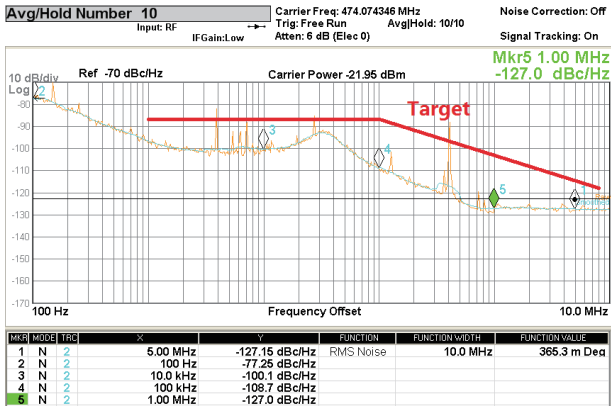

Fig. 8. U-band integer-N phase noise @ 474 MHz.

200 ps. A fast PFD needs a fast cooperating CP to eliminate the dead-zone effect which could increase in-band phase noise. To shorten the source/sink switch turn on/off time, switches are placed at the gate node of source/sink output MOSFETs. Compared with placing the switch at the source/drain node, the gate-switch has no static current flowing through it and therefore helps to decrease both switching time and reference spurious.

4. Measurement results

Figure 7 shows the RMS phase error integrated from 100 Hz to 10 MHz for the U-band LO frequency and we can see that these RMS values are less than 1°. Note that Figure 7 is a result from a combination of integer-N mode and fractional-N mode. Although the fractional-N technique is beneficial for in-band phase noise, it suffers from quantization noise out of loop-band-width. Therefore integer-N mode is preferable for low frequency with small division ratio (DR). Besides, the CP characteristics, such as source/sink current matching and noise contribution, could also affect phase noise dramatically since they vary with the CP output node voltage. Figures 8 and 9 show the U-band phase noise of integer-N mode and fractional-N mode respectively. We can see that for these two spectra integer-N mode with a DR of 237 has better phase noise performance than fractional-N mode with a DR of 28.9, because of the smaller loop-band-width and freedom from out-of-band quantization noise. Figure 10 shows an S-band phase noise at 658.75 MHz which is divided-by-4 for testing purposes, so the actual LO frequency within the RFIC is 2635 MHz, one of three CMMB S-band frequency spots. We can also see that the phase noise specification mentioned in section 2.2 is met in both modes.

Table 1. Comparison between this work and related frequency synthesizers.

Parameter	Ref. [5]	Ref. [6]	Ref. [7]	This work
Application	DVB-H	DVB-T	DVB-T	CMMB
Technology	0.18 μm CMOS, 1.8 V	0.18 μm CMOS, 1.8 V	0.18 μm CMOS, 1.8 V	0.35 μm SiGe, 2.8 V
Frequency range (MHz)	470–890 1400–1800	48–860	975–1960	474–858 (U-band) 2635–2660 (S-band)
VCO core	Two LCs	Three LCs	Single LC	Three LCs
Loop bandwidth (kHz)	60	200	92.5	200
Phase noise (dBc/Hz)	–94 @ 10 kHz –127 @ 1 MHz	–90 @ 10 kHz –105 @ 1 MHz	–91 @ 10 kHz –123 @ 1 MHz	–95 @ 10 kHz –113 @ 1 MHz
RMS phase error	0.5°	2°	1°	1°
Die area excluding PADs (mm^2)	2.45	1.2	1.27	1.17

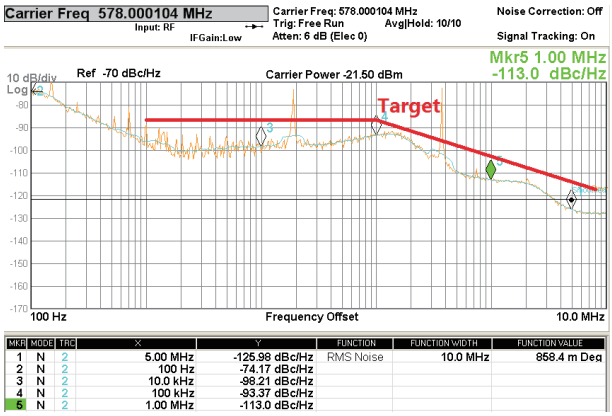

Fig. 9. U-band fractional-N phase noise @ 578 MHz.

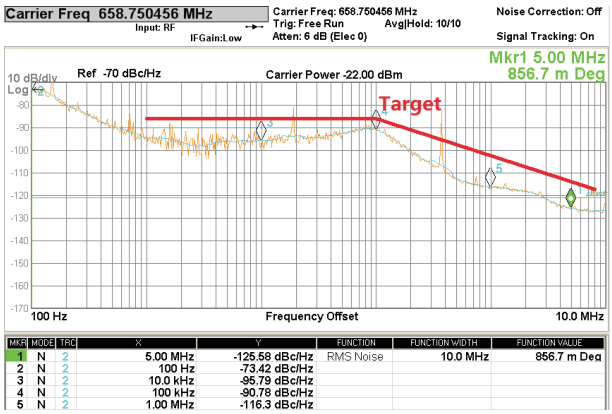

Fig. 10. S-band phase noise @ 658.75 MHz (after divide-by-4).

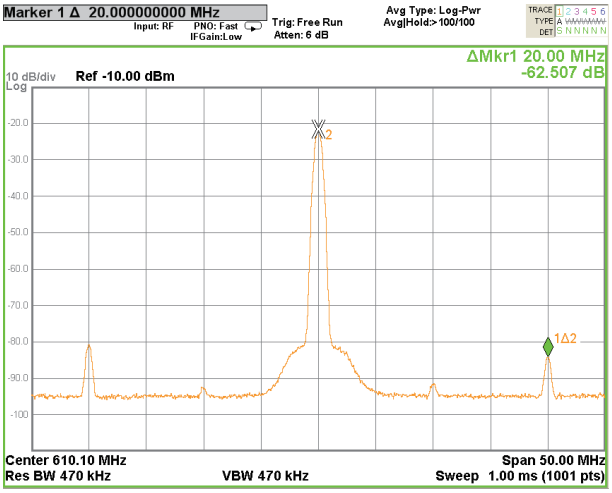

Fig. 11. U-band spectrum and reference spur for fractional-N mode.

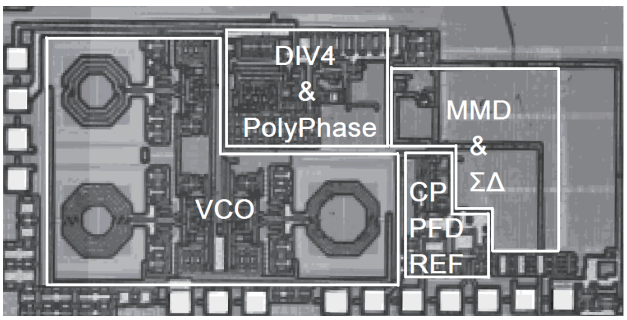

Fig. 12. PLL die photograph.

Figure 11 shows a U-band spectrum and reference spur at 610 MHz under fractional-N mode. It can be seen that there is hardly any fractional spur for the SSMF structure of the $\Sigma\Delta$ modulator and the reference spur is less than 60 dBc/Hz.

Figure 12 shows a die paragraph of this dual-band frequency synthesizer RFIC with an area of 1.17 mm^2.

A performance comparison between the proposed PLL and other related frequency synthesizers is listed in Table 1.

5. Conclusion

In this paper, a dual-band low phase noise LC-VCO frequency synthesizer for CMMB application is designed and implemented in 0.35 μm SiGe technology. A novel switch for a capacitor array VCO is presented, which can isolate parasitic coupling and increase the tuning range. A hybrid MMD composed with reformed CML D-latch and CMOS logic works up to 2 GHz under a 2.8 V supply and provides a large division ratio range. Measurement results show this PLL satisfies the requirements of the CMMB specification. The proposed frequency synthesizer has been applied to a CMMB receiver.

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