A direct-conversion WLAN transceiver baseband with DC offset compensation and carrier leakage reduction

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Abstract: A dual-band direct-conversion WLAN transceiver baseband compliant with the IEEE 802.11a/b/g standards is described. Several critical techniques for receiver DC offset compensation and transmitter carrier leakage rejection calibration are presented that enable the direct-conversion architecture to meet all WLAN specifications. The receiver baseband VGA provides 62 dB gain range with steps of 2 dB and a DC offset cancellation circuit is introduced to remove the offset from layout and self-mixing. The calibration loop achieves constant high-pass pole when gain changes; and a fast response time by programming the pole to 1 MHz during preamble and to 30 kHz during receiving data. The transmitter baseband employs an auto-calibration loop with on-chip AD and DA to suppress the carrier leakage, and AD can be powered down after calibration to save power consumption. The chip consumes 17.52 mA for RX baseband VGA and DCOC, and 8.3 mA for TX carrier leakage calibration (5.88 mA after calibration) from 2.85 V supply. Implemented in a 0.35μm SiGe technology, they occupy 0.68 mm^2 and 0.18 mm^2 die size respectively.

Key words: direct-conversion; WLAN; DC offset; carrier leakage; calibration; SiGe technology
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1. Introduction

The wireless industry has experienced a significant growth in previous years. The IEEE 802.11b standard has been extensively incorporated into battery-driven mobile devices, such as cell phones, PDAs and mobile PCs, and is used throughout the world in corporate offices, hot spots such as airports and railway stations, and also in home networks. Recently, new WLAN standards such as the IEEE 802.11a and the recently ratified IEEE 802.11g based on orthogonal frequency division multiplexing (OFDM) pose significant implementation challenges in the front-end. Low in-band phase noise, high linearity and accurate quadrate matching are required. In order to meet the strict specification about power consumption and high linearity, direct conversion and the OP-AMP-RC low-pass filter are used.

However, many significant technical challenges are involved with direct-conversion design: (a) receiver DC offsets, (b) second order intermodulation, (c) transmitter carrier leakage, (d) I/Q amplitude and phase mismatch, and (e) $1/f$ noise at baseband. There are several recent methods to handle carrier leakage. Balancing techniques[1] are frequently used, however, tolerances rarely allow more than 30 dB suppression of the carrier leakage. Another possibility is to add a correctly leveled and phase shifted part of the carrier signal to the RF signal[2], but this procedure requires very complex mixers. The third method[3, 4] is to use a calibration loop with on-chip power detector and DA to suppress the carrier leakage, however, this method requires a complex power detector which consumes a large area and adds design complexity. Therefore, the goal of this work is to develop a simple, robust, and easy to implement algorithm for canceling carrier leakage.

In this paper, we report a dual-band direct-conversion WLAN transceiver baseband in 0.35 μm SiGe process for IEEE 802.11a/b/g applications. Compared with published works, this design achieved excellent performance with low cost and high performance by employing several unique solutions in receiver DC offset compensation and transmitter carrier leakage rejection calibration. We describe the receiver baseband architecture and the detailed circuit implementation: (1) a large controlled range variable gain amplifier (VGA) based on resistive feedback configuration with high linearity; (2) a DC offset compensation circuit with two feedback loops to achieve constant high-pass cutoff frequency and a fast response time. We also present the transmitter baseband architecture and a carrier leakage calibration loop with on-chip AD and DA to suppress the carrier leakage.

2. Receiver baseband VGA & DCOC

Figure 1 shows a detailed block diagram of the receiver baseband section. Following the mixer, a sixth-order low-pass Butterworth filter is used, which is designed for 9.5 MHz bandwidth, and uses automatic calibration for corner frequency over all temperature, power supply and process variation. The baseband VGA consists of two stages of VGAs providing 62 dB gain range with 2-dB steps, and the gain is controlled by a 5-

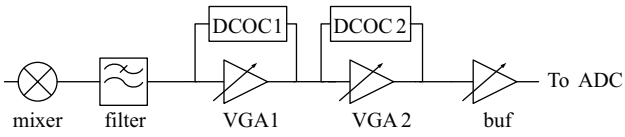

Fig. 1. Block diagram of receiver baseband.

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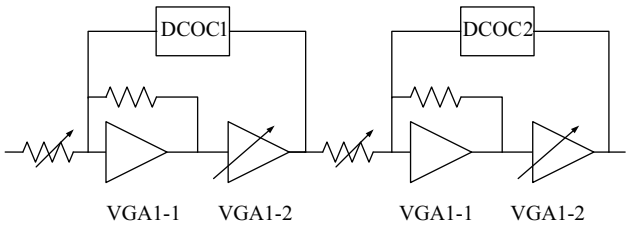


Fig. 2. Block diagram of baseband VGA.

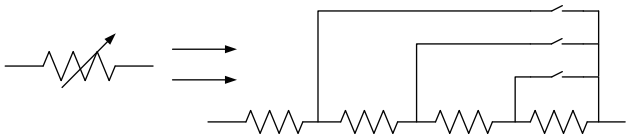


Fig. 3. One-hot switched resistor.

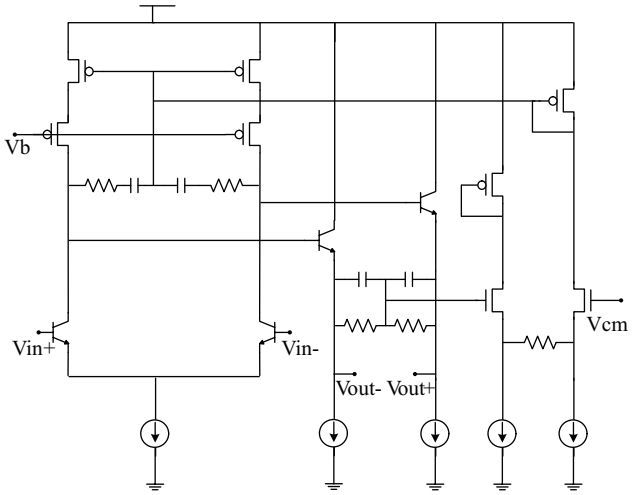


Fig. 4. Schematic of OP-AMP.

bit digital signal with a total of 31 steps. DC-servo loops are used around all gain stages to remove DC offsets introduced from LO self-mixing and layout mismatch.

2.1. BBVGA

The baseband VGA is designed to provide a gain range of 62 dB with a gain step of 2 dB, and is placed after the baseband filter for good linearity. The detailed circuit schematic of the VGA is illustrated in Fig. 2.

The first programmable gain block VGA1 consists of two stages of amplifiers while VGA2 also has two stages. Each stage amplifier uses resistive feedback configuration, whose gain is set by the ratio of the feedback resistors to the input resistors[5]. To adjust the stage gain, either the feedback or input resistors need to be varied. Each stage varies input resistors to achieve gain programmability. The MOS transistors are used to switch the input resistors, as is shown in Fig. 3. Thus, large sizes should be used to assure that switch on-state resistance are much smaller than the switched resistors so that the designed gain would not be influenced when switching, however, the sizes should not be too large so that the phase margin of the operational amplifier are not be reduced.

With the same configuration, the former three stages step two gains by 16 dB, and the fourth stage steps seven gains by 2 dB. Thus, the four stages cover a linear 62 dB gain range in 2-dB steps with a total of 31 steps.

In Fig. 4, the schematic of the proposed OP-AMP used in an amplifier is shown. It consists of a differential input stage with cascode configuration, an output stage, and a common-mode feedback (CMFB) circuit. To achieve higher swing/linearity, the CM level is detected by an RC network instead of two coupled differential pairs[6]. The OP-AMP employs frequency compensation, and the stability is obtained by a proper choice of R and C. Increasing the open-loop gain of OP-AMP reduces non-linearity of the amplifier, so the OP-AMP's gain should be high enough to assure the amplifier's linearity. The simulation shows that the OP-AMP can achieve GBW of 1.76 GHz, phase margin of 72°, DC gain of 60 dB, and power consumption of 0.85 mA.

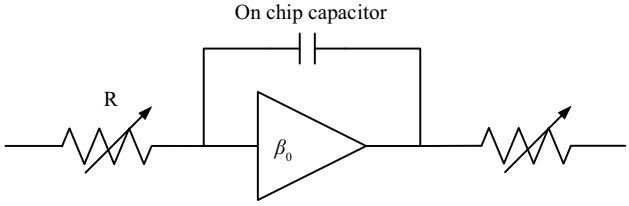


Fig. 5. Schematic of DC offset cancellation.

2.2. DCOC

In a direct-conversion receiver, the main causes of DC offsets are layout mismatch and self-mixing of the leakage LO signal. After the mixer stage, the gain provided in each of the I and Q paths is in the 60-dB range, and then any differential offset at the mixer output or at one point of the baseband chain may get enough amplification to cause clipping within the signal path, or at the output of the receiver[7]. Therefore, the offset cancellation is necessary for the direct-conversion receiver, and it is implemented as a high-pass filter by using two feedback loops over the whole baseband path.

As is shown in Fig. 2, the transfer function of each closed loop is expressed as

$$H(S) = \frac{A}{1 + A\dfrac{\beta_0}{1 + s/w_0}} = \frac{A(s + w_0)}{s + (1 + A\beta_0)w_0}, \quad (1)$$

where A represents the gain of baseband VGA, and β_0 and w_0 denote the low-frequency gain and the 3-dB bandwidth of the DCOC circuit, respectively. Therefore, the high-pass cutoff frequency of the closed loop can be calculated as

$$f_c = f_0(1 + A\beta_0). \quad (2)$$

The f_0, β_0 and A should be carefully designed to assure that the cutoff frequency is neither too low which will delay the startup time or too high which will reduce the signal bandwidth[8].

The detailed DCOC circuit is shown in Fig. 5. The differential DC output voltage of each loop is sensed with an active

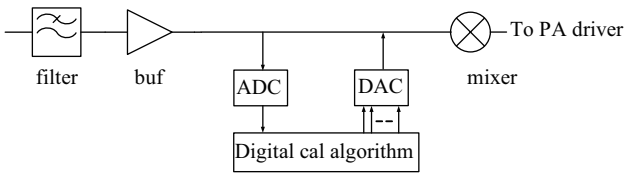


Fig. 6. Transmitter carrier leakage calibration loop.

RC filter whose cutoff frequency f_0 is decided by R, C and β_0. By using a pair of resistors that converts the output voltage to a current, a correction is injected at the input of the gain stage that compensates for DC offsets.

A common problem with the introduction of DCOC is that the high-pass cutoff frequency of the closed loop will vary with gain[7], as is shown in Eq. (2). To overcome this, the R of Fig. 5 is designed to vary with gain so that the cutoff frequency will not be varying when gain changes. The low-pass cutoff frequency of the active RC filter is calculated as

$$f_0 = \frac{1}{2\pi RC\beta_0}. \tag{3}$$

Then Equation (2) can be expressed as follows:

$$f_c = f_0(1 + A\beta_0) = \frac{1 + A\beta_0}{2\pi RC\beta_0} \approx \frac{A\beta_0}{2\pi RC\beta_0} = \frac{A}{2\pi RC}. \tag{4}$$

Therefore, when R varies with gain changing (A), the cutoff frequency f_c will maintain the same value.

To enable fast initial acquisition of DC offset, a higher-frequency pole can be programmed during a training phase, while during normal reception the pole can be programmed to a lower frequency to avoid corrupting the data[8]. Therefore, this high-pass corner is set to 1 MHz during preamble and switched back to 30 kHz when receiving data. This is also implemented by varying R of Fig. 5.

3. Transmitter carrier leakage calibration

In the direct-upconversion (DUC) architecture, a severe drawback is carrier leakage, which will peak out of the signal band and cause EVM to exceed the specification[9]. Therefore, suppressing carrier leakage is required in the DUC architecture to meet WLAN specification. This is implemented by reducing all DC offsets, which are upconverted to the carrier. The main contributors are the offset from the baseband filter and the offset from the mixer. The latter is mainly caused from the layout mismatch of the mixer, which can be improved by using large device sizes and good layout techniques. However, this may not be sufficient to meet the specification in terms of carrier leakage because the offset from the baseband filter can not be simply removed by well-matched layout such as the offset from the DACs. Therefore, carrier leakage calibration is necessary for the direct-conversion transmitter to meet specification.

3.1. Principle of calibration

Figure 6 shows the transmitter carrier leakage calibration loop. An on-chip 1 bit ADC samples the DC offset from the baseband filter, converts it to digital word and sends the word to the digital calibration algorithm. Then the algorithm sends a proper digital word to a 7 bit DAC in order to compensate the DC offset.

As we illustrated above, the offset caused from the layout mismatch of the mixer can be reduced by well-matched layout, so we can achieve the minimum carrier power if the DC offset from the baseband filter can be reduced to a minimum by the digital calibration algorithm. Therefore, the goal of the calibration algorithm is to generate a proper digital word which compensates the DC offset from the baseband filter to a minimum.

An advantage of the calibration is that the proposed ADC is only 1 bit which can save die size heavily, and the consequence is that the algorithm must try all digital words (2^7) and select the most proper one. This is called exhaustive search, which is a rather time-consuming and resource-wasting way. However, this worry can be neglected since calibration is only used during startup when no signal is transmitted.

Firstly, before calibration starting, the digital calibration algorithm determines the polarity of DC offsets according to the digital word of ADC. Secondly, exhaustive search is performed to find the proper control code for DAC to create a compensated DC offset, and the digital code for DAC is changed from 0000000 to 1111111 increasing 1 each time until the ADC changes its output polarity. Finally, when finding the proper digital word, the calibration algorithm turns off the ADC and stores the optimized digital word. Then during normal working phase only the DAC works with the stored optimized digital word. Therefore, the time consumption is negligible, and the ADC current consumption can also be neglected. Besides, offset cancellation technique based on output offset storage is also used to reduce the offset within ADC.

Another advantage is that the calibration does not introduce any high-pass pole compared with receiver DC offset cancellation, so the calibration only removes the carrier leakage, leaving the signal untouched.

3.2. DAC

The proposed DAC uses R-2R binary-weighted current sinks and the detailed schematic is shown in Fig. 7(b). The output current of DAC is injected into one of the differential bias branches of the buffer in order to compensate the DC offset, as is shown in Fig. 7(a). Whether the current is added to the left or the right bias branch lies on the command of the calibration algorithm.

The resolution and the bits of DAC should be carefully designed so that the calibration can not only cover the expected range of carrier power but also achieve a high resolution result. Therefore, 7 bit DAC is employed to this design and the I_{ref} current is programmable in order to meet the resolution and the range specification at different carrier leakage power.

4. Simulation and measurement results

The circuit is designed and fabricated in a 0.35 μm SiGe technology. Figure 8 gives a die photograph of the receiver baseband VGA and DCOC, and Figure 9 shows a die photograph of the transmitter carrier leakage calibration. They occupy 0.68 mm^2 die size and 0.18 mm^2 die size respectively.

In our system, it is required that any gain change in the receiver needs to settle very quickly. Figure 10 gives the mea-

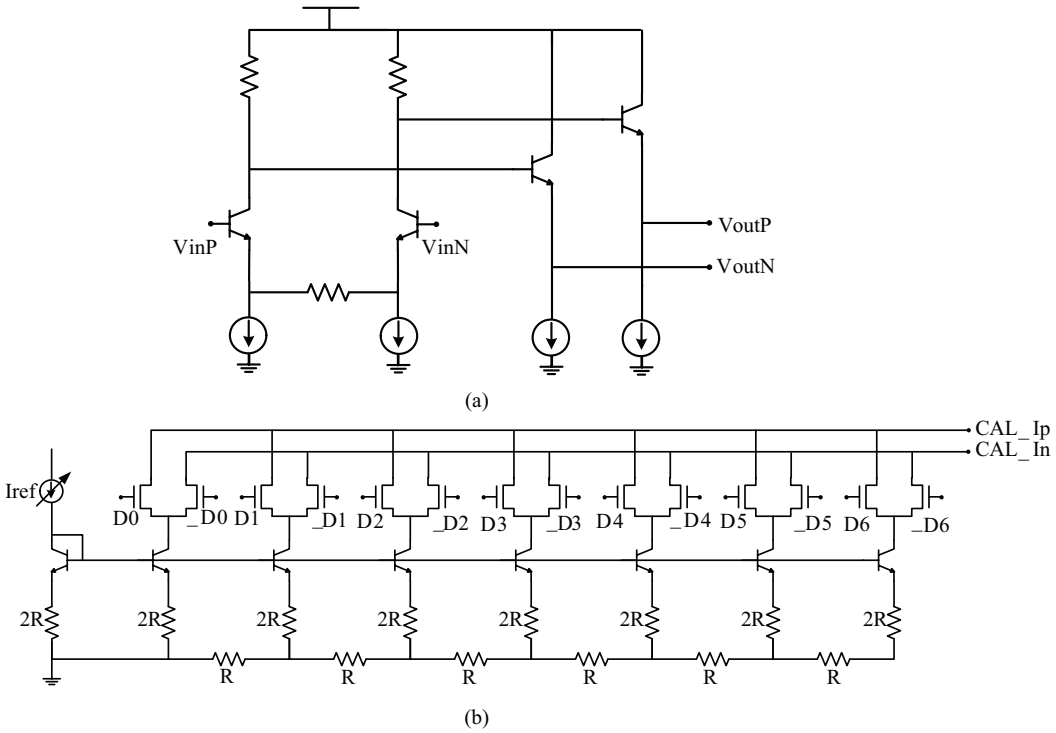


Fig. 7. (a) Calibrated buffer. (b) Schematic of 7 bit DAC.

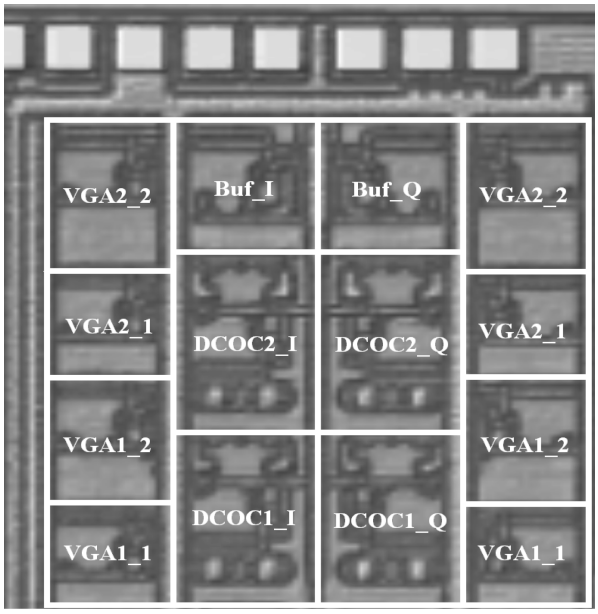


Fig. 8. Die photograph of the receiver baseband VGA and DCOC.

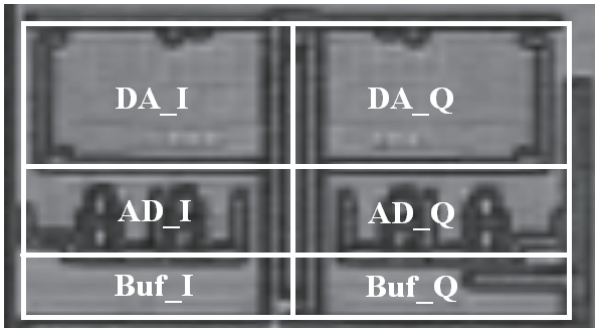


Fig. 9. Die photograph of the transmitter carrier leakage calibration.

surement result of RX DCOC settling response when BBVGA gain changes. Figure 10(a) shows the settling time for +32 dB gain step, and Figure 10(b) shows the settling time for –32 dB gain step. The time consumptions are 518 ns and 99 ns respectively, which are both at 1 MHz high-pass cutoff frequency during a training phase.

In order to assure the carrier leakage suppression even when the auto-calibration does not work, we design the 7 bit DA so that it can be tuned manually. Figure 11 gives the measured 7 bit DA manual calibration characteristic. With the 8 bit calibration setting word applying in Q-channel, carrier leakage is suppressed down from –29.8 to –66.9 dBm.

The measured transmitter performance with calibration is shown in Fig. 12. In Fig. 12(a) before calibration is applied, the power ratio between the wanted signal and the unwanted carrier leakage is –18.26 dBm. In Fig. 12(b) after calibration is applied, whereas the other signals remain unchanged compared to Fig. 12(a), the ratio is suppressed down to –37.23 dBm. We can see that the performance of manual calibration is better than auto-calibration from Figs. 11 and 12. This is because manual calibration can both reduce the offset from the baseband filter and the offset from mixer, but auto-calibration can only cancel the offset from the baseband filter; besides, the proposed ADC is only 1 bit and it will be disturbed by random noise. Therefore, the auto-calibration algorithm should make the ADC sample multiple times and take the average value in order to minimize the noise impaction by which the reliability of the algorithm can be improved dramatically.

The output spectrum of the transmitter with calibration is

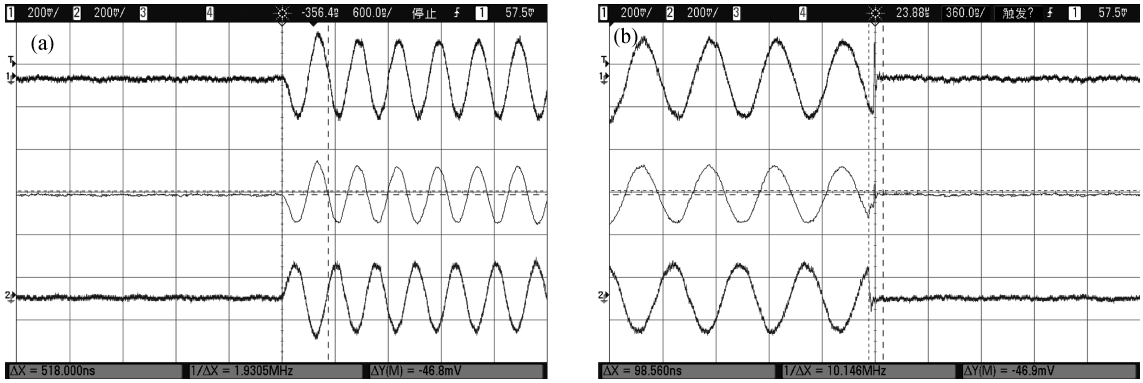


Fig. 10. Measurement result of RX DCOC settling response. (a) +32 dB BBVGA gain step. (b) –32 dB BBVGA gain step.

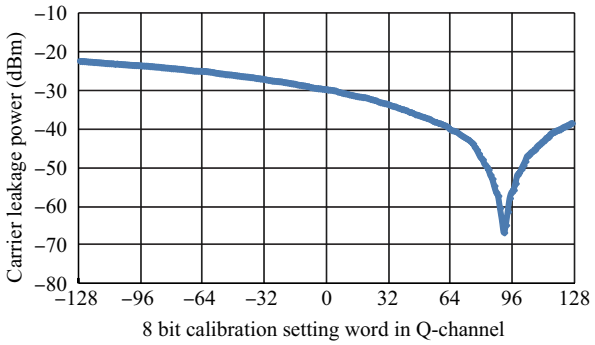


Fig. 11. Measured 7 bit DA manual calibration characteristic.

Table 1. Summary of WLAN baseband performance.

Parameter	Measured value
RX VGA gain range	62 dB
Gain step	2 dB
RX DCOC high-pass cutoff frequency	1 MHz @ high frequency 30 kHz @ low frequency
TX carrier leakage suppression	–37 dBc @ manual-cal –19 dBc @ auto-cal
RX baseband current consumption	13.12 mA @ BBVGA 4.4 mA @ DCOC
TX calibration current consumption	8.3 mA @ cal phase 5.88 mA @ normal phase
Supply voltage	2.85 V
RX and TX area	0.68 mm^2 @ RX 0.18 mm^2 @ TX

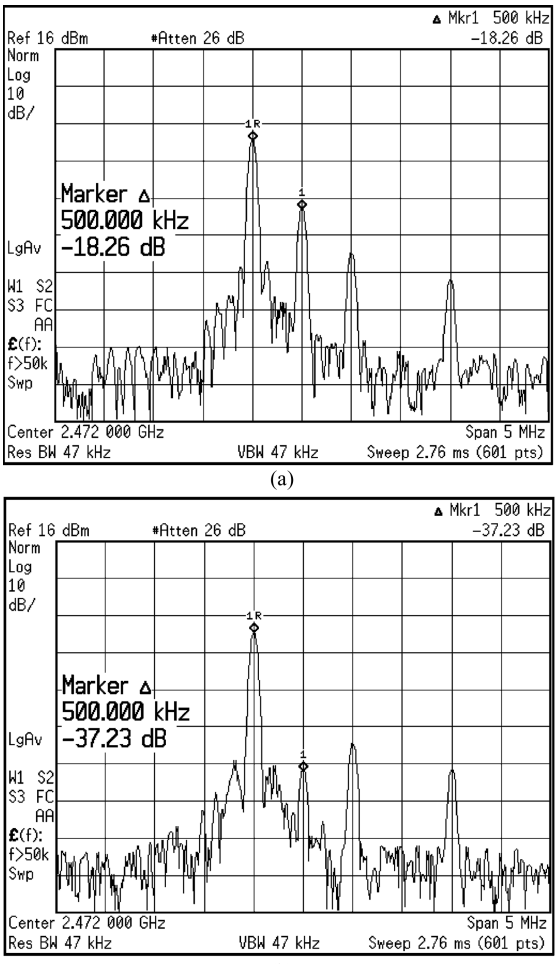
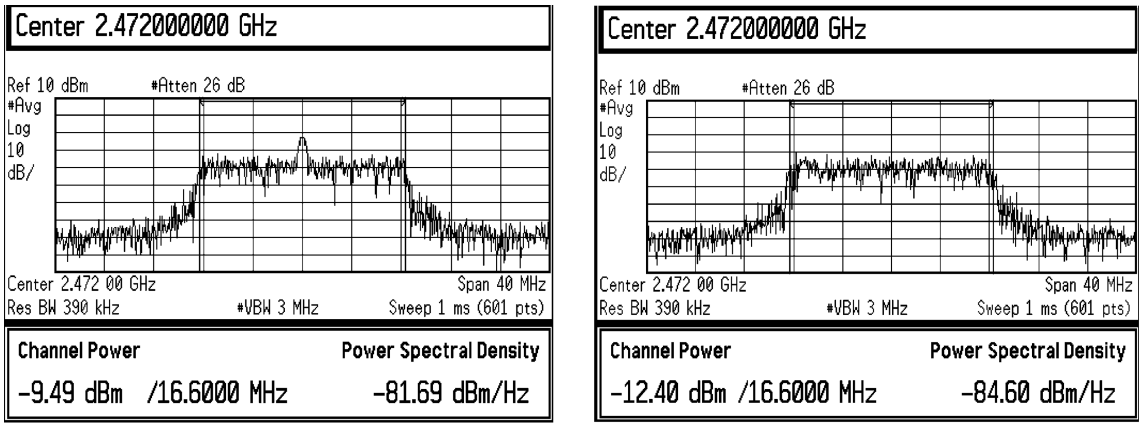


Fig. 12. Measured transmitter performance with calibration. (a) Before calibration. (b) After calibration.

shown in Fig. 13. Figure 13(a) shows before the calibration, the carrier leakage peaks out of the signal band and will cause EVM to exceed the specification. Figure 13(b) shows after the calibration, the carrier leakage is reduced below the signal band. Table 1 summarizes the WLAN baseband performance.

5. Conclusion

This paper presents a dual-band direct-conversion WLAN transceiver baseband for IEEE 802.11a/b/g. It was realized in 0.35 μm SiGe BiCMOS technology with 0.68 mm^2 die size for RX baseband VGA and DCOC while 0.18 mm^2 die size for TX carrier leakage calibration. The RX baseband achieves 60 dB gain range in 2-dB steps. In addition, some unique solutions in receiver DC offset cancellation and transmitter carrier leakage reduction are introduced to achieve excellent performance. The RX baseband consumes 17.52 mA (13.12 mA for BBVGA and 4.4 mA for DCOC), and the TX baseband consumes 8.3 mA (5.88 mA after calibration) under 2.85 V supply.



(a) (b)

Fig. 13. Output spectrum of transmitter with calibration. (a) Before calibration. (b) After calibration.

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