Performance optimization of MOS-like carbon nanotube-FETs with realistic source/drain contacts based on electrostatic doping*

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Abstract: Due to carrier band-to-band-tunneling (BTBT) through channel-source/drain contacts, conventional MOS-like Carbon Nanotube Field Effect Transistors (C-CNFETs) suffer from ambipolar conductance, which deteriorates the device performance greatly. In order to reduce such ambipolar behavior, a novel device structure based on electrostatic doping is proposed and all kinds of source/drain contacting conditions are considered in this paper. The non-equilibrium Green's function (NEGF) formalism based simulation results show that, with proper choice of tuning voltage, such electrostatic doping strategy can not only reduce the ambipolar conductance but also improve the sub-threshold performance, even with source/drain contacts being of Schottky type. And these are both quite desirable in circuit design to reduce the system power and improve the frequency as well. Further study reveals that the performance of the proposed design depends strongly on the choice of tuning voltage value, which should be paid much attention to obtain a proper trade-off between power and speed in application.

Key words: sub-threshold slope; ambipolar conductance; electrostatic doping; BTBT; Schottky contact; CNFET
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1. Introduction

In recent years, much attention has been directed to CNFETs as building blocks of nano-electronic systems. Such interest is justified by the promise of intrinsic performance comparable to silicon-based MOSFET technology[1] and better scaling perspectives[2]. According to source/drain leads material, the contact between the source/drain leads and the CNT channel can be of Ohmic[3] or Schottky type[4], corresponding to C-CNFETs and Schottky barrier carbon nanotube-FETs (SB-CNFETs). In order to overcome the physical limitation of sub-threshold slope limitation[5] in SB-CNFETs and C-CNFETs, band-to-band tunneling has been made use of to obtain a sub-threshold slope below this limitation in tunneling carbon nanotube-FETs (T-CNFETs).

Generally speaking, the Schottky barrier in SB-CNFETs contributes to the ambipolar behavior and limits the performance of these devices[4,6]. Therefore, much research work has been done and much progress has been made to reduce the ambipolar conductance in SB-CNFETs recently[7–9]. Certain attention has also been paid to the optimization of conducting characteristic of T-CNFETs[10]. As for C-CNFETs, the band-to-band-tunneling, although it could be made use of to obtain an inverse sub-threshold slope smaller than the physical limitation for conventional thermal emission device[11], would lead to deteriorated OFF-state performance, flattened sub-threshold transfer characteristic and even ambipolar conductance[12]. A linear doping strategy was proposed by Hassaninia *et al.* in Ref. [13] to reduce the ambipolar conductance of C-CNFETs. But the simulation results showed that the obtained performance improvement, even at severe cost to the device area, was quite limited. At the same time, the present technology is not yet at this stage to obtain such a linear doping profile. A dual-gate-material based device structure has been proposed in our earlier work[14]. Such a device structure could contribute to a great decrease in OFF-state current as well as obvious reduction of ambipolar conductance, but bring great challenge to the fabrication technology.

On the other hand, it is just a general method to divide CNFETs into SB-CNFETs and C-CNFETs. In fact, C-CNFETs are unavoidably to be connected to metal electrodes in application.

In order to obtain C-CNFETs with reduced ambipolar conductance and greater feasibility for fabrication, an electrostatic doping based device design is proposed with all kinds of contacting conditions considered in this paper. And the simulation results show that this device design can not only reduce the ambipolar conductance but also decrease the sub-threshold slope of C-CNFETs.

2. Electrostatic doping strategy

A two-dimensional schematic view of the device structure with ohmic contact is shown by Fig. 1(a). Coaxial geometry, realizable in realistic application[15], is adopted for simplicity.

In Fig. 1(a), the light gray part represents the carbon nanotube. As shown by the "N" labeled rectangles, both sides of the CNT are highly doped by controlling the electrostatics of the nanotube environment by molecules[16] or metal ions[17], and serve as source/drain leads, respectively. The middle part of the CNT is left intrinsic and serves as the conducting channel, as the "i" labeled rectangle shows. Three metal electrodes are deposited outside the intrinsic CNT just as the "G1", "G2" and "G3" labeled rectangles show, where "G2" serves as a gate electrode and is applied with gate voltage V_g, while "G1" and

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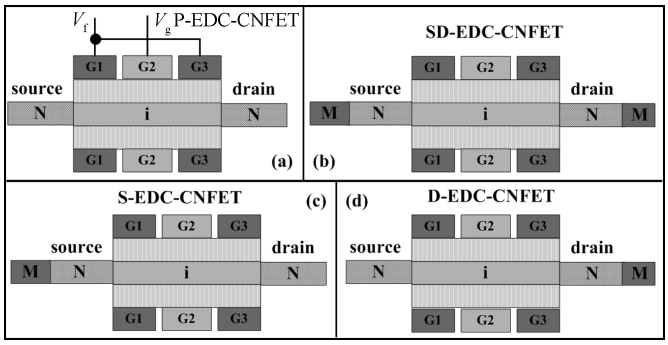


Fig. 1. Two-dimensional sketches of electrostatic doping based C-CNFET structures with all kinds of contacting conditions.

"G3" serve as tuning electrodes and are applied with tuning voltage V_f.

The metal electrodes and intrinsic CNT, which share the same material work function, are separated by an oxide with a thickness of 2 nm. It should be noted that what Fig. 1(a) shows is just a schematic diagram of the electrostatic doping based device design. The tuning electrodes could be realized by adopting bury-gate [9], multi-gate[18] or even electrochemical doping[19] techniques in practice. And the spaces between G1 (G3) and G2 would disappear when the bury-gate technique is adopted to realize such electrostatic doing strategy.

For convenience of introduction, such electrostatic doping based CNFET structure is denoted "EDC-CNFETs", while the conventional C-CNFETs are denoted "C-CNFETs".

When the first CNFET was presented in 1998[20, 21], just one CNFET was assembled on an individual nanotube, where both source and drain leads of the device were connected directly to metal electrodes. Such a topological structure, called "assembling approach one" in this paper, dominated both theoretical and experimental researches in the following years. However, with the fast development of both carbon nanotube growth and CNFET assembling techniques, the method of assembling several devices on an individual nanotube, called "assembling approach two" in this paper, has become an acceptable approach to improve device performance as well as simplify circuit manufacture. For example, Reference [22] demonstrated one-, two-, and three-transistor circuits that exhibit a range of digital logic operations, such as an inverter, a logic NOR, a static random-access memory cell, and an ac ring oscillator. A five stage ring oscillator was assembled on an individual carbon nanotube by Chen *et al.* in Ref. [23]. In Ref. [24], two-bit carbon nanotube ferroelectric field-effect memories were assembled on an individual nanotube. The source/drain leads would either be connected directly to metal electrodes or share the same CNT parts with another CNFET in these cases.

Considering both these two assembling approaches, we can divide the contacting conditions of EDC-CNFETs into four categories, as Figure 1 shows. Figure 1(a) represents the situation where both source and drain leads of the considered EDC-CNFET are connected to another two EDC-CNFETs in assembling approach two, and the corresponding device structure is denoted by P-EDC-CNFET. Figure 1(b) represents the situation where both source and drain leads of the considered EDC-CNFET are connected to metal electrodes in assembling approach two or assembling approach one, and the corresponding device structure is denoted by SD-EDC-CNFET. Figure 1(c) (Figure 1(d)) represents the situation where the drain (source) lead of the considered EDC-CNFET is connected to another EDC-CNFET while the source (drain) lead contacts with a metal electrode in assembling approach two, and the corresponding device structure is denoted by S-EDC-CNFET (D-EDC-CNFET). For the convenience of comparison, the corresponding device structures with a uniform gate electrode are denoted by P-C-CNFET, SD-C-CNFET, S-C-CNFET and D-C-CNFET, respectively.

What should be noted is that the above mentioned metal electrode in assembling approach two could be a power supply electrode, an output electrode and so on.

3. Modeling method

Due to wave-particle dualism, charges in CNFETs are governed by both Schrödinger and Poisson equations. Quantum phenomena play an important role in device performance and couldnot be ignored any more[25, 26], especially in the nano region. In this paper, the NEGF method is used to develop the CNFETs model to take quantum phenomena, such as carrier tunneling and quantum capacitance, into account. The NEGF formalism, which solves the Schrödinger equation and the Poisson equation iteratively, describes the carriers transporting in CNFETs exactly[27, 28] and provides a sound basis for quantum device simulation. In this approach, the device is described by a Hamiltonian H_C using a simple π-orbital nearest neighbor tight-binding model without consideration of the exchange-correlation effect. For the convenience of calculation, self-energy matrixes Σ_S and Σ_D, which provide the appropriate quantum boundary conditions, are introduced to describe the effect of the source/drain leads.

The simulation procedure of NEGF can be summarized as follows:

Step 1: Specify the initial guess for the self-consistent potential ϕ of the device and the operating bias.

Step 2: Solve the Schrödinger equations to obtain the charge density matrix ρ. The specification of the green function $G = [(E + i0^+)I - H_C - \Sigma_S - \Sigma_D]^{-1}$ is included in this step.

Step 3: Feed ρ into Poisson's equation to obtain a new guess for the self-consistent potential ϕ.

Step 4: Iterate steps 2 and 3 until both ϕ and ρ converge to the required accuracy.

Step 5: Using the NEGF formalism and the converged ρ, the terminal currents and the electron density can be calculated.

In order to improve the calculating speed, the sparse matrix and the Jacobin algorithm are applied and the mode space is doped in this paper, and it is valid when the potential variation around the tube is much smaller than the spacing between the sub-bands. Due to quantum confinement along the tube circumference, the wave functions of the carriers are bound around the CNT and can only propagate along the tube axis. Therefore, the potential profile does not vary around the circumference of the CNT and the sub-bands can be decoupled[11]. According to both theoretical analysis and experimental results, it is valid for the mode space to consider the lowest two sub-bands as for CNFETs with (13, 0) carbon nanotube

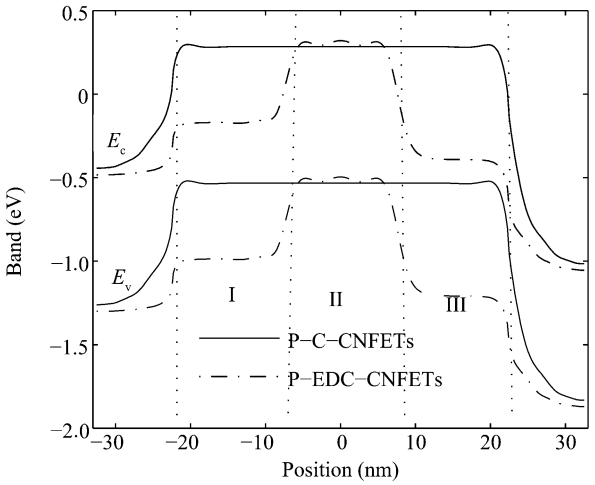


Fig. 2. Band profile of conventional P-C-CNFETs (solid lines) and P-EDC-CNFETs (dot-and-dash lines) with tuning voltage $V_f = 0.8$ V (as for P-EDC-CNFETs), source-drain voltage $V_d = 0.6$ V and gate voltage $V_g = 0$ V, where the E_c labeled black lines stand for the conductance bottom while the E_v labeled gray lines indicate the valence top.

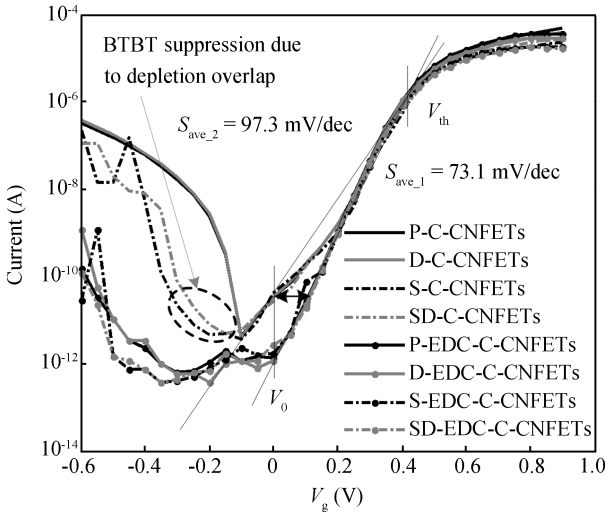


Fig. 3. Transfer characteristics of both C-CNFETs and EDC-CNFETs with all kinds of source/drain contacting circumstances, where $V_d = 0.6$ V, source/drain doping level $\rho = 15 \times 10^8$ m^{-1}, $L_{G1} = L_{G2} = L_{G3} = 15$ nm, source/drain leads length $L_{SD} = 15$ nm, $V_f = 0.8$ V, oxide thickness $t = 2$ nm, oxide dielectric $\varepsilon = 16$, carbon nanotube chirality of (13, 0), tight-binding parameter $V_{pp} = -3$ eV.

channel[10, 29, 30] under the assumed bias condition in this paper.

A detailed description of the modeling of CNFETs based on the NEGF method can be found in Ref. [31, 32].

4. Performance Analysis

Taking ohmic source/drain contact, for instance, at first.

Being different from that in SB-CNFETs, the drain current, mainly consisting of thermal emission current, is determined by the barrier height of the channel in C-CNFETs. When a large positive gate voltage is applied, the band profile in the channel is pushed down far enough to turn the device on. With the decrease in V_g, the band profile in the channel ascends and thus the drain current decreases accordingly. Without further energy broadening from the Schottky barrier, the sub-threshold slope of the P-C-CNFETs is much closer to the physical limitation of $S = \ln 10[(\partial I_d/\partial V_g)(1/I_d)]^{-1} = \ln 10\, k_B T/q \approx 60$ mV/dec, where q is the electron charge while k_B and T denote the Boltzmann constant and the temperature, respectively. Extracting the sub-threshold slope from the transfer characteristic, as shown in Fig. 3, one observes a sub-threshold slope of about 71.5 mV/dec when V_g is swept from 0.4 V to 0.2 V.

However, with the further decrease in V_g, the valence top of the channel would be pulled far up over the conductance bottom of the drain lead, as the solid lines in Fig. 2 show. An analytical solution of a one-dimensional Poisson equation for the potential at the channel-dielectric interface, which is denoted by Φ_f, could lead to an analytical expression of Φ_f in the form of $\Phi_f \propto \exp(-x/\lambda)$, showing that λ is the relevant length scale for potential variations. This screening length λ is a function of not only CNT diameter d_{CNT} but also oxide thickness d_{ox}. For the coaxial geometry considered here, it would be given by $\lambda = \sqrt{\varepsilon_{CNT} d_{CNT}^2 \ln[1 + (2d_{ox}/d_{CNT})]/8\varepsilon_{ox}}$[33], where ε_{CNT} and ε_{ox} are the relative dielectric constants of the nanotube and the gate oxide. As a result, the combination of small CNT diameter and oxide thickness in CNFETs allows one to obtain not only an abrupt change in the device current I_d as a function of the gate voltage[34], but also substantial carrier BTBT. A large number of holes transport from the drain lead into the channel via BTBT and then pile up in channel due to the existence of the energy barrier of the source lead. The continued rise in charge density would enlarge the quantum capacitance value in the channel and thus deteriorate the control of the gate on the conducting ability of the channel. Consequently, a larger sub-threshold slope is obtained when V_g is swept from 0.2 V to −0.18 V.

With the further decrease in V_g, the valence top of the channel would even be pulled up over the conductance bottom of the source lead. A tunneling passageway would be formed in this case and the resulting tunneling current would contribute to the sharp increase in I_d with a further decrease in V_g, as the left part of the black solid line in Fig. 3 shows.

For comparison, the band profile of P-EDC-CNFETs is shown as the dot-and-dash lines in Fig. 2. For the convenience of introduction, the band profile regions that corresponding to G1, G2 and G3 are denoted with I, II and III, respectively. The band profile bend in regions I and III, under the action of V_f, contributes to the effective elimination of the BTBT that exists in conventional C-CNFETs. As a result, the transfer characteristic curve extends further with the sub-threshold slope not affected, just as the dot marked lines in Fig. 3 show. With further decrease in V_g, carriers BTBT at the II–III and I–II interfaces would contribute to the non-monotonic behavior in the transfer characteristic of the device.

Comparing the dot marked black line to the black line in Fig. 3, we find that the performance of P-EDC-CNFETs overtakes that of P-C-CNFETs in terms of not only reduced ambipolar conductance but also better sub-threshold performance. It is clear that P-C-CNFETs and P-EDC-CNFETs share the same threshold voltage V_{th}, which is about 0.4 V in this case. When

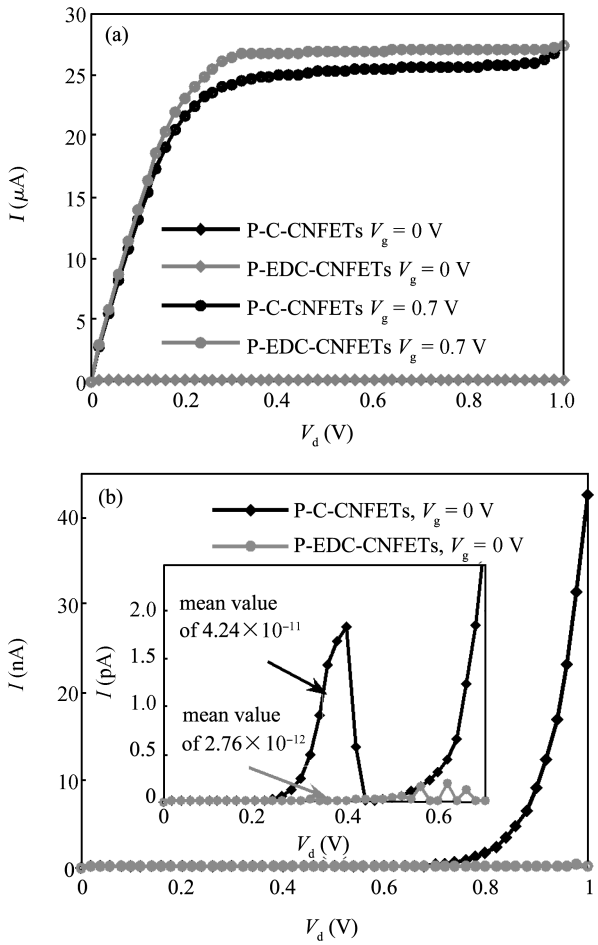


Fig. 4. Comparison between the output characteristics of P-C-CNFETs (black lines) and P-EDC-CNFETs (gray lines) that correspond to the (a) ON-state and (b) OFF-state.

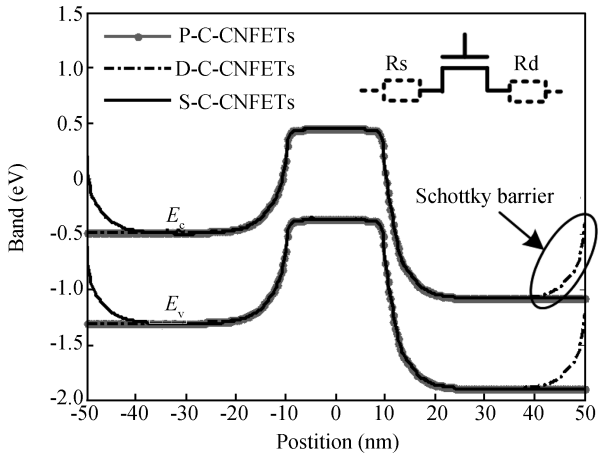


Fig. 5. The band profile of C-CNFETs with all kinds of source/drain contacting conditions with $V_d = 0.6$ V, $V_g = -0.3$ V, source/drain leads doping level of $\rho_2 = 15\times10^8$ m^{-1} and CNT chirality of (13, 0)

the initial voltage V_0 is set to 0 V, the average sub-threshold slope of P-EDC-CNFETs is about 73.1 mV/dec, about 25% smaller than that of P-C-CNFETs (about 97.3 mV/dec). The decreased average sub-threshold slope would mainly contribute to two advantages.

On the one hand, it would reduce the power of either static or dynamic power dominated applications. When the same initial gate voltage of 0 V is chosen, P-EDC-CNFETs are almost of the same ON-state but have better OFF-state performance than P-C-CNFETs, as Figure 4 shows. The output characteristics of P-C-CNFETs and P-EDC-CNFETs with $V_g = 0$ V and V_d varying between 0 V and 1 V are shown as the black lines and gray lines in Fig. 4(b). The average OFF-state current of P-C-CNFETs is about 4.24×10^{-11} A when V_d increases from 0 V to 0.7 V, as the black line in the inset of Fig. 4(b) shows. The average OFF-state current of P-EDC-CNFETs is just 2.7×10^{-12} A, about 93.6% smaller than that of P-C-CNFETs. With the further increase of V_d, the OFF-state current of P-C-CNFETs increases sharply while that of P-EDC-CNFETs remains much the same, which would contribute to greater static leakage power saving by adopting the electrostatic doping based design proposed in this paper.

When the same ON-OFF current ratio is chosen, as Figure 3 shows, the sub-threshold voltage of P-EDC-CNFETs is about 0.12 V smaller than that of P-C-CNFETs. Then the sub-threshold range and thus the required supply voltage V_{DD} of P-EDC-CNFETs is about 30% smaller than that of P-C-CNFETs. It is known that the expression for the dynamic power is $P_{dyn} = C_L V_{DD}^2 f_{0\to1}$, where C_L and $f_{0\to1}$ stand for the intrinsic output capacitance and the switching frequency of the considered gate, respectively. As a result the smaller V_{DD} would contribute to a much greater, 51% in this case, dynamic power saving.

On the other hand, the decreased average sub-threshold slope would result in a smaller supply voltage V_{DD}, as introduced above. Considering the expression of gate delay $\tau = C_g V_{DD}/I_d$, the decreased V_{DD} would result in a faster switching speed, which in turn would contribute to a smaller dynamic power.

As introduced above, C-CNFETs are unavoidable to contact with metal electrodes in realistic circuits, even with several CNFETs assembled on an individual CNT. The Schottky barrier exists at the source/drain-CNT interface due to the work function difference between the CNT and the source/drain leads contact material. The Schottky barriers, with the height depending largely on the choice of source/drain lead contact material, would have a negative impact on the carrier transport, including not only the carriers' thermal emission but also their band-to-band tunneling. The effect of the Schottky contact could be equaled to be effective resistance that connected to the device in series, just as the two dashed rectangles (R_S and R_D) in Fig. 5 show. The value of the effective resistances are dependent on not only the bias condition but also the device parameters, such as the source/drain contacting material, the chirality of the CNT and the doping level of the source/drain leads.

The transfer characteristics of both C-CNFETs and EDC-CNFETs with all kinds of contacting conditions are modeled as Figure 3 shows, when the parameters listed in the caption of Fig. 3 are adopted. Comparing all kinds of transfer characteristic curves in Fig. 3, we find that (1) the proposed electrostatic doping based CNFET structure would contribute to an improved device performance even with Schottky contacts considered; (2) the effects of the Schottky contacts on the device performance of EDC-CNFETs are relatively small and even negligible with the proper choice of source/drain contact-

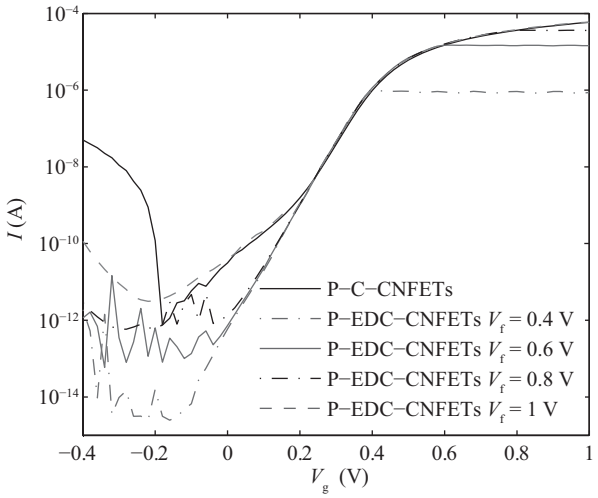
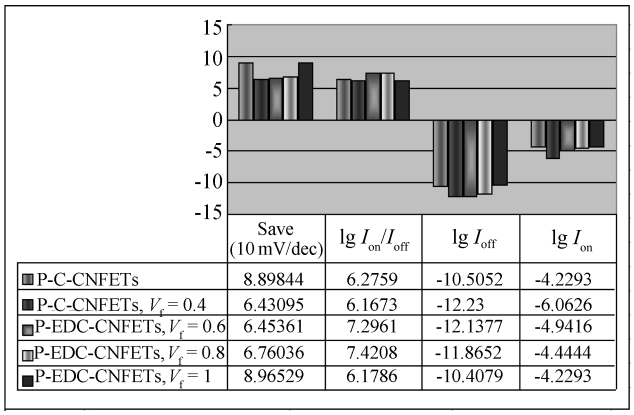


Fig. 6. Transfer characteristics of P-EDC-CNFETs with different V_f values.



	Save (10 mV/dec)	lg I_{on}/I_{off}	lg I_{off}	lg I_{on}
P-C-CNFETs	8.89844	6.2759	-10.5052	-4.2293
P-C-CNFETs, V_f = 0.4	6.43095	6.1673	-12.23	-6.0626
P-EDC-CNFETs, V_f = 0.6	6.45361	7.2961	-12.1377	-4.9416
P-EDC-CNFETs, V_f = 0.8	6.76036	7.4208	-11.8652	-4.4444
P-EDC-CNFETs, V_f = 1	8.96529	6.1786	-10.4079	-4.2293

Fig. 7. Dependence of performance criteria on V_f values.

ing material; (3) the device performance of C-CNFETs depends more highly than that of EDC-CNFETs on device scale. For example, when the feature size is chosen to be 15 nm, the depletion at the metal-source/drain interface would overlap with that at the source-channel interface, and this would contribute to the ascension of the source/drain band profile and thus the postponement of carrier band-to-band tunneling, as the dash-dotted ellipse in Fig. 3 shows. However, EDC-CNFETs would not suffer from such a phenomenon.

What should be pointed out is that device parameters, such as the source/drain contacting material, the coupling degree between the source/drain leads and the contacting material, would have certain impacts on the performance of EDC-CNFETs. So much attention should be paid to them in application.

5. Choice of V_f

It is apparent that the suppression of BTBT leads to a reduction in ambipolar conductance. So it is safe for us to conclude that the performance of EDC-CNFETs depends highly on the value of V_f. In order to confirm such conclusion, the transfer characteristics of P-EDC-CNFETs with the same V_g but different V_f values are modeled in Fig. 6.

If the value of V_f is relatively big, 1 eV for instance, the band profile in regions I and III lies low enough that the valence top of region II would be pulled up over the conductance bottom of regions I and III under the action of a small enough gate voltage. And this would contribute to the carrier pile-up in the channel and thus the deterioration of sub-threshold performance and increase in ambipolar conductance.

If the value of V_f is relatively small, 0.4 eV for instance, only a slight band bend takes place in regions I and III. The band profile of region II is pushed down below those of regions I and III when $V_g > 0.4$ V. Right now, the barrier height that electrons in the source/drain leads face is determined by the band profile of regions I and III, which is independent of the change in V_g. The resulting I_d saturation, shown as the gray dot-and-dash line in Fig. 6, would lead to the deterioration of the ON-state performance in terms of a weakened current driving ability and thus a larger gate delay.

For a deeper insight into the impact of the V_f value, a series of device performance criteria have been defined as follows:

S_{ave}: Average sub-threshold slope over the whole sub-threshold region with $V_0 = 0$ V, reflecting not only the switching speed but also the potential for low-power application.

lg(I_{on}): Logarithm of drain current corresponding to the ON-state, i.e. I_d with $V_g = 1$ V, reflecting the current driving ability and thus the switching delay of the device.

lg(I_{off}): Logarithm of drain current corresponding to the OFF-state, i.e. I_d with $V_g = 0$ V, reflecting the value of the static leakage power.

lg(I_{on}/I_{off}): Logarithm of ON–OFF current ratio.

The dependence of the above performance criteria on the V_f value are extracted from Fig. 6 and shown in Fig. 7. It is safe for us to conclude that (1)the electrostatic doping strategy can improve the device performance as a whole; (2) the electrostatic doping strategy would deteriorate the ON-state performance if a bad V_f value is chosen; (3) the proper value of V_f depends largely on the bias condition, the source/drain doping level, the CNT chirality and so on. Much attention should be paid to the choice of V_f value to obtain a sound trade-off with working frequency, dynamic power and static power. A V_f value of 0.8 V is a good choice here.

6. Conclusion

With the advancement of technology increasing, the ultimately scaled CNFETs would suffer from severe OFF-state performance: both theoretical and experimental results reveal that the scaled device shows an increasing leakage current as well as a substantially larger inverse sub-threshold slope. As for C-CNFETs, the BTBT taking place at the source/drain-channel contact would contribute to carrier pile-up in the channel and deterioration of device performance. In order to reduce the ambipolar conductance of the C-CNFETs, an electrostatic doping based device structure is proposed in this paper. Such a device structure with all kinds of source/drain contacting circumferences is modeled. The NEGF based simulation results reveal that such an electrostatic doping strategy could not only reduce the ambipolar conductance but also improve the sub-threshold performance effectively, which are both very desirable in device design. However, the device performance im-

provement depends strongly on the choice of V_f value, and much attention should be paid to this to obtain a sound trade-off between working frequency, dynamic power and static power.

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