Above 700 V superjunction MOSFETs fabricated by deep trench etching and epitaxial growth

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Abstract: Silicon superjunction power MOSFETs were fabricated with deep trench etching and epitaxial growth, based on the process platform of the Shanghai Hua Hong NEC Electronics Company Limited. The breakdown voltages of the fabricated superjunction MOSFETs are above 700 V and agree with the simulation. The dynamic characteristics, especially reverse diode characteristics, are equivalent or even superior to foreign counterparts.

Key words: superjunction; deep trench etching; epitaxial growth; power MOSFET

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1. Introduction

There exists a trade-off relationship between specific on-state resistance (R_{on}) and breakdown voltage (BV) for conventional power MOSFETs ($R_{\mathrm{on}} \propto \mathrm{BV}^{2.5}$)[1], which limits the application of power MOSFETs in many fields. In the 1990s, a new structure called a composite buffer layer or superjunction (SJ) was proposed to overcome the theoretical silicon limit[2−9]. The specific R_{on} of the SJ structure is approximately linear with BV; therefore SJ power devices have attracted tremendous attention from researchers. CoolMOS™, an SJ-MOSFET, was introduced to the market by the Infineon Company in 1998[10]. Compared to a traditional vertical double diffused MOSFET (VDMOSFET) with the same chip area, CoolMOS™ offers extremely low static and dynamic losses. Several methods of fabricating SJ structures have been investigated in the last decade[11, 12]. However, domestic research on superjunction fabrication has rarely been reported, because the breakdown voltage of the SJ devices is very sensitive to the charge mismatch, which makes the device manufacture a very challenging task. In this paper, we report a silicon SJ power MOSFET with a breakdown voltage above 700 V. The device was achieved by deep trench etching and epitaxial growth, based on the process platform of the Shanghai Hua Hong NEC Electronics Company Limited.

2. Basic structure

Figure 1 shows the basic structure of an SJ power MOSFET. The drain, gate and source of the device are represented by D, G and S, respectively.

The SJ-MOSFET is based on the MOSFET principle, but the N-drift region of the standard power MOSFET is replaced by alternatively stacked, heavily doped P- and N-type semiconductor pillars. This means that the electric field is built up not only in the vertical direction as in standard power MOSFETs, but also in the horizontal direction. Therefore, the SJ-MOSFET allows the breakdown voltage to be dependent just on the drift region thickness and independent of the drift region doping concentration if both P and N pillars are completely depleted before the breakdown. In this situation, the breakdown voltage is independent of the drift region doping, and the SJ-MOSFET has 5–100 times lower specific on-resistance than conventional high voltage MOSFETs. The on-state resistance is not proportional to the breakdown voltage raised to the power of 2.5 as in the traditional MOSFET, but is approximately linear with the breakdown voltage. Different power law relationships between the avalanche breakdown voltage and the specific on-resistance for SJ-MOSFETs have been obtained by several authors[5, 13−15].

3. Simulation

Appropriate control of the N- and P-pillars' charges improves the performance and robustness of the SJ-MOSFET. Therefore the shapes and doping concentrations of the pillars are the most important design parameters. For this purpose,

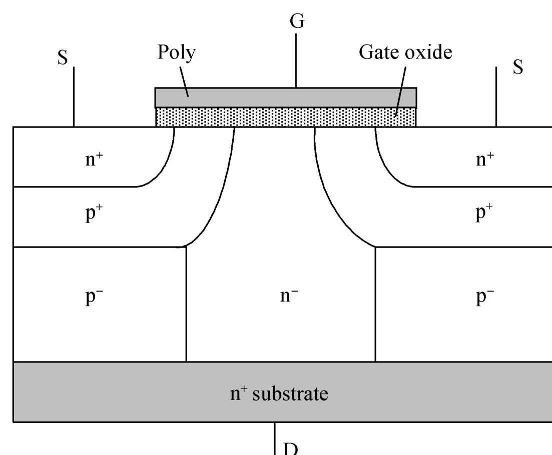

Fig. 1. Basic structure of an SJ power MOSFET.

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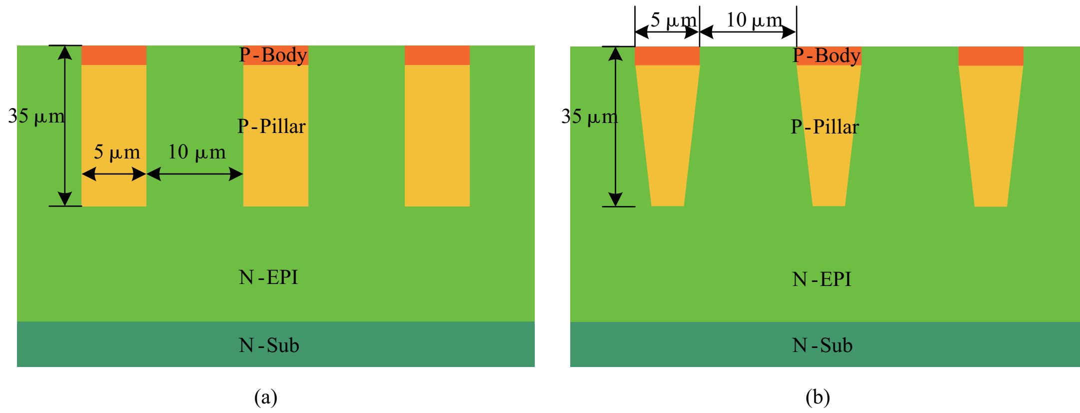


Fig. 2. Schematic diagrams of (a) rectangular trench and (b) trapeziform trench.

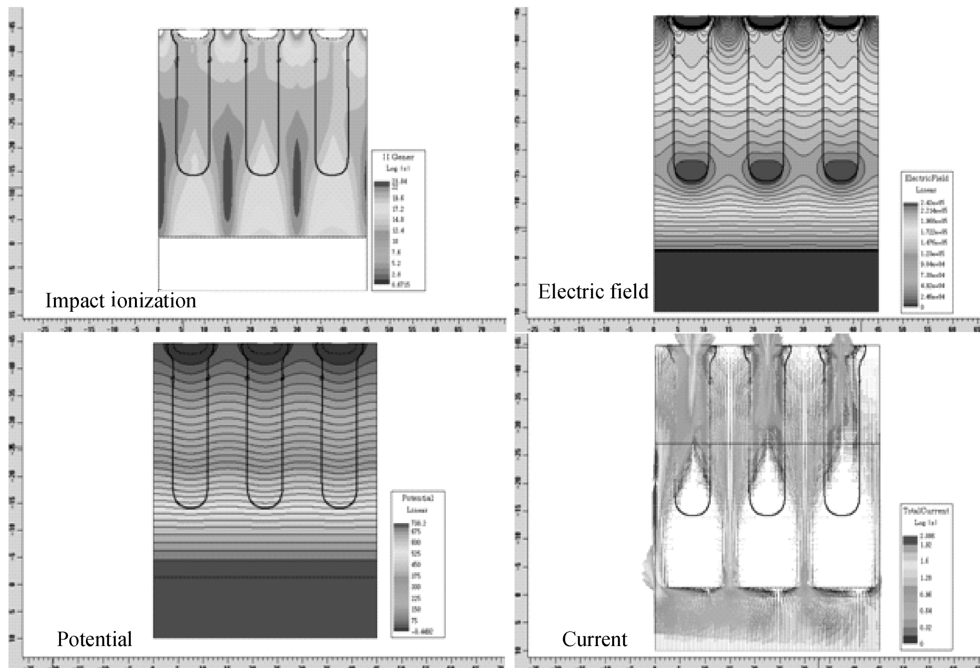


Fig. 3. Simulation of an SJ-MOSFET with rectangular trenches.

two types of trench structures, rectangular and trapeziform, were simulated by the 2-D simulator, Medici[16, 17]. Figures 2(a) and 2(b) show schematic diagrams of the two structures, where P-pillar, N-EPI and P-body correspond to P^-, N^- and P^+ in Fig. 1, respectively. The widths, depths and interspaces of the P-pillars are 5 μm, 35 μm and 10 μm, respectively. The SJ-MOSFET was fabricated on N-type silicon substrate. The epitaxial layer parameters, including resistivity and thickness, are mainly determined by the breakdown voltage; on the other hand, the effects of these parameters on the on-state resistance must be taken into account. By theoretical analysis and simulation, we choose a phosphorus-doped epitaxial layer of $\rho = 7.5\ \Omega\cdot$cm and 45 μm in thickness. The boron impurity concentration in the P-pillar was 2.0×10^{15} cm^{-3}. The boron ion implantation energy and dose in the P-body were 120 keV and 6.0×10^{13} cm^{-3}, respectively.

Figure 3 shows a simulation of an SJ-MOSFET with rectangular trenches. The breakdown voltage is about 738 V. Figure 4 shows a simulation of an SJ-MOSFET with trapeziform trenches. The breakdown voltage is about 665.9 V. As we all know, the breakdown voltage in the charge balance condition ($Q_p = Q_n$; Q_p and Q_n are the p- and n-pillar charges, respectively) is much higher than that in the charge imbalance condition ($Q_p \neq Q_n$)[13]. It is easier to obtain charge balance in the rectangular trench since its charge distribution is more uniform under our process conditions. The simulation shows that the rectangular trench has relatively flat equi-potential lines and thus a more uniform electric field distribution compared to the trapeziform one. Therefore, the rectangular trench was chosen in our experiments.

4. Experimental results and discussion

To fabricate an SJ-MOSFET, trench-filling SJ technology to achieve P-pillars has been developed. At first, dioxide is patterned for the hard masks against dry etching. Next, trenches are formed by deep trench etching. Then the trenches are filled with boron-doped epitaxial monocrystalline silicon layers. In

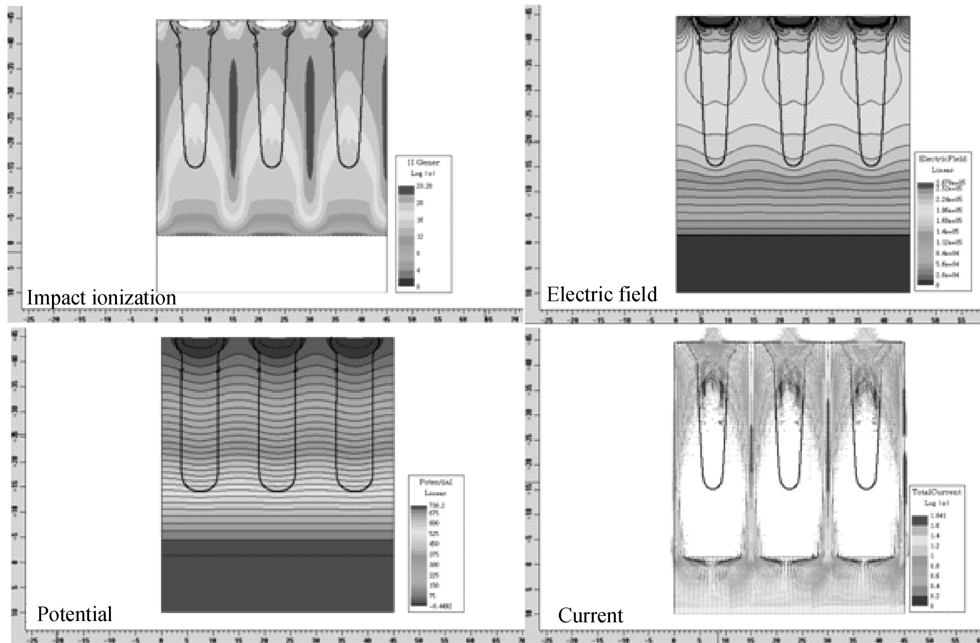
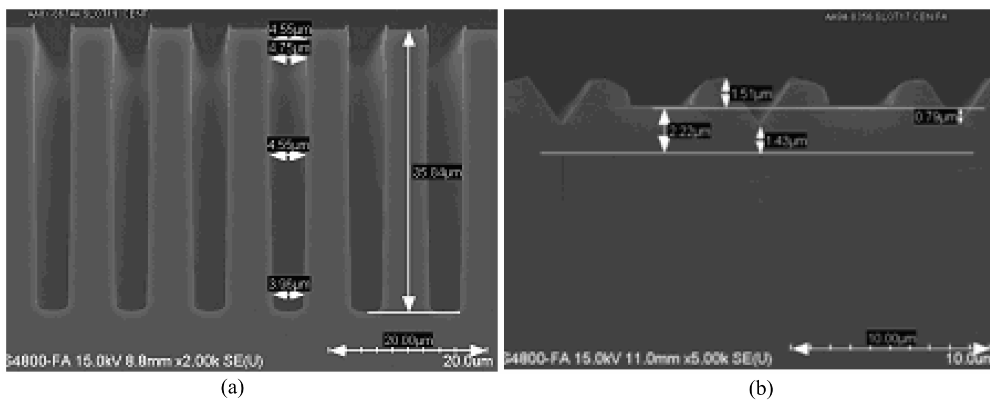
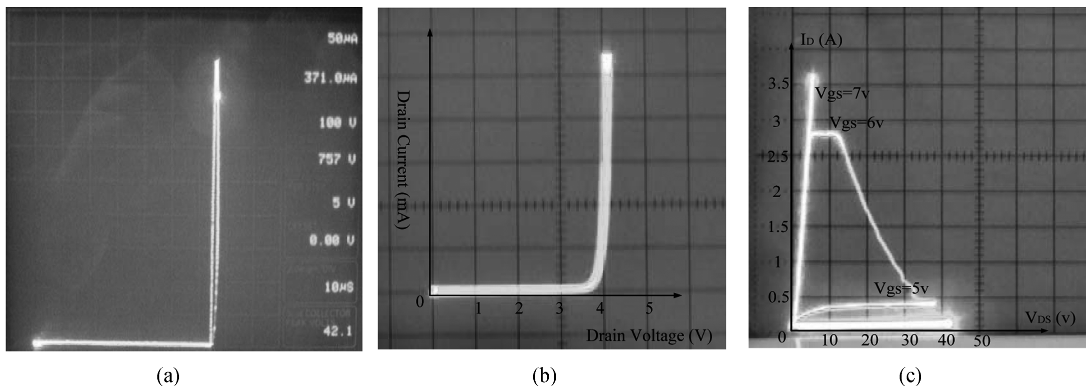


Fig. 4. Simulation of an SJ-MOSFET with trapeziform trenches.



(a) (b)

Fig. 5. Scanning electron microscopy (SEM) images of the cross-sections. (a) Deep trench etching. (b) Epitaxial growth.



(a) (b) (c)

Fig. 6. Measured I–V curve of the fabricated SJ-MOSFET. (a) Breakdown voltage. (b) Threshold voltage. (c) Output characteristics.

order to obtain rectangular trenches, the process conditions and flows should be controlled carefully and precisely. Figure 5 illustrates the cross-sections of the rectangular trenches and P-pillars. The trenches have very abrupt sidewalls, and neither microscopic defects nor voids have been observed after epitaxial growth. P-body and N^+ source were fabricated by ion implantation and drive-in diffusion, just as in a conventional VDMOSFET.

Table 1. Dynamic characteristics.

	Parameter	This work	IPx60R380C6[18]	Unit
C_{iss}	Input capacitance	1029.2	700	pF
C_{rss}	Reverse transfer capacitance	4.2	—	pF
C_{oss}	Output capacitance	72.8	46	pF
$T_{d(on)}$	Turn-on delay time	15.2	15	ns
T_{rise}	Rise time	23.1	10	ns
$T_{d(off)}$	Turn-off delay time	28.4	110	ns
T_{fall}	Fall time	13.6	9	nS
Q_{gs}	Gate-to-source charge	5.2	4	nC
Q_{gd}	Gate-to-drain ('Miller') charge	7.3	16	nC
Q_g	Total gate charge	19.1	32	nC
t_{rr}	Reverse recovery time	124.0	293	ns
I_{rrm}	Reverse recovery current	11.8	21	A
Q_{rr}	Reverse recovery charge	733.2	3300	nC

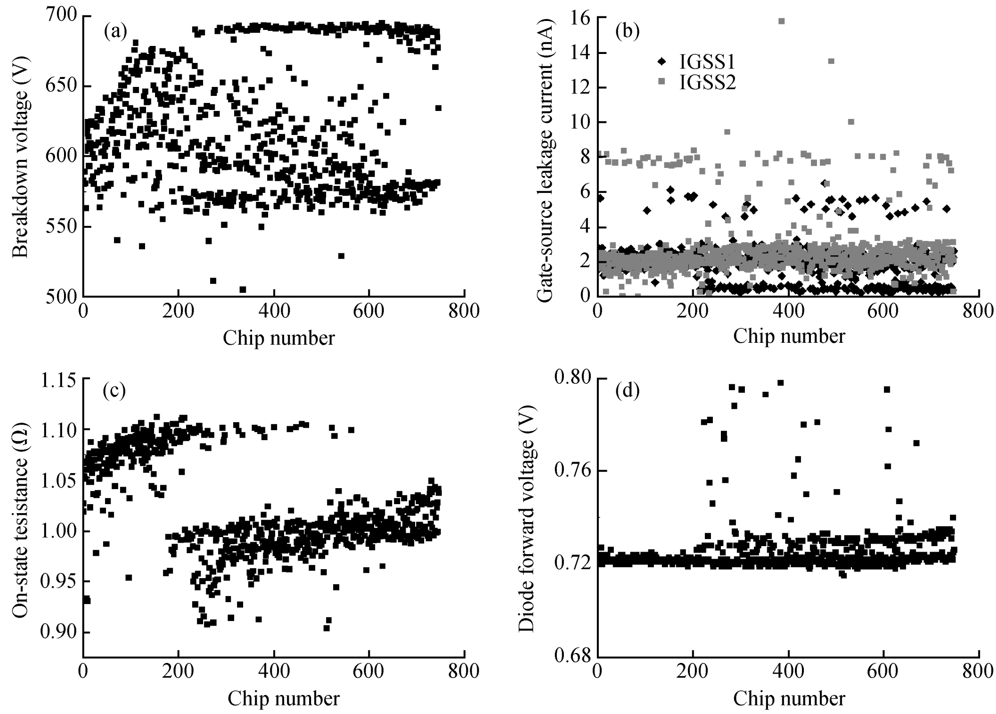


Fig. 7. Statistical characteristic data of the fabricated 800 chips. (a) Breakdown voltage. (b) Gate–source leakage current. (c) On-state resistance. (d) Diode forward voltage.

Table 2. Test conditions.

Parameter	Test condition
I_{GSS1}	V_{gs} = –30 V, V_{ds} = 0 V
I_{GSS2}	V_{gs} = +30 V, V_{ds} = 0 V
B_{VDSS}	V_{gs} = 0 V, I_d = 250 μ A
R_{DSON}	V_{gs} = 10 V, I_d = 1 A
V_{FSD}	V_{gs} = 0 V, I_s = 1 A

Figure 6 shows the measured I–V curves for the SJ-MOSFET. The breakdown voltage and threshold voltage are approximately 750 V and 4 V, coordinating with the simulation. As shown in Table 1, the dynamic characteristics of our SJ-MOSFET, especially the reverse diode characteristics, are equivalent or even superior to the IPx60R380C6 by Infineon.

In order to check the feasibility and reliability of the design and process, we have produced and measured about 800 chips. The test conditions are exhibited in Table 2. The test results in Fig. 7 demonstrate that the design and process of the SJ-MOSFET are available, but the uniformity of the process needs to be improved. Inappropriate resistivity and thickness of the epitaxial layer resulted in big on-state resistances of the fabricated SJ-MOSFETs.

5. Conclusions

Two types of trench structure for 700 V SJ-MOSFETs have been simulated. It has been found that the rectangular trench has a higher breakdown voltage because it develops a flatter electric field distribution compared to the trapeziform one. An SJ process of deep trench etching and epitaxial growth has been developed based on the process platform of HH NEC. The fabricated SJ-MOSFETs have equivalent or superior dynamic performances to their foreign counterparts.

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