A 10-bit 100-Msps low power time-interleaved ADC using OTA sharing*

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Abstract: A high performance 10-bit 100-MS/s two-channel time-interleaved pipelined ADC is designed for intermediate frequency 3G receivers, and OTA is shared among the channels for low power dissipation. Offset mismatch, gain mismatch and time skew mismatch are overcome by OTA sharing, increasing the accuracy of each channel and global passive sampling respectively. The linearity deterioration caused by the charge injection of the output switch and the crosstalk of the off-switch capacitor is removed by modifying the clock signal arrangement. The total power consumption of the presented ADC is 70 mW from a 3.3-V power supply. Fabricated in a 180-nm CMOS process, the core of the prototype occupies an area of 2.5×1.5 mm^2, achieving more than 70-dB spurious-free dynamic range and over 56-dB signal-to-noise distortion ratio over the Nyquist input band at 100-MHz sampling frequency.

Key words: OTA sharing; time-interleave; pipeline; charge injection; crosstalk; low power
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1. Introduction

High-speed medium-resolution pipelined analog-to-digital converters (ADCs) are popular among a variety of applications ranging from communication to image signal processing. The sampling speed of the ADC can be increased proportionately by time-interleaving. Besides high-speed sampling, portability also poses a design challenge to achieve low power consumption. In order to reduce the power consumption, several techniques have been introduced to the pipelined ADC design. Among these, OTA sharing has been proven to be one of the most efficient. By sharing the power hungry OTAs among channels or between sequential stages[1, 2], the analog power consumption is almost reduced by half.

In this paper, a high performance low power 10-bit 100-Msps time-interleaved ADC is proposed to meet the requirement of the IF 3G receiver. Though time-interleaving can increase the sampling speed significantly, it suffers from offset mismatch, gain mismatch and time skew, which will deteriorate the linearity of the ADC[3−5]. These mismatches can be overcome respectively by OTA sharing between channels, increasing the accuracy of each channel and global passive sampling[6]. This paper also studies the error due to the charge injection of the output switch and crosstalk of the off-switch capacitor. By modifying the clock generator and the clock signal arrangement, these effects are eliminated, and the linearity of the presented ADC is significantly improved.

2. Proposed ADC architecture

Time-interleaving plus OTA sharing can reduce the power consumption and also maintain a high sampling frequency. By using two channels, the operating frequency of the multiplying digital-to-analog converter (MDAC) is reduced by half, and the increased number of OTAs due to an extra channel is also reduced by sharing the OTAs between the two channels.

2.1. ADC system structure

The proposed 10-bit 100-MS/s time-interleaved ADC is shown in Fig. 1. It consists of two 10-bit 50-MS/s pipelined ADCs, and each one is composed of an SHA (sample and hold) and five stages. Each of the first two stages employs 3-bit/stage structure to ensure linearity, while the following stages employ 2.5-bit/stage topology. In order to increase power efficiency, the OTAs of the MDAC are shared by two channels, which can decrease the power consumption and reduce the offset mismatch effect. In order to maintain high linearity when the input frequency increases, each channel includes an SHA to catch the high frequency input signal, the OTA of the SHA is also shared between two channels.

2.2. OTA sharing structure

The basic structure of OTA sharing is shown in Fig. 2[6]. The whole system works as follows: when Φ_1 is high, the input signal is sampled on the capacitor of C1, while C2 is connected between the input and output of the OTA, transferring charge

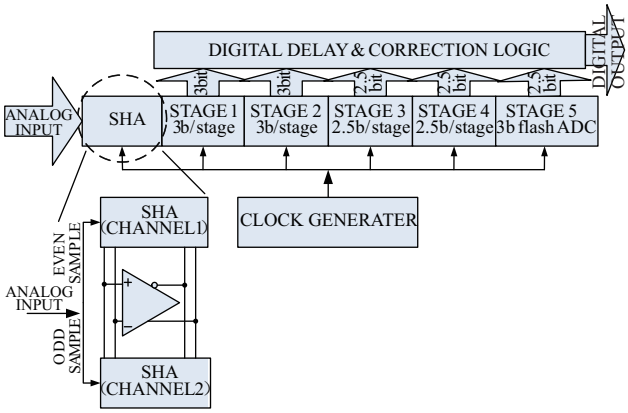

Fig. 1. ADC structure.

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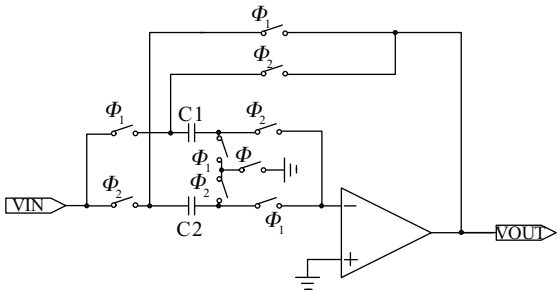

Fig. 2. Typical OTA sharing structure.

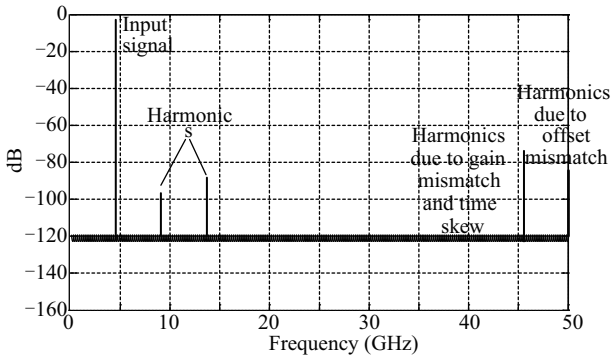

Fig. 3. Tones due to mismatches.

to output voltage; when Φ_2 is high, C2 samples the input signal, and C1 is in the settling phase. Φ is a full speed clock, employed to synchronize the sampling instant, eliminating the time skew mismatch. Though the power consumption can be reduced, unfortunately, the linearity of the ADC is degraded due to any mismatches between the two channels, and the additional switch caused by OTA sharing results in further degradation of linearity[1].

3. Nonideal effects of mismatches and switches

3.1. Nonideal effects of mismatches

Though the power consumption can be reduced, the linearity of the front end SHA is degraded due to any mismatch between two channels[3−5]. As shown in Fig. 3, for two-channel interleaving, offset mismatch causes the tone to be located at frequency of $f_s/2$, where f_s is the sampling frequency. Tones due to gain mismatch and time skew are located at frequency of $f_s/2 - f_{in}$, where f_{in} is the frequency of the input signal. The amplitude of the tone due to time skew is proportional to the square of the input frequency, while tone due to gain mismatch is not.

The linearity deterioration due to these three mismatches can be calculated independently[3].

Assuming that the channel offsets are Gaussian random variables, the linearity deterioration due to offset mismatch can be calculated using

$$\mathrm{SNDR} = 10\lg\frac{A^2}{2\sigma_o^2}, \tag{1}$$

where A is the signal amplitude, and σ_o is the variance of offsets.

The linearity deterioration due to gain mismatch can be calculated using

$$\mathrm{SNDR} = 10\lg\frac{\dfrac{A^2}{2}\overline{g}^2}{\dfrac{A^2}{2}\left(\overline{g^2} - \overline{g}^2\right)}, \tag{2}$$

where $\overline{g}$ is the average gain of channels, and $\overline{g^2}$ is the square of the quadratic mean of the gain.

Assuming that the phase skews are Gaussian random variables, the linearity deterioration due to phase skew can be calculated using

$$\mathrm{SNDR} = 20\lg\frac{1}{w_0\sigma_t}, \tag{3}$$

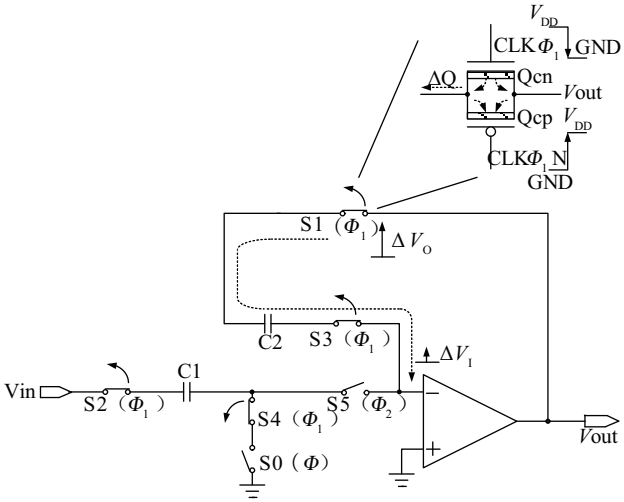

Fig. 4. Charge injection to summing node.

where w_0 is the input frequency, and σ_t is the variance of phase skew.

To eliminate or reduce these mismatch effects, several techniques are employed. The offset mismatch is mainly caused by mismatch of the input pair of transistors of the OTA; in order to remove this effect, the OTA is shared by the MDACs of two channels. As the amplitude of the tone due to gain mismatch is inversely proportional to the square of the gain accuracy, in order to lower the effect of gain mismatch, every channel's resolution is designed to be 11 bit, leaving 1 extra bit to ensure the linearity of the whole ADC. The phase skew error can be removed by global passive sampling[6], which uses one full speed clock to synchronize the sampling moments of the two channels.

3.2. Nonideal effects of switches

Another challenge of OTA sharing is to maintain the charge fidelity at the summing node; the summing node is the input node of the OTA, which is shared by two channels. As the summing node is frequently switched across the two channels, it is vulnerable to crosstalk due to the off-switch capacitor, and the charge injection of the output switch also contributes an error voltage to the summing node.

As shown in Fig. 4, when the settling phase of the SHA finishes, switches S1 and S3, which connect the capacitor across the OTA, turn off simultaneously. It takes some time to make

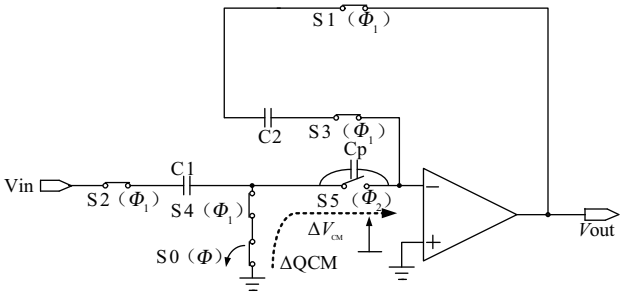

Fig. 5. Summing node crosstalk.

the switch S3 turn off due to the parasitic capacitor of the gate of the switch; during this period, the charge injection caused by the output switch S1 will affect the charge stored on the summing node as the switch S3 has not been completely turned off. In the next phase, this charge will cause a voltage related to the former output on the summing node, which will deteriorate the settling accuracy. Though the charge injection can be reduced by using a small switch, this worsens the stability of the MDAC[7].

The charge injection can be removed by advancing the turning off of switch S3, which is similar to bottom-plate sampling[8]. In this case, switch S3 is turned off first so that the summing node is isolated, free from charge injection[9].

Another factor that affects the settling of the OTA sharing is the crosstalk of the off-switch capacitor. In order to eliminate the phase skew, global passive sampling demands that the switch controlled by the full speed clock turns off before the sampling switch. This, though, ensures that the accuracy of the sampling has a negative influence on the settling of the adjacent channel. Illustrated in Fig. 5, the turning off switch S0 introduces an offset error to the summing node by the off-switch capacitor. This error does not relate to the contemporary input; however, it can affect the settled output. As the output is "stirred" by the opening of S0, the SNDR performance degrades. Because it is a common mode error, it cannot be eliminated by introducing a dummy switch. This error can only be alleviated by moving the falling edge of global clock Φ forward, leaving enough time for the output to resettle. However, as this disturbance is relatively small, the resettling period is short compared with the whole settling period.

4. Circuit implementation

4.1. Improved OTA sharing structure

The proposed OTA sharing SHA structure in Fig. 6 is based on the structure given by Ref. [10]. The clock signals which dictate the sampling moment of the SHA are generated locally in SHA to reduce the time skew between Φ_{1F} and Φ_{2F}. When the full speed clock Φ is high, CTR goes high, pulling Φ_{1F} and Φ_{2F} down to ground; when Φ is low, CTRN goes high, thus making Φ_{1F} follow Φ_1 and Φ_{2F} follow Φ_2. By dictating the falling edge of the pre-phase clock signal Φ_{1F} and Φ_{2F} by a global clock signal Φ, the sampling error raised from phase skew is avoided, and the additional resistance of the extra switch is also eliminated.

The switch to switch of the OTA between two channels is controlled by another pre-phase clock signal Φ_{1e} and Φ_{2e}.

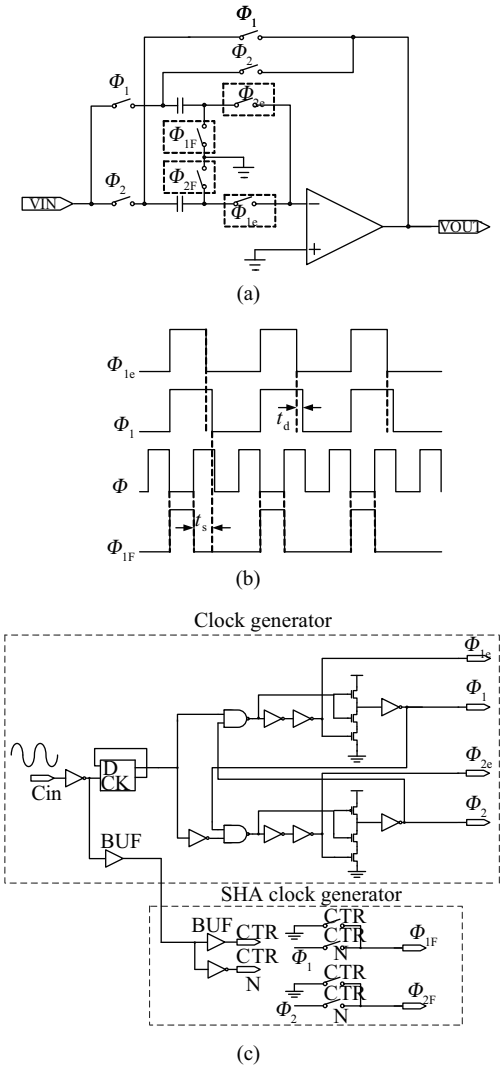

Fig. 6. Proposed double sampling structure. (a) SHA structure. (b) Timing diagram for SHA. (c) Clock generator.

The falling edge of Φ_{1e} is advanced to Φ_1 so that the summing node is isolated before the turning off of the output switch, thus avoiding the charge injection of the output switch. The time interval t_s between the falling edge of Φ_{1F} and the falling edge of Φ_1 should be long enough, so that there is enough time for the SHA to resettle to cancel the nonideal effects of the crosstalk of the off-switch capacitor. However, the charge leakage during t_s makes the linearity decrease, so in order to achieve best performance, careful design and compensation should be done.

The clock signal arrangement of the following stages is slightly different from the clock arrangement of SHA. As the input signal from the previous stage does not change, time skew between the two channels will not import extra tone, so the clock signal of Φ_{1F} and Φ_{2F} is replaced with Φ_{1e} and Φ_{2e} to avoid the charge injection of the sampling switch, while the switch to switch the OTA between two channels is still controlled by Φ_{1e} and Φ_{2e} to avoid the charge injection of the output switch.

4.2. OTA structure

The DC gain of the OTA is a key factor in the OTA sharing design, as the OTA input is never reset, causing a memory ef-

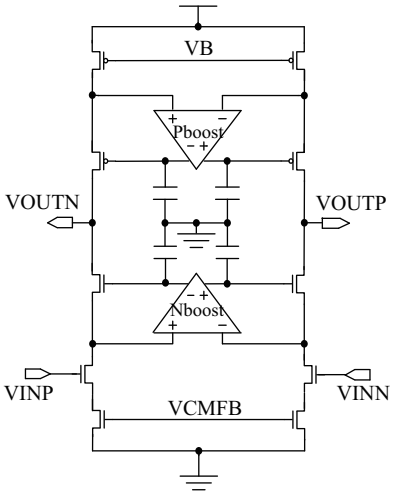

Fig. 7. OTA structure.

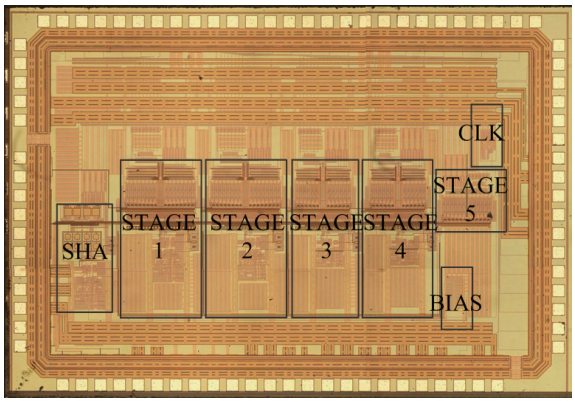

Fig. 8. Die photograph of the ADC.

fect that spurs harmonics degrading the linearity performance of the SHA[1]. In this design a single-stage telescopic amplifier with a conventional gain-boosting circuit is used to achieve high DC gain. The OTA structure is shown in Fig. 7. The proposed amplifier achieves about 70° phase margin, greater than 110-dB DC gain, and more than 2-V output differential swing range for the 3.3-V supply.

5. Measurement results

The 10-bit 100-MS/s time-interleaved ADC is fabricated in 0.18 μm CMOS technology. The die micrograph is shown in Fig. 8. The core of the prototype occupies a die area of 2.5 × 1.5 mm^2, and is composed of SHA, stage1 to stage5, bias circuit and clock generator. The measurement is at room temperature (27 ℃) with a power supply of 3.3 V. The static performances of ADC, including differential nonlinearity (DNL) and integral nonlinearity (INL) are shown in Fig. 9. The DNL is less than 0.23 LSB, while the INL is less than 0.41 LSB. Figure 10 shows the measured spectrum for an input frequency of 4.9 MHz, and Figure 11 shows the spectrum for 49.1-MHz input. The ADC achieves more than 70-dB SFDR and over 56-dB SNDR performance with Nyquist input at 100-MHz sampling rate. As indicated in Fig. 12, the ADC dynamic performance remains relatively good for 10-bit resolution at 100-MS/s sampling rate

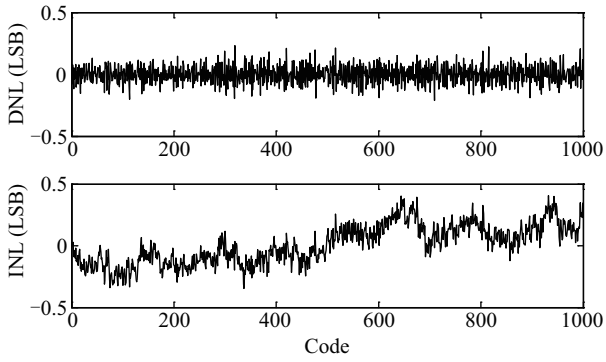

Fig. 9. Measured static performance of the ADC.

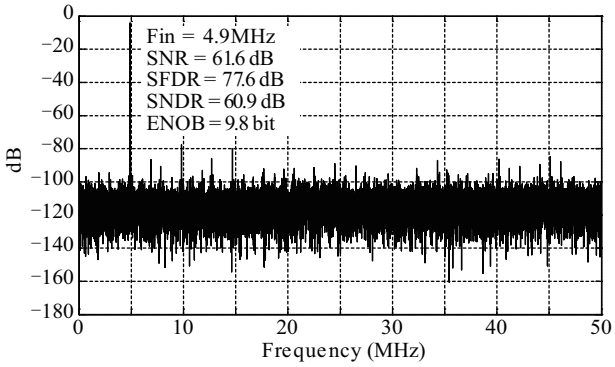

Fig. 10. Dynamic performance of the ADC with 4.9-MHz input.

Table 1. Summary of measured performance.

Parameter	Value
Technology	0.18 μm CMOS
Conversion rate	100 MHz
Resolution	10 bit
Total power	70 mW @ 3.3-V supply
Core area	2.5 × 1.5 mm^2
DNL, INL	–0.21 to 0.23 LSB, –0.35 to 0.41 LSB
SFDR	77.6 dB (f_{in} = 4.9 MHz)
	71.1 dB (f_{in} = 49.1 MHz)
SNDR	60.9 dB (f_{in} = 4.9 MHz)
	56.8 dB (f_{in} = 49.1 MHz)
SNR	61.6 dB (f_{in} = 4.9 MHz)
	58.3 dB (f_{in} = 49.1 MHz)
ENOB	9.8 bit (f_{in} = 4.9 MHz)
	9.2 bit (f_{in} = 49.1 MHz)

for input frequencies up to 99.1 MHz, which is about twice the Nyquist frequency. The dynamic performance becomes worse as the input signal frequency goes higher; this is mainly due to the time skew between two channels. Nonlinearity caused by time skew is proportional to the square of the input frequency. Even though the sampling instants of two channels are synchronized by one global clock, when the input frequency goes higher, the tone due to the mismatch between the generators of Φ_{1F} and Φ_{2F} becomes higher, deteriorating the linearity of the ADC. The ADC performance is summarized in Table 1.

With a 3.3-V supply, the time-interleaved ADC consumes 70 mW. The figure of merit (FOM) is 1.17 pJ/step, and it is

Table 2. Comparison of performance of several ADCs with similar resolution.

	This work	ISCAS01[11]	JSSC03[12]	CICC06[13]	JSSC04[14]	CICC06[15]	ASSCC08[16]	ISOCC09[17]
Bit	10	10	10	10	10	10	10	10
MS/s	100	80	80	100	150	100	100	100
Power (mW)	70	80	69	67	123	76	31	25.2
V_{DD} (V)	3.3	1.8	3	1.8	1.8	1.8	1.8	1.8
DNL/INL	0.23/0.41	0.66/0.76	—	0.8/1.6	0.69/1.5	0.75/1.8	0.48/0.95	0.58/0.94
SFDR (dB)	71.1	64.9	72.8	65	—	69	67	68.3
SNDR (dB)	56.8	55.7	57.7	54 52	57	53	53.2	
ENOB (bit)	9.22	8.97	9.29	8.68	8.34	9.18	8.51	8.54
V_{in} (Frequency) (MHz)	49.1	41	99	1	75	3.99	4.9	4
Technology (μm)	0.18	0.18	0.18	0.18	0.18	0.18	0.18	0.18
OTA sharing	Yes	No	Yes	No	No	No	Yes	Yes
FOM (pJ/step) Nyquist frequency	1.17	1.99	1.38	—	2.53	—	—	—
FOM (pJ/step) DC	0.79	—	—	1.63	—	1.31	0.85	0.68

$$\text{FOM} = \frac{\text{Power}}{2^{\text{ENOB}} \times f_s}$$

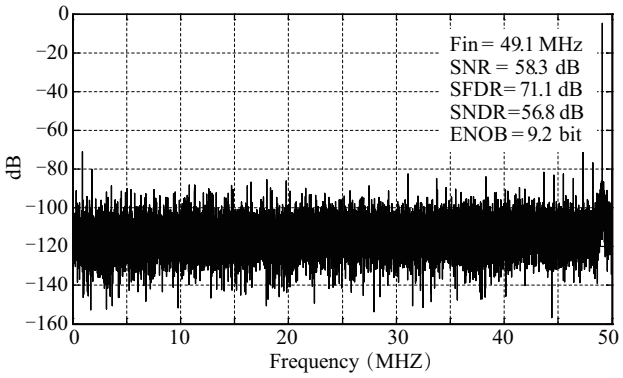

Fig. 11. Dynamic performance of the ADC with 49.1-MHz input.

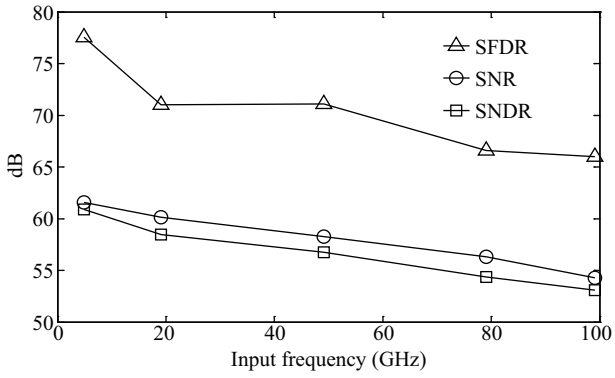

Fig. 12. Measured dynamic performance versus input frequency at 100-MHz sampling rate.

calculated using

$$\text{FOM} = \frac{\text{Power}}{2^{\text{ENOB}} \times f_s}, \quad (4)$$

where Power is the power dissipation, ENOB is the effective number, and f_s is the sampling rate.

Table 2 shows a comparison of the performance of this work with several ADCs with similar resolution and technology. Compared with other ADCs with similar design specifications, the FOM of the Nyquist frequency input of the presented ADC is better than Refs. [11, 12, 14], while the dynamic performance is only slightly inferior to Ref. [12].

The SFDR and ENOB with 4.9-MHz input of this work are 77.6 dB and 9.8 bit respectively as shown in Fig.10, so the FOM of DC is 0.79 pJ/step. The measurements of Refs. [13, 15–17] are performed with an input frequency less than or around 5 MHz; compared with the measurement result of Refs. [13, 15–17], this work is better than Refs. [13, 15, 16] and close to Ref. [17], while the dynamic performance is much better than Refs. [13, 15–17], achieving the best trade-off between power and performance.

6. Conclusion

This paper describes a 10-bit 100-MS/s time-interleaved ADC. Mismatches between channels are overcome by OTA sharing, increasing the accuracy of each channel and global passive sampling. The errors of OTA sharing due to the charge injection of the output switch and the crosstalk of the off-switch capacitor are removed from the output by modifying the clock signal arrangement. With 4.9-MHz and 49.1-MHz input, the ADC achieves 61-dB SNDR, 77-dB SFDR and 56-dB SNDR, 70-dB SFDR in 100-MHz sampling frequency respectively. With a 3.3-V supply the power consumption of the prototype is 70 mW.

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