An 8-bit 180-kS/s differential SAR ADC with a time-domain comparator and 7.97-ENOB*

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Abstract: This paper presents a differential successive approximation register analog-to-digital converter (SAR ADC) with a novel time-domain comparator design for wireless sensor networks. The prototype chip has been implemented in the UMC 0.18-μm 1P6M CMOS process. The proposed ADC achieves a peak ENOB of 7.98 at an input frequency of 39.7 kHz and sampling rate of 180 kHz. With the Nyquist input frequency, 68.49-dB SFDR, 7.97-ENOB is achieved. A simple quadrate layout is adopted to ease the routing complexity of the common-centroid symmetry layout. The ADC maintains a maximum differential nonlinearity of less than 0.08 LSB and integral nonlinearity less than 0.34 LSB by this type of layout.

Key words: successive approximation register; time-domain comparator; analog-to-digital converter
DOI: 10.1088/1674-4926/31/9/095011 **EEACC:** 2570

1. Introduction

Analog-to-digital converters are building blocks in system-on-chips (SOCs) and ultra-wideband (UWB) communication systems. The successive approximation register analog-to-digital converter (SAR ADC) architecture is particularly suitable for applications with moderate speed/resolution, reconfigurability and very low-power consumption. The advantages of wireless sensor networks (WSNs) lie in the development of a low-cost, scalable, and flexible network architecture. A typical wireless sensor node consists of an RF front end, an ADC, an optional microprocessor to process the collected data, and a power supply block. It has been proved that one of the largest sources of power dissipation in most cases is the RF front end and ADC[1−5].

The primary source of power consumption in an SAR ADC is the comparator. The conventional voltage comparator always consists of a preamplifier and latch. The tail current source of the preamplifier always draws static current during normal working mode[6]. The time-domain comparator in Ref. [7] has eliminated static power, it only dissipates dynamic power, so it has achieved a reduction in power consumption, but it can only be applied to a single-ended SAR ADC. Compared with the single-ended SAR structure, the fully-differential circuit structure achieves better common-mode noise rejection and less distortion, but it consumes more power; however, the differential SAR ADC is still the most common circuit in mixed-signal circuits. The goal of this paper is to propose a low power differential SAR ADC that is suitable for application in WSNs, because the differential architecture is highly beneficial for robustness; however, the power consumption of the sensor system is liable to increase with differential architecture, so the proposed ADC is designed to maintain low power with differential architecture by a novel time-domain comparator which dissipates no static power. This novel time-domain comparator can be applied to both single-ended and differential SAR ADCs.

2. ADC architecture

Figure 1 shows a block diagram of an 8 bit converter which comprises a binary-weighted capacitor array, a comparator, an SAR control unit and switches[3]. As shown, this ADC employs a fully differential DAC, which can reject the common-mode disturbances generated by the digital circuits, the clock drivers, etc. Basically, conversion requires three phases[3]: the first is the purging phase, during which both the bottom and top plates of the capacitances are connected to ground. The second is the sampling phase, during which the bottom side of the capacitor array is connected to the input voltage of the ADC and the top side of the capacitor arrays to the common mode voltage V_{CM}. At the sampling mode, all the capacitors are charged to $V_{in} - V_{CM}$. Here, V_{CM} is the common-mode voltage of the input signal. It ensures that equal and opposite charge is stored on each of the capacitor arrays. The third part is the bit-cycling phase, which starts by resolving the MSB. For the first bit cy-

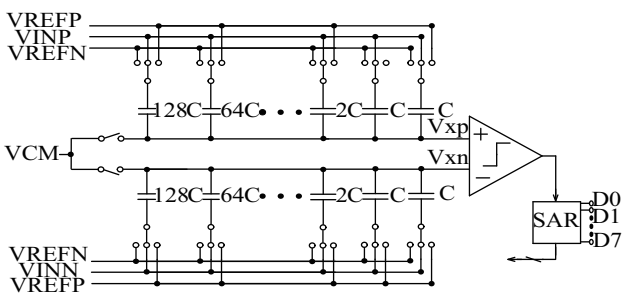

Fig. 1. Block diagram of the differential SAR ADC.

* Project supported by the National Natural Science Foundation of China (No. 60976032).
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Received 29 March 2010, revised manuscript received 26 April 2010

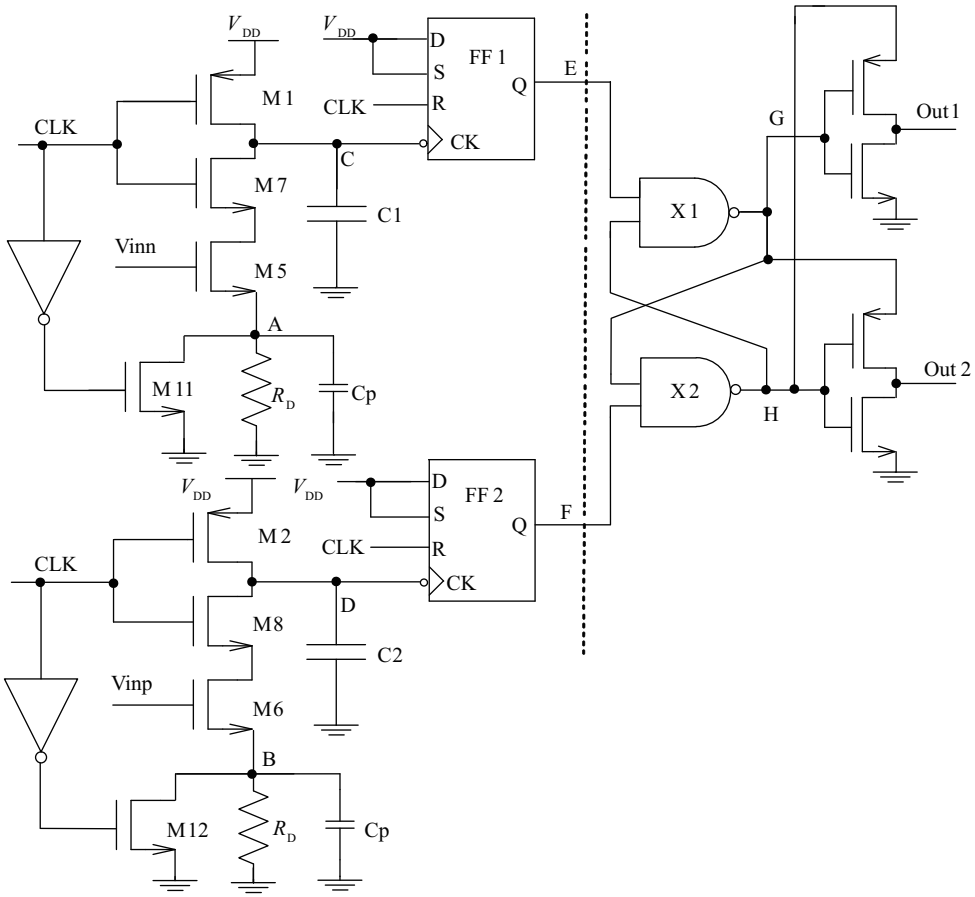

Fig. 2. Time-domain comparator schematic diagram.

cle, the largest capacitance 128C in the positive (negative) array is switched to V_{REFP} (V_{REFN}) while the remaining capacitors are switched to V_{REFN} (V_{REFP}), the resulting structure forms a capacitor divider with equal capacitance from the output to V_{REFP} and V_{REFN}. If MSB is resolved as "1" by the comparator, the MSB capacitor 128C in the positive (negative) remains at V_{REFP} (V_{REFN}). If not, MSB is 0, and 128C in the positive (negative) is connected to V_{REFN} (V_{REFP}). Successive approximation continues in this fashion for the remaining bits, finally, V_{xp} and V_{xn} converge towards the common mode voltage V_{CM}. The change in V_{xp} and V_{xn} can be calculated as follows:

$$V_{xp} = V_{cm} - V_{inp} + \sum_{j=0}^{7} \frac{D_j C_j}{C_{total}} V_{refp} + \sum_{j=0}^{7} D_j \left(1 - \frac{C_j}{C_{total}}\right) V_{refn}, \tag{1}$$

$$V_{xn} = V_{cm} - V_{inn} + \sum_{j=0}^{7} \frac{D_j C_j}{C_{total}} V_{refn} + \sum_{j=0}^{7} D_j \left(1 - \frac{C_j}{C_{total}}\right) V_{refp}. \tag{2}$$

3. Circuit implementation

3.1. A novel time-domain comparator

Figure 2 shows the circuit schematic of the proposed time-domain comparator. Compared with the conventional voltage comparator, this time-domain comparator eliminates static power and can be applied to both single-ended and differential SAR ADCs. It is a combination of two voltage-to-time converters[7] and an arbiter circuit[8]. The flip-flops FF1 and FF2 are set (S) and reset (R) on the negative level. When the signal CLK is low, transistors M1 and M2 charge the nominally equal capacitors C1 and C2 to V_{DD}, while nodes A and B are discharged to remove any residual charge, nodes E and F, which are outputs of flip-flops FF1 and FF2, are reset to 0, so G and H are initially set to high and Out1, Out2 are reset to 0. When CLK makes the transition high, transistors M5 and M6 become constant current generators and discharge capacitors C1 and C2 at a constant rate. When the voltage across C1 and C2 crosses the threshold voltage of flip-flops FF1 and FF2, the flip-flops are triggered by the negative clock edge and transmit the data (V_{DD}) to the following arbiter circuit, which consists of two NAND gates (X1 and X2) and the following two inverters. The arbiter reveals the pulse that arrives first and provides the comparator output. For example, if $V_{INN} > V_{INP}$, the voltage of node C drops faster than node D, so E first goes high, then G goes low and Out1 becomes high. It should be mentioned that the moment G goes to low, the supply of the bottom inverter disappears, so Out2 and Out1 will not become high simultaneously.

One of the inputs of the time-domain comparator in Ref. [6] is connected to a fixed voltage, V_B, which must be large enough to ensure that M6 is on when CLK is high so as to provide the reference pulse. This time-domain comparator in Ref. [6] is not suitable for a differential SAR ADC. The proposed time-

domain comparator can be applied to both single-ended and differential SAR ADCs.

The accuracy of the comparator is mainly determined by KT/C noise, the latch time margin ΔT (the minimum delay between set and clock to ensure correct latching)[6].

According to i$\Delta t = C\Delta$, we can get:

$$\frac{V_{\text{inn}} - V_{\text{gs5}}}{R_{\text{D}}}\Delta t_1 = C\Delta V_{\text{out1}}, \tag{3}$$

$$\frac{V_{\text{inp}} - V_{\text{gs6}}}{R_{\text{D}}}\Delta t_2 = C\Delta V_{\text{out2}}. \tag{4}$$

At this point $V_{\text{inn}} \approx V_{\text{inp}} \approx V_{\text{cm}}$, we can get:

$$\Delta V_{\text{out1}} \approx \Delta V_{\text{out2}} = \Delta V_{\text{out}} \Rightarrow \Delta t_1 = \frac{R_{\text{D}}C\Delta V_{\text{out}}}{V_{\text{inn}} - V_{\text{gs5}}}, \tag{5}$$

$$\Delta t_2 = \frac{R_{\text{D}}C\Delta V_{\text{out}}}{V_{\text{inp}} - V_{\text{gs6}}}. \tag{6}$$

According to Eqs. (3) and (4), we can get:

$$\Delta T = \Delta t_1 - \Delta t_2 \approx \frac{R_{\text{D}}C\Delta V_{\text{out}}\Delta V_{\text{in}}}{(V_{\text{cm}} - V_{\text{gs5, 6}})^2}. \tag{7}$$

So the error voltage caused by latch time margin ΔV_{in} is equal to:

$$\Delta V_{\text{in}} = \frac{\Delta T(V_{\text{cm}} - V_{\text{gs5, 6}})^2}{R_{\text{D}}C\Delta V_{\text{out}}}. \tag{8}$$

The KT/C error voltage caused by charging and discharging capacitance is equal to:

$$\overline{V_{\text{C noise}}} = \sqrt{\frac{2KT}{C}}. \tag{9}$$

In conclusion, the accuracy of the comparator is mainly determined by Eqs. (6) and (7); the accuracy of the comparator can be improved by increasing the capacitance and resistor value.

The accuracy of this proposed comparator is about 90 μV, which is enough even for a 12-bit ADC.

3.2. Capacitor and switch array

The whole capacitor and switch array are used as a sample and hold stage and as a DAC to perform the successive approximation. During sampling, the input is sampled by two sets of capacitor arrays that are coupled, through the top-plate sampling switch. During bit-cycling, the charge redistribution process is controlled by switches in the positive and negative switch matrices, which drive the bottom-plates of the capacitors to the appropriate voltages. The linearity of the SAR ADC is dependent upon the capacitor matching in the capacitor array. To improve the capacitor matching accuracy, the common-centroid layout is usually adopted[15]. The total capacitance of the positive (negative) capacitor array is 256 C_{unit}; routing such great numbers of unit capacitances placed in a common-centroid symmetry is quite difficult, so the conventional common-centroid layout is not applied here. Moreover, some signal lines pass through the capacitors, and the parasitic coupling between the two plates of the capacitors and routing

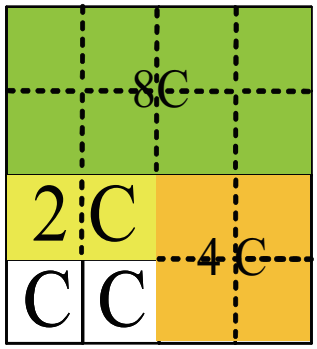

Fig. 3. Layout of a 4-bit capacitor array.

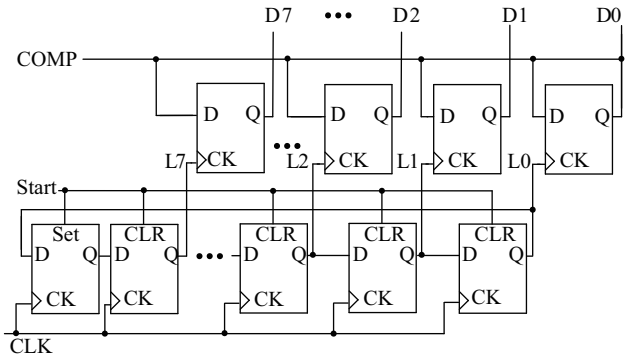

Fig. 4. Schematic of the SAR logic.

lines influence the linearity of the ADC. Here, the signal lines do not pass through the plates of capacitances and an array of dummy capacitors are used around every unit capacitance to ensure a uniform etch environment[16], and each capacitor in the capacitor array consists of numbers of unit capacitors. A unit capacitance of about 50 fF metal–insulator–metal capacitor (MIMCAP of 7 × 7 μm^2) is chosen to guarantee the 8-bit linearity requirement. For simplicity, Figure 3 shows a 4-bit example of the proposed capacitor array layout. This type of layout has not only greatly decreased the routing complexity but also maintained good linearity. The ADC maintains a maximum DNL of less than 0.08 LSB, and INL less than 0.34 LSB by this type of layout.

3.3. SAR logic circuit

The SAR logic block provides all the control signals which ensure that the switches and the comparator work correctly, and generates the digital output codes. The core state logic, in this SAR, consists of a cyclic shift register, which makes up the bottom row of flip-flops shown in Fig. 4 and a set of switch drive registers[14], as shown in the top row in Fig. 4. The conversion is initiated by a step signal, Start, which sets the first flip-flop in the shift register and resets the remaining flip-flops. Following the Start step signal, the Li signal of the cyclic shift register is successively asserted, enabling their associated switch drive registers. The current bit being resolved is determined by L7–L0, only one of which is high every period. Di asserts on the rising edge of Li at the start of the decision period for bit i. When Li falls, the decision for that bit is made, bringing Di back low only if COMP is low.

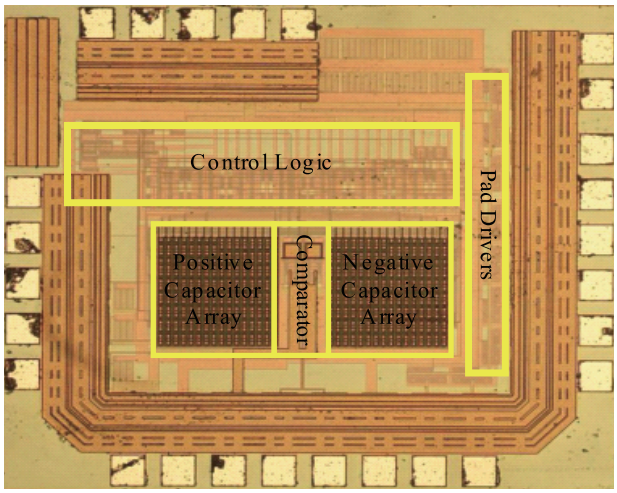

Fig. 5. Die photograph of the ADC.

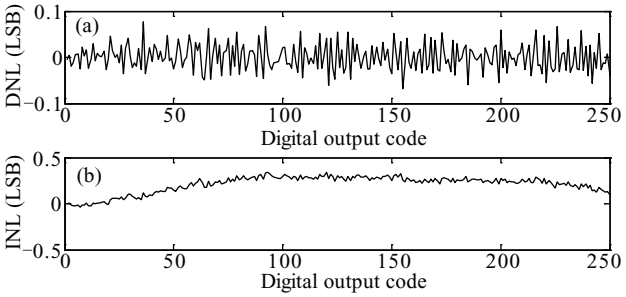

Fig. 6. Measured static performance of the ADC. (a) DNL. (b) INL.

4. Implementation and measured results

The ADC is designed in a 0.18-μm standard CMOS process with a core area of 0.65 mm^2. Figure 5 presents a die photograph, while Figure 6 shows the static performance measured using a code density test with a full swing sinusoidal input. To test the 8-bit ADC, more than 1 million samples were taken. Here the ADC differential nonlinearity (DNL) and integral nonlinearity (INL) are less than 0.08 LSB and 0.34 LSB respectively, so the accuracy of the ADC is nearly ideal. Figure 7 shows the measured spectrum for the input frequencies of 89.7 and 199.7 kHz. The ADC achieves 49.73-dB SNDR and about 68.5-dB SFDR performance with Nyquist input at the full sampling rate. In Fig. 8, it achieves a peak SNDR of 49.81 dB (7.98-ENOB) at an input frequency of 39.7 kHz and the SFDR performance does not degrade with the increase of input frequency. As indicated in Fig. 8, the ADC dynamic performance remains relatively constant at 180-kS/s sampling rate for input frequency up to 200 kHz, which is over twice the Nyquist frequency. The total power consumption of the ADC (including the output pad driver digital power) is 86.76 μW at 1.8-V supply. To evaluate the efficiency of the ADC, the typical figure of merit (FOM) definition of the ADC is defined as:

$$\mathrm{FOM} = \frac{\mathrm{Power}}{2^{\mathrm{ENOB}} \times f_{\mathrm{s}}}. \tag{10}$$

The FOM of this work corresponds to 1.93 pJ/conversion-step. Table 1 summarizes the ADC performance and compares this work with other recently reported work. The main objective is to achieve the best linearity while ensuring that the power consumption satisfies the WSN system specifications. Table 1 shows that the proposed SAR ADC achieves the best ENOB, SNDR, DNL and SFDR of all these ADCs. Reference [12] achieves the lowest FOM, but it is a single-ended SAR ADC, which cannot effectively reject supply rail, ground and substrate disturbances in practical applications. This proposed converter also features a better ENOB than MAXIM's similar product (MAX1110) which is an 8-bit 50-kS/s SAR ADC and has an ENOB of 7.85 and 68-dB SFDR.

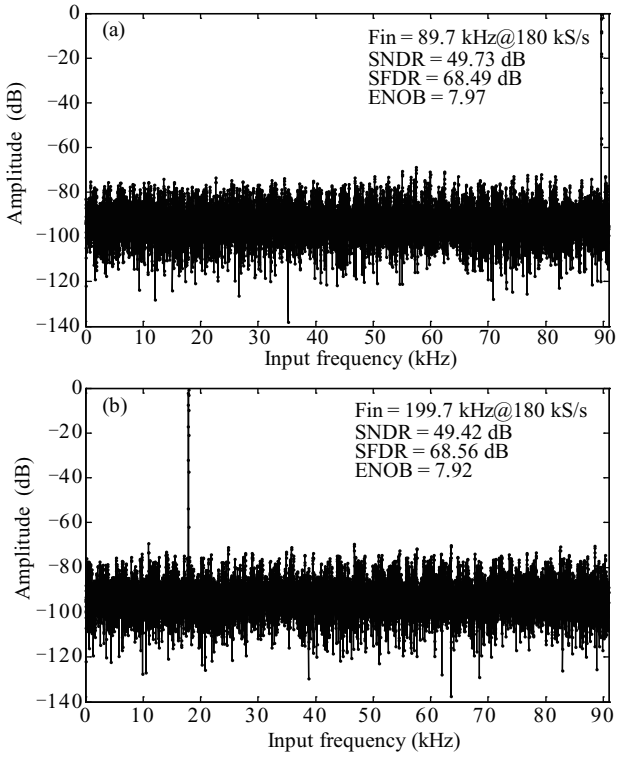

Fig. 7. Measured dynamic performance of the ADC with (a) 89.7-kHz input and (b) 199.7-kHz input.

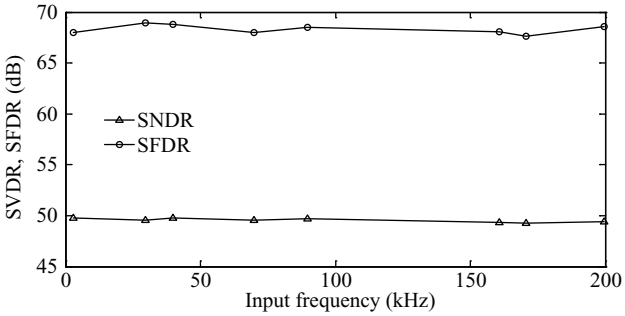

Fig. 8. Measured dynamic performance versus input frequency at 180-kHz sampling rate.

5. Conclusions

This paper describes an 8-bit 180-kS/s differential ADC with a novel time-domain comparator which can be applied to

Table 1. Summary of measured performance and comparison of the performance of several ADCs.

Parameter	This work	JSSC, 2003[11]	JSSC, 2007[12]	ASSCC, 2007[10]
Bits	8	8	8	8
kS/s	180	1.5	200	500
Input signal swing	±1	0.125	1	—
Technology (μm)	0.18	0.18	0.18	0.18
DNL (LSB)	–0.07 to 0.08	—	–0.9 to 0.26	–0.24 to 0.17
INL (LSB)	–0.01 to 0.34	—	–0.53 to 0.5	–0.28 to 0.31
Supply voltage (V)	1.8	0.45	0.9	1
Power (μW)	87	0.49	2.47	7.75
SFDR (dB)	68.49 (f_{in} = 89.7 kHz) 68.56 (f_{in} = 199.7 kHz)	—	58.9	62.69
SNDR (dB)	49.73 (f_{in} = 89.7 kHz) 49.42 (f_{in} = 199.7 kHz)	41.8	47.4	46.92
ENOB	7.97 (f_{in} = 89.7 kHz) 7.92 (f_{in} = 199.7 kHz)	6.65	7.58	7.5
FOM (pJ/step)	1.93	3.25	0.065	0.086

both single-ended and differential SAR ADCs. The input signal swing is ±1 V. The proposed ADC achieves a peak ENOB of 7.98 at an input frequency of 39.7 kHz and gets an ENOB of 7.97 at the Nyquist input frequency. Moreover, it preserves a 7.92-ENOB at an input frequency up to twice the Nyquist input frequency. Including the output pad drivers' digital power, the converter dissipates only 86.76 μW from a 1.8-V power supply at a sampling rate of 180-kS/s, which is comparably low among SAR ADCs with moderate resolution and speed.

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