A high precision high PSRR bandgap reference with thermal hysteresis protection*

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Abstract: To meet the accuracy requirement for the bandgap voltage reference by the increasing data conversion precision of integrated circuits, a high-order curvature-compensated bandgap voltage reference is presented employing the characteristic of bipolar transistor current gain exponentially changing with temperature variations. In addition, an over-temperature protection circuit with a thermal hysteresis function to prevent thermal oscillation is proposed. Based on the CSMC 0.5 μm 20 V BCD process, the designed circuit is implemented; the active die area is 0.17×0.20 mm^2. Simulation and testing results show that the temperature coefficient is 13.7 ppm/K with temperature ranging from –40 to 150 ℃, the power supply rejection ratio is –98.2 dB, the line regulation is 0.3 mV/V, and the power consumption is only 0.38 mW. The proposed bandgap voltage reference has good characteristics such as small area, low power consumption, good temperature stability, high power supply rejection ratio, as well as low line regulation. This circuit can effectively prevent thermal oscillation and is suitable for on-chip voltage reference in high precision analog, digital and mixed systems.

Key words: bandgap voltage reference; curvature-compensated; power supply rejection ratio; over-temperature protection; BCD process

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1. Introduction

The bandgap voltage reference (BGR) is in great demand in most integrated analog, digital or mixed signal systems, such as ADC, DAC, switching power supply and PLL, for its low temperature drift in a large temperature range (TR) and high power supply rejection ratio (PSRR), and it has been one of the essential components to affect the performance of high stability electronic products. With the continuous improvement of integrated circuit (IC) design precision and process technology, the traditional first-order temperature-compensated BGR has already been unable to meet the application requirements sufficiently with a temperature coefficient (TC) over 20 ppm/K, so many high-order temperature-compensated techniques have been proposed[1−7]. With these techniques, the temperature stability of the BGR has been increased significantly. However, each BGR structure has respective drawbacks for some applications. In short, a proper BGR is a tradeoff of performance, structural complexity, size, power and process constraints. In addition, to achieve a high performance voltage reference, it is necessary to pay more attention to some other important parameters like PSRR, TR, line regulation and thermal protection, and so forth.

This paper describes a high-order curvature-compensated BGR, which utilizes the characteristic of bipolar transistor current gain β exponentially changing with temperature variations to compensate the high-order temperature item in the conventional BGR. Meanwhile, in order to avoid thermal oscillation an over-temperature protection block with a thermal hysteresis function is added, which greatly improves the stability of the BGR. The circuit is designed and fabricated in CSMC 0.5 μm 20 V BCD technology. Both simulation and testing results reveal that the proposed BGR has good temperature stability in a large TR and high PSRR, as well as effective thermal oscillation prevention at a cost of small area and low power consumption.

2. Conventional first-order temperature-compensated BGR

The core of the conventional first-order temperature-compensated BGR is shown in Fig. 1. The output bandgap volt-

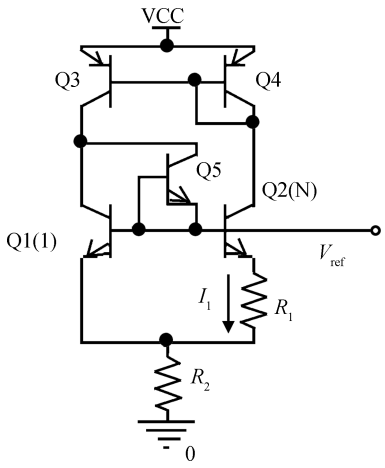

Fig. 1. First-order temperature-compensated BGR.

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age reference $V_{\rm ref}$ is a weighted sum of a negative TC voltage $V_{\rm BE}$ which is the forward-bias voltage across a p–n junction, and a positive TC voltage $V_{\rm T}$ which is the thermal voltage kT/q, proportional to absolute temperature (PTAT). Here, k is Boltzmann's constant, T is the absolute temperature, and q is the charge of an electron. $V_{\rm ref}$ should be insensitive to the temperature changes and stable over the range of supply voltage changes in the first-order compensation. As shown in Fig. 1, $V_{\rm ref}$ is given as:

$$V_{\rm ref} = V_{\rm BE\_Q1} + 2V_{\rm T}\ln(N)R_2/R_1, \tag{1}$$

where N is the ratio of the emitter area of Q2 and Q1. The second item is proportional to PTAT, which is used to compensate the negative TC of $V_{\rm BE\_Q1}$. But the first-order compensated BGR only cancels the negative temperature dependence of the base–emitter voltage $V_{\rm BE}$ by adding a PTAT voltage, which is a fully linear function of T. The relationship between $V_{\rm BE}$ and T, however, shows nonlinear behavior, and $V_{\rm BE}$ is a complex function of T containing many higher order items. The temperature characteristic of $V_{\rm BE}$ is studied extensively and expressed as:

$$V_{\rm BE}(T) = V_{\rm G0} - [V_{\rm G0} - V_{\rm BE}(T_{\rm R})] \times \frac{T}{T_{\rm R}} + V_{\rm T}(\eta - \alpha)\ln\frac{T}{T_{\rm R}}, \tag{2}$$

where $V_{\rm G0}$ is the bandgap voltage of silicon extrapolated at 0 K, $T_{\rm R}$ is the reference temperature, $V_{\rm BE}(T_{\rm R})$ is the base–emitter voltage of the npn transistor at $T_{\rm R}$, η is a temperature constant depending on the technology, and a is the order of the temperature dependence of the collector current. When $I_{\rm C}$ is proportional to the PTAT current $a = 0$, otherwise $a = 1$. As shown in Eq. (2), the first item of $V_{\rm BE}$ is independent of temperature, and the second and third items are linear and high-order nonlinear dependent on temperature respectively. Comparing with Eqs. (1) and (2) reveals that the conventional BGR only eliminates the first-order T term of $V_{\rm BE}$ by $\Delta V_{\rm BE}$ and fails to compensate the high-order T terms, especially $T\ln T$ in $V_{\rm BE}(T)$. As a result, the typical TC of the first-order BGR is approximately larger than 20 ppm/K in the industrial TR (–50 to 125 ℃)[1, 8]. With the rapid development of deep sub-micron and ultra-deep sub-micron IC technology, especially the increasing data conversion accuracy, the conventional BGR can no longer meet the requirements. Therefore, a high-order temperature-compensated BGR with a lower temperature drift over a wider TR and high PSRR is needed.

3. High-order curvature-compensated BGR

A BGR employing the characteristic of bipolar transistor current gain β exponentially changing with temperature variations to compensate the high-order T item is proposed in this section, as shown in Fig. 2. The current gain β is written as:

$$\beta(T) = \beta_\infty \exp\left(-\frac{\Delta E_{\rm G}}{kT}\right), \tag{3}$$

where $\Delta E_{\rm G}$ is the bandgap narrowing factor of the emitter proportional to the emitter doping level, and β_∞ is a scale factor independent of T. This temperature dependence is the consequence of the emitter bandgap decrease, caused by the large

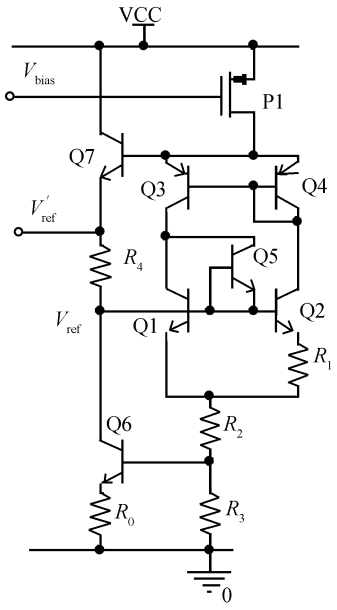

Fig. 2. High-order curvature-compensated BGR.

number of dislocations and lattice deformations at high doping levels. The exponential compensation is realized by Q6, Q7, R_0, R_1 and R_3, thus

$$I_{\rm B\_Q6} = \frac{2\dfrac{\Delta V_{\rm BE}}{R_1} - \dfrac{V_{\rm BE\_Q6}}{R_3}}{1 + \beta_{\rm Q6}\dfrac{R_0}{R_3}}. \tag{4}$$

The output voltage $V_{\rm ref}$ of the exponential-compensated BGR is derived as

$$V_{\rm ref} = V_{\rm BE\_Q1} + 2\frac{V_{\rm T}\ln N}{R_1}R_2 + \left(2\frac{V_{\rm T}\ln N}{R_1} - I_{\rm B\_Q6}\right)R_3. \tag{5}$$

Assuming $1 + \beta_{\rm Q6}\frac{R_0}{R_3} \approx \beta_{\rm Q6}\frac{R_0}{R_3}$, combining Eqs. (4) and (5) gives

$$V_{\rm ref} = V_{\rm BE\_Q1} + K_1 T + K_2 T\exp\frac{\Delta E_{\rm G}}{kT}, \tag{6}$$

where K_1 and K_2 are both optimization parameters, K_1 compensates the linear term of $V_{\rm BE}$, and K_2 does the same for the curvature term. After optimization, only higher order terms equal to or greater than three remain in $V_{\rm ref}$. By adjusting K_1 and K_2, the temperature drift of $V_{\rm ref}$ can be minimized. This technique uses the base current of Q6 as the curvature compensation source, and needs no extra circuitry required in the conventional second-order compensated BGR to generate bias currents for curvature compensation; moreover, it possesses a superior temperature stability. Briefly, this structure achieves simple and efficient temperature compensation with small size and low power consumption, and is suitable for data conversion applications which require a precision voltage reference.

For the clamping of Q1, Q2 and resistors R_1–R_3, Q6 is forced to work between the active region and the cutoff region. Q7 serves as a current source to provide a stable bias current for the core of BGR and minimizes the nonlinear temperature

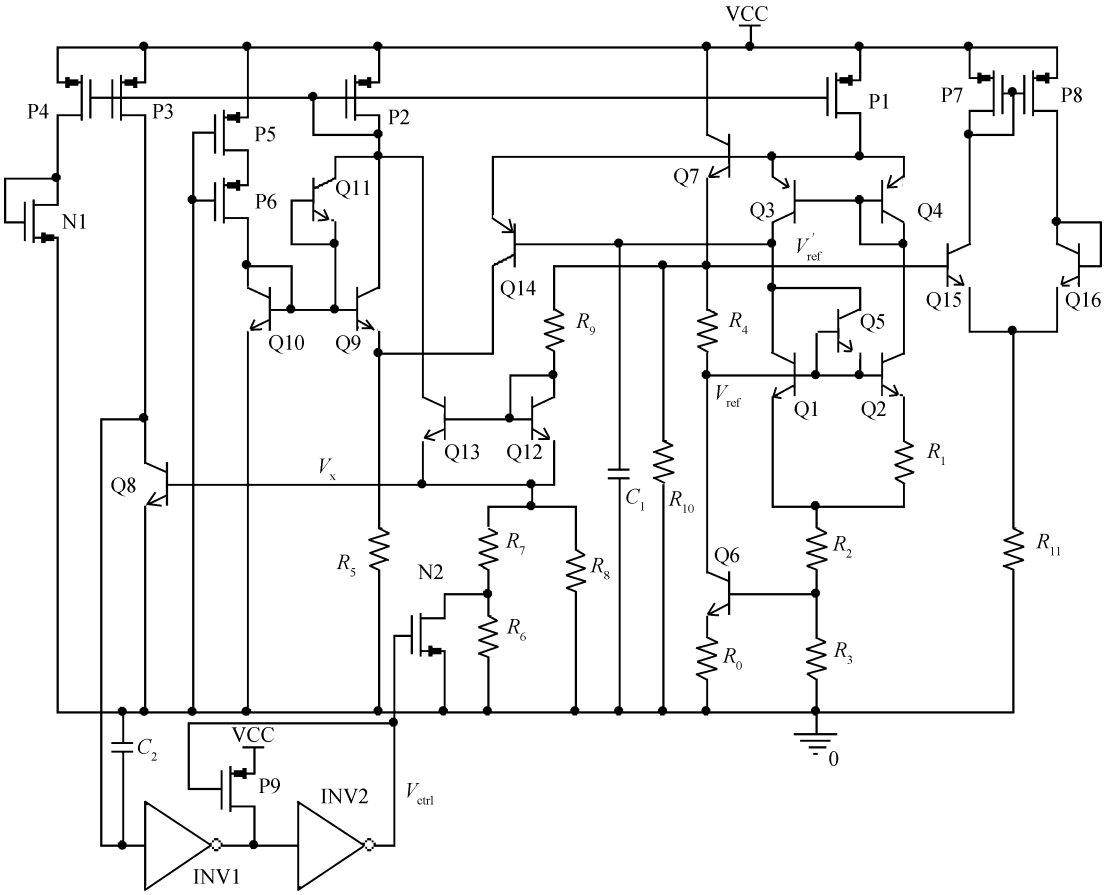

Fig. 3. Whole circuit of the proposed BGR.

drift of V_{ref}. Since the voltage across R_4 is small enough, V'_{ref} is believed to be equal to V_{ref} in the stable working state (this has been proved by the simulation and testing results). Q5 acts as a reverse-biased diode which has a reverse saturation current as a temperature-sensitive function. When the temperature rises, the reverse current of Q5 increases, which compensates the current incremental in ΔV_{BE} caused by PTAT current. The transistor P1 isolates the core of the BGR from the power supply to significantly improve the PSRR. The BGR is designed in the BCD process, which is compatibly bipolar with a high transconductance strong load-drive capability, CMOS with the high integration low power consumption, and DMOS with the high voltage-tolerance. The BCD process is an ideal process for developing monolithic power IC, such as power management IC and motor drive IC[9, 10].

4. Over-temperature protection circuit with thermal oscillation prevention

When the output load current changes, the temperature of the chip may surge[11, 12]; even worse, in the vicinity of the over-temperature threshold thermal oscillation may occur repeatedly, so an over-temperature protection circuit with a thermal hysteresis function is introduced.

The over-temperature protection block consists of Q8, Q12, Q13, N2 and R_6–R_9, shown in Fig. 3. When the working temperature of the chip drops to 130 ℃ or lower, BGR operates smoothly. There is no current flowing through the resistor R_4 (ignoring the base currents of Q1 and Q2); V'_{ref} is equal to V_{ref}. The base voltage V_x of Q8 is smaller than its turn-on threshold V_{BE_ON}, Q8 is cut off and its collector potential is high, that is, V_{ctrl} is high, which makes N2 open and R_6 short. Supposing that the on-resistance of N2 is ignored, the base voltage of Q8 is

$$V_{x(on)} = I_x(R_7//R_8), \tag{7}$$

where I_x is the sum of currents flowing through the emitters of Q12 and Q13, and is determined by V_{ref}, V_{BE_Q12} and resistors R_6–R_9, neglecting the base current of Q8. P9 acts as an electrical level restorer in the logic circuit to accelerate the slew rate of the circuit, as well as eliminating the static power of the inverters. Once the working temperature of the chip exceeds 150 ℃, for the negative TC of V_{BE_Q8}, $V_x > V_{BE\_ON}$, Q8 switches on, the V_{ctrl} signal is pulled down and N2 shuts off; the base voltage of Q8 is now

$$V_{x(off)} = I_x((R_7 + R_6)//R_8). \tag{8}$$

A low V_{ctrl} signal at 150 ℃ could be able to cut off the high power devices in the chip, thereby reducing the temperature of the chip and power consumption. The circuit stops working until the temperature is lower than 130 ℃. There is a hysteresis temperature range of 20 ℃ to avoid the possible thermal oscillation occurring near the temperature protection threshold, which can be adjusted by R_6. The current mirror (CM) constituted by Q12 and Q13 is used to reduce the sensitivity of V_{ref}

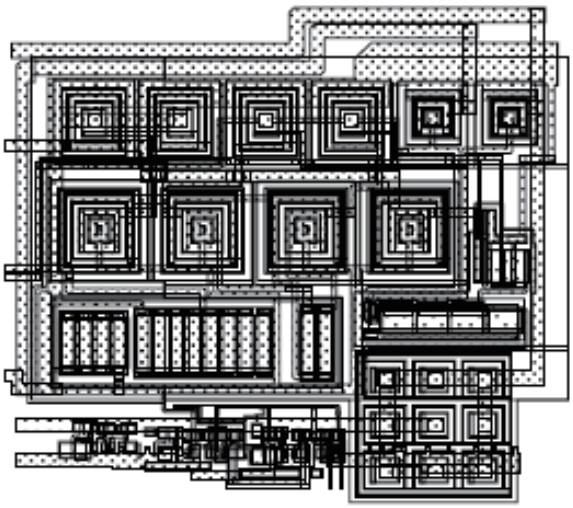

Fig. 4. High-order curvature-compensated BGR layout.

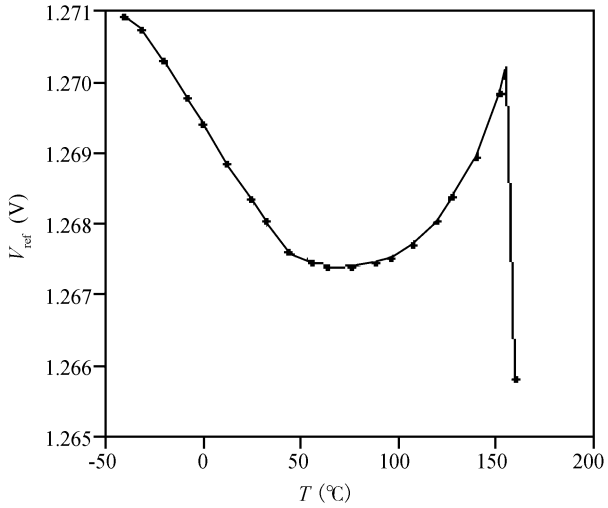

Fig. 5. Output reference V_{ref} versus temperature.

to the current changes. In detail, as the temperature exceeds 150 ℃, I_x decreases and the current reduction is divided into two parts by the CM: one branch through Q13 is fed back to the BGR core by Q9 and Q14, therefore generating a voltage increment at V_{ref}; another branch through Q12 is fed back to V'_{ref}, thus generating a voltage increment, too. Consequently, the voltage floating on R_4 remains zero.

The start-up circuit is composed of P5, P6 and Q10, shown in Fig. 3, which provides a stable bias voltage once the chip powers up. By mirroring of Q9 and P2 the bias voltage is converted into current for the BGR core. Q11 conducts as a negative feedback loop to stabilize the current through Q9. To reduce the impact of the load current a voltage follower is set up at the output for buffering and isolation. The proposed BGR consumes a small area and has low power consumption to achieve a low temperature drift and high PSRR, and greatly inhibits the noises caused by the power supply and process, with excellent thermal oscillation prevention. The BGR is very suitable to be integrated into high precision power management chips.

In order to minimize process errors and improve process consistency, Q1 and Q2 adopt a common centro-symmetric structure in the layout design, thus raising the matching accuracy of area ratio N. The proportion resistances are planned to be a cross-packed structure with external dummy components. All key devices are protected by dual guard ring isolation to further reduce the impact of substrate noise. The active die area is 0.17×0.20 mm^2, as shown in Fig. 4.

5. Results and discussion

The proposed BGR was simulated and fabricated in the CSMC 0.5 μm 20 V BCD process on the basis of the BSIM3V3 model in Cadence Hspice at a single supply of 3.3 V. The resistors R_1–R_3 employ n diffusion resistors with a TC of 0.00518 ppm/K, while R_0 and R_4 use p diffusion resistors with a TC of –0.00305 ppm/K. The simulated waveform of the output reference voltage V_{ref} is depicted in Fig. 5. The maximum variation of V_{ref} is 3.4 mV in the range of –40 to 150 ℃ with a TC of 12.8 ppm/K. When the temperature is beyond 150 ℃, the over-temperature circuit begins to work, thereby decreasing V_{ref} rapidly. Figure 6 presents a plot of the simulated PSRR, which is –98.2 dB at a low frequency of 10 kHz. This is adequate for most power management chip applications. The line regulation is 0.3 mV/V with a supply voltage variation of 2.7–5 V. Figure 7 shows a plot of the measured output voltage ver-

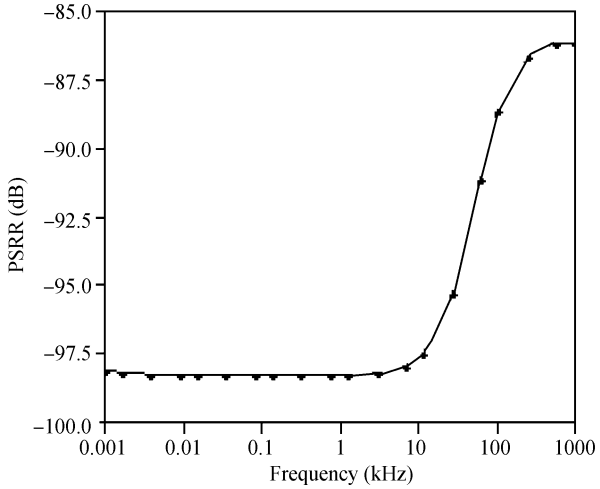

Fig. 6. Response of PSRR.

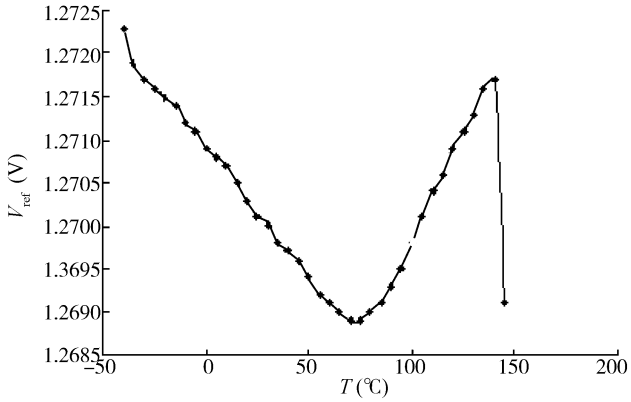

Fig. 7. Measured BGR temperature coefficient.

Table 1. Performance list of the first-order and proposed BGR.

	Process (μm)	PSRR (dB)	TC (ppm/K)	Line regulation (mV/V)	TR (℃)
Conventional first-order BGR	0.5	–50	22.7	2.3	–40 to 125
Ref. [1]	0.35	–82	5	0.6	–50 to 125
Ref. [2]	0.35	93	3.5	—	–40 to 125
Ref. [3]	0.5	—	5.6	0.2	–20 to 100
Ref. [4]	0.18	—	1	—	–40 to 125
Ref. [5]	0.5	66.7	2.7	—	–20 to 80
Ref. [6]	0.5	—	4.6	1.6	–40 to 125
Ref. [7]	0.18	55	10	—	0 to 150
Proposed high-order BGR	0.5	–98.2	12.8	0.3	–40 to 150
Performance improvement of proposed BGR compared with the conventional one	—	1.96	1.77	7.67	—

sus temperature varying from –40 to 150 ℃ with a power supply of 3.3 V. The output voltage has a maximum variation of 3.5 mV and the TC is about 13.7 ppm/K. It can be seen that the TCs of simulation and testing stay almost consistent. The measured output voltage values at different temperature points are generally higher than the simulated values by 1.5 mV, and the measured over-temperature protection threshold is 145 ℃, which is lower than the simulated one. All these deviations are acceptable and may come from process errors and model errors. The measured results verify the correctness and feasibility of the proposed BGR.

Finally, Table 1 briefly compares the high-order curvature-compensated BGR proposed in this paper with the conventional first-order BGR, as well as some other compensated BGRs in the references. From Table 1, a conclusion can be drawn that the proposed BGR improves the PSRR and the temperature stability significantly in a wider TR, with a better line regulation at a cost of small area and low power dissipation. Its active die area is 0.17×0.20 mm^2, which is only 1.18 times the conventional BGR (0.17×0.17 mm^2) in the same process. At the same time, the over-temperature protection circuit with thermal hysteresis function is introduced to improve the performance of the BGR effectively. The proposed BGR is a good performance compromise of temperature stability, TR, PSRR, size, power, process, etc.

6. Conclusion

A simple and efficient high-order curvature-compensated technique for BGR is studied. The proposed exponential curvature compensation technique has the advantages of superior temperature stability and no need for extra circuits to generate a curvature compensation voltage source over the conventional one. An over-temperature protection block with thermal hysteresis function has prevented thermal oscillation efficiently and improved the stability of the BGR. Based on the CSMC 0.5 μm 20 V BCD process the proposed BGR is implemented. With a temperature range from –40 to 150 ℃ the BGR achieves a TC of 13.7 ppm/K and a PSRR of –98.2 dB, as well as a line regulation of 0.3 mV/V with a supply voltage variation of 2.7–5 V. The whole power consumption is only 0.38 mW and the active die area is 0.17×0.20 mm^2. Simulation and experimental results indicate that the proposed BGR provides good temperature stability and high PSRR and low line regulation, especially effective thermal oscillation prevention, besides small size and low power consumption. The proposed BGR is suitable for on-chip voltage reference in high precision analog, digital and mixed systems.

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