A 12-bit current steering DAC with 2-dimensional gradient-error tolerant switching scheme*

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Abstract: A 12-bit intrinsic accuracy digital-to-analog converter integrated into standard digital 0.18 μm CMOS technology is proposed. It is based on a current steering segmented 6+6 architecture and requires no calibration. By dividing one most significant bit unary source into 16 elements located in 16 separated regions of the array, the linear gradient errors and quadratic errors can be averaged and eliminated effectively. A novel static performance testing method is proposed. The measured differential nonlinearity and integral nonlinearity are 0.42 and 0.39 least significant bit, respectively. For 12-bit resolution, the converter reaches an update rate of 100 MS/s. The chip operates from a single 1.8 V voltage supply, and the core die area is 0.28 mm^2.

Key words: current steering DAC; gradient error; switching scheme; static performance testing method
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1. Introduction

Fast and accurate digital-to-analog converters (DACs) are widely required in system-on-chip systems. Current steering DACs are based on an array of matched current cells. These are organized in unitary or binary weighted elements. The segmented architecture is most frequently used to combine high conversion rate and high resolution[1]. In this architecture the least significant bits steer binary weighted current sources, while the most significant bits are thermometer encoded and steer a unitary current source array.

DACs' static properties depend on the matching property of the current sources array[2, 3]. Due to systematic effects, the parameters of the transistors vary depending on their location in the current source array. A good switching sequence switches the sources so that the errors do not accumulate. Besides the well-known row-column switching scheme[4], some switching schemes are presented to limit linear and quadratic errors[1, 5−7]. However, the schemes above are not adapted for a 6-bit unitary current sources array.

Matching properties is also dependent on the overdrive of gate voltages. With the development of technology, it is difficult to achieve good matching, while the supply voltage drops. Most published works with good linearity are designed under high power supply, such as the DAC in Ref. [1], which works from a 2.7 V supply, and the overdrive voltage of a unitary source is 1 V, which is unacceptable under lower supply voltage.

In this paper, we propose a 12-bit current steering DAC operated from a single 1.8 V power supply with a new 2-dimensional gradient-error tolerant switching scheme. The DAC is implemented in a standard digital single-well, single-poly, six-metal 0.18 μm CMOS process. The measured differential nonlinearity (DNL) and integral nonlinearity (INL) are both below 0.5 LSB, and the measured SFDR is 73.3 dB at a 520 kHz output signal. The core area is 0.28 mm^2.

2. Reduction of systematic errors

For segmented DACs, the most significant bits (MSBs) are thermometer encoded and steer a unitary current sources array generally, and the static performance of a segmented DAC is strongly dependent on the linearity of the unitary array. Linearity can be achieved by overcoming all possible random and systematic errors[1]. To overcome random errors, a large area of unitary current source array is preferred. However, linear errors and symmetrical errors are generated, while random errors are limited. Besides well-known row-column switching schemes[4], some switching schemes are presented to limited linear and quadratic errors[1, 5−7]. The Q^2 random-walk scheme was introduced in Ref. [1] to achieve the first intrinsic accuracy 14-bit DAC in CMOS technology. Besides the Q^2 random-walk scheme, a gradient-error and edge-effect tolerant switching scheme is presented in Ref. [5]. These two schemes can reduce linear and quadratic errors effectively. But the switching sequences in Ref. [1] are only for an 8 bit unitary current sources array, and switching sequences in Ref. [5] are for 3-bit, 4-bit and an 8-bit unitary current sources array. An extended scheme is not mentioned in either paper. An INL bounded switching scheme[6] achieves optimal performance for a 1-dimensional array with linear gradients. However, if the current sources are not arranged in a 1-dimensional array or if errors are not caused by linear gradients, it is not optimal[7]. In this paper, a 2-dimensional switching scheme for current steering DACs is proposed. Compared with the above schemes, our scheme is adapted for a 6-bit unitary current sources array. It combines the advantages of the Q^2 scheme and gradient-error

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Table 1. Comparison with previously published switching schemes.

Normalized error distribution	Random walk[1]		Gradient-Tolerant[5]		Our scheme	
	DNL	INL	DNL	INL	DNL	INL
Linear	1	3.20	1	1.07	0.39	0.26
Quadratic	1	1.49	1	1.49	0.23	0.44
Joint (ratio = 1)	1	2.04	1	0.94	0.19	0.20

16	4	8	9	14	5	11	7	15	3	6	2	1	10	12	13
3	2	1	15	8	9	10	12	5	11	13	4	16	6	7	14
6	10	7	12	1	13	4	15	8	14	16	9	11	5	2	3
5	13	11	14	2	3	16	6	7	12	10	1	9	8	4	15
13	15	5	1	4	12	6	11	14	16	8	7	10	9	3	2
9	7	4	6	3	10	8	5	1	2	12	15	13	14	11	16
12	14	3	2	7	16	13	9	10	5	11	6	4	1	15	8
10	11	16	8	15	2	1	14	9	13	4	3	7	12	5	6
15	5	12	3	9	14	7	16	6	10	2	11	8	13	1	4
8	9	13	4	12	6	15	3	16	1	14	5	2	11	10	7
1	16	14	11	10	4	2	8	13	9	7	12	3	15	6	5
7	6	2	10	11	1	5	13	4	15	3	8	12	16	14	9
11	8	15	5	13	7	12	10	3	4	9	14	6	2	16	1
14	12	9	7	5	8	3	2	11	6	1	16	15	4	13	10
4	3	10	16	6	11	14	1	2	8	15	13	5	7	9	12
2	1	6	13	16	15	9	4	12	7	5	10	14	3	8	11

Fig. 1. Array A for 4-bit unitary decoding.

tolerant switching scheme, and achieves good linearity.

In Fig. 1, the basic scheme for 4-bit unitary decoding is shown. Every unitary source is divided into 16 elements in array A. Each unitary source has exactly one element in each row and in each column, while each has exactly one element in each 4×4 region, which is separated by bold lines. It is almost the same as that for the 4-bit unitary array mentioned in Ref. [5]. This scheme eliminates linear errors and quadratic errors effectively, and it reduces the impact of edge-effect[5].

For 6-bit unitary decoding, the unitary sources array contains 64×64 sources to ensure that each unitary source has one element in each row and in each column. The array has too many sources and is hard to construct. To make an analogical unitary sources array for 6-bit unitary decoding, a tradeoff is performed. Figure 2 shows our scheme for 6-bit unitary decoding. Every unitary source in array B is divided into 16 elements. Each unitary source has exactly one element in every two rows and in every two columns, while each has exactly one element in each 8×8 region. Array B is extended from array A. Each number in array A generates a 2×2 matrix in array B. The relationship between arrays A and B is

$$\begin{aligned} b(1,1) &= a, \\ b(1,2) &= a + 32, \\ b(2,1) &= a + 16, \\ b(2,2) &= a + 48, \end{aligned} \tag{1}$$

or

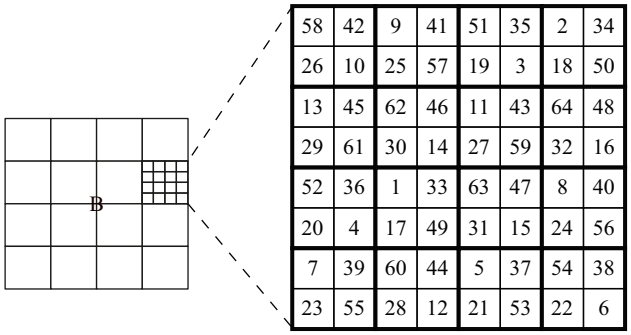

Fig. 2. Partial array B for 6-bit unitary decoding.

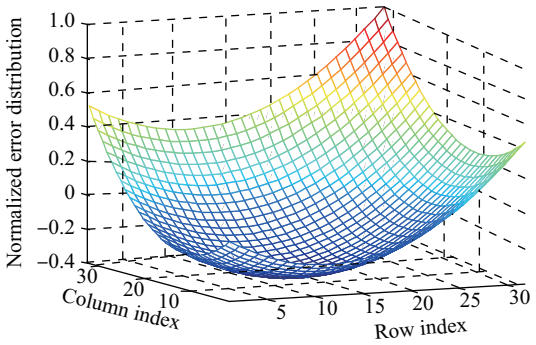

Fig. 3. Normalized gradient error distribution.

$$\begin{aligned} b(1,1) &= a + 48, \\ b(1,2) &= a + 32, \\ b(2,1) &= a + 16, \\ b(2,2) &= a, \end{aligned} \tag{2}$$

where a is a number in array A while b is a 2×2 matrix in array B generated by number a.

Using Eq. (1) only can generate an array which has one element in every two rows and in every two columns, whereas the gradient errors accumulate. Array B generated by Eq. (1) associated with Eq. (2) limits the error accumulating.

The normalized gradient error distribution is shown in Fig. 3. The ratio of linear errors to quadratic errors is 1. Figure 4 shows that array B generated by Eq. (1) associated with Eq. (2) is better than the array generated by Eq. (1) only. The former accumulates the gradient errors while the latter does not. The normalized DNL is 0.19, and the normalized INL is 0.20.

The simulation results of three switching schemes under the three error distribution conditions are summarized in Table 1, which shows that our scheme achieves the best linearity.

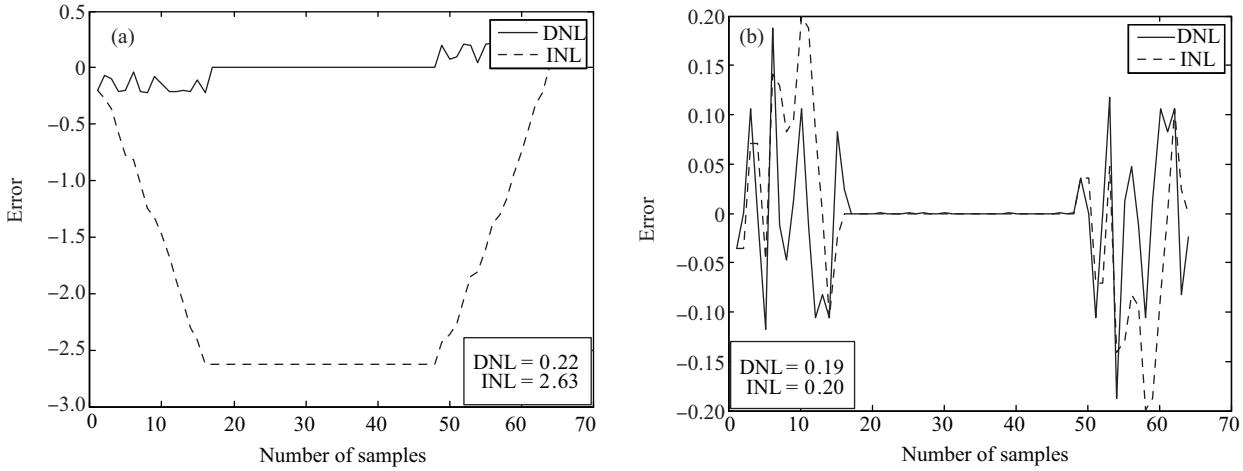

Fig. 4. (a) Array generated by Eq. (1) only. (b) Array B generated by Eq. (1) associated with Eq. (2).

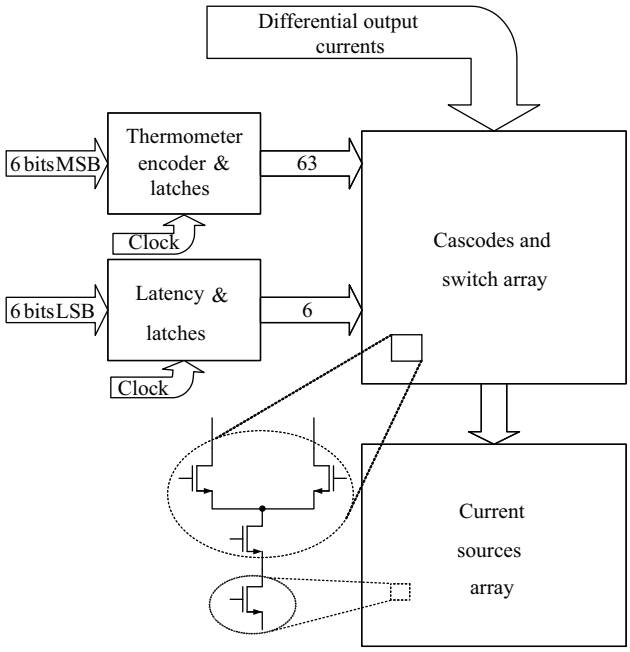

Fig. 5. Block diagram of 12-bit DAC.

3. DAC architecture and implementation

The block diagram of the presented 12-bit segmented architecture is depicted in Fig. 5. The six most significant bits (MSBs) are encoded from binary to thermometer code in the thermometer encoder, which steer the unitary weighted current sources. The six least significant bits (LSBs), which steer the binary weighted current source, are delayed by the latency block. Latches provide two complementary signals needed at the input of the current switches and shift their crossing point to avoid switching both transistors off. Latches are controlled by clock signal and ensure that the MSBs and LSBs steer the current sources array simultaneously.

It is well known that high output impedance is beneficial to the static and dynamic performance of the DAC[8]. The cascode transistors boost the output impedance and make the current sources less susceptible to the voltage of the output.

One of the key points to preserve a high update rate is to keep a simple and compact encoding logic. A fast row-column encoder of 6 bits is chosen. Part 1 and part 2 in Fig. 6 describe the scheme. The high 6 bits of digital input signals are divided into two parts, I_{1-3} and I_{4-6}. These two parts have 3 bits each and encode to row 7 bit thermometer codes a_m and column 7 bit thermometer codes b_n. The scheme for 3-bit binary-to-thermometer encoding is shown in Fig. 6(a). Row codes and column codes encode to final 63 bit thermometer codes T_{1-63} for 6 bit digital input. The encoding formula can be described as

$$T_{8n+m} = a_m b_n + b_{n+1}, \tag{3}$$

assuming b_0 equal "1" and b_8 equal "0". Figure 6(b) shows the encoding circuits.

The encoding circuits are followed latches constituted by D-triggers and some logic circuits. The circuits and their function are shown in Fig. 6(c). The purpose of the circuits is to synchronize all DAC cells, make each thermometer code a differential couple and simultaneously improve their crossing point. Improving the crossing point ensures that the two switching transistors are never switched off simultaneously. If the switching transistors switch off simultaneously, the unitary current source would cut off and the voltages of two outputs would both be lowered. The asymmetry gives rise to a glitch at the DAC outputs and has a passive impact on the dynamic characteristics of the DAC.

Besides switching signals, the clock signal is critical to the dynamic characteristics too. The clock driver depicted in Fig. 6(d) works as a clock buffer. It works when the input signal is a differential couple of sine or clock signal whose V_{pp} is above 0.8 V. It drives the followed clock tree, which reduces the delay differences on the clock net.

4. Measurement results

The 12-bit current steering DAC has been implemented in a standard digital single-well, single-poly, six-metal 0.18 μm CMOS process. The microphotograph of the chip is shown in Fig. 7. The core area is 0.28 mm^2.

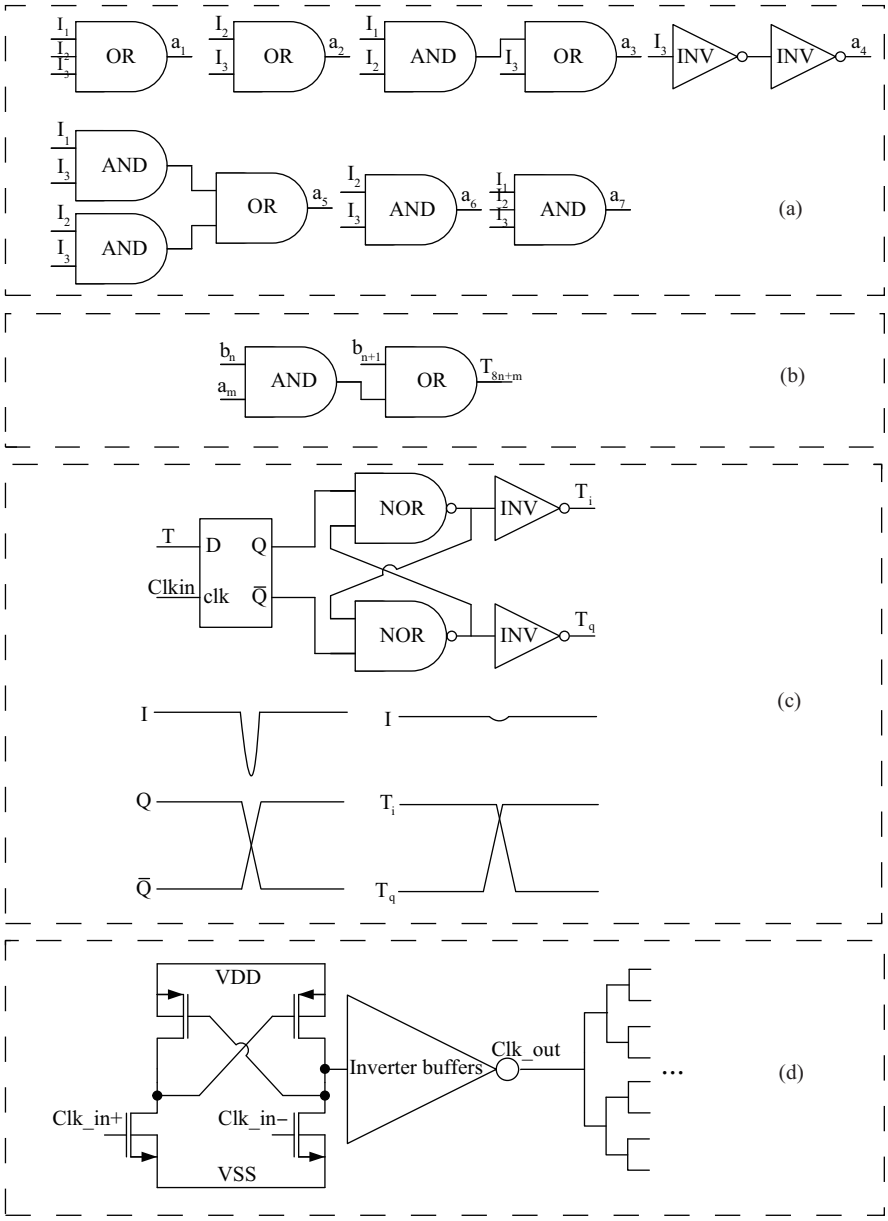

Fig. 6. (a) Scheme for 3-bit binary-to-thermometer encoding. (b) Encoder, (c) latch and (d) clock driver circuits.

A novel testing method is adopted to test the static performance of the DAC. To test the DNL and INL, all the output step sizes must be measured. Generally speaking, to measure one certain step size, its low voltage level and high voltage level are measured by a high resolution voltage meter. Most testing facilities have large low frequency noise, especially at DC, but have good accuracy at high frequency. In our scheme, all the output step sizes are measured at relatively high frequency by a spectrum analyzer.

If the input is a periodically alternate signal, based on the Fourier series, the output is constituted of a series of cosine signals. It can be expressed as

$$f(t) = a_0 + \sum_{n=1}^{\infty} \frac{2E}{n\pi} \sin\frac{n\pi}{2} \cos\frac{nt}{T}, \tag{4}$$

where a_0 is the DC offset, E is the $V_{\rm pp}$ and T is the period of the signal. Its waveform and spectrum are depicted in Fig. 8. During the testing, for example, the input signal is a periodically alternate series of "000000000000" and "000000000001", and the frequency is 1 MHz. Because 1 MHz is quite a low frequency to the DAC, the output signal can be treated as an ideal periodically alternate signal. According to Eq. (4), the output comprises a series of cosine signals. Their maximal amplitude is $2E/\pi$ at 1 MHz, proportional to E obviously. Measuring the amplitude at 1 MHz with a spectrum analyzer, the output step size between "000000000000" and "000000000001" (E) can be deduced. Other step sizes can be deduced similarly.

The measured static properties are shown in Fig. 9(a), where DNL and INL are both smaller than 0.5 LSB. Figure 9(b) shows the dynamic characteristic of the converter versus input frequency when the clock is 100 MHz. The total current dissipation is 12 mA, and the current source arrays consume 10 mA to achieve an output range of 1 $V_{\rm pp}$ on a load resistance of 50 Ω, while bias and digital parts consume another 2 mA.

The comparison of this work with other reported low area-

Table 2. Comparison with reported works.

Parameter	This work	Ref. [10]	Ref. [11]	Ref. [12]
Process	0.18 μm CMOS	0.25 μm CMOS	0.13 μm CMOS	0.13 μm CMOS
Resolution (bits)	12	12	12	12
Power supply (V)	1.8	3.3 and 2.5	3.3	3.3
Load resistor (Ω)	50	50	—	37.5
Output range (V_{pp})	1	—	—	2
DNL (LSB)	0.42	—	1	1
INL (LSB)	0.39	—	3	3
Clock (MHz)	100	150	300	300
SFDR (dB)	73.3 @ 520 kHz	70 @ 27.2 MHz	75 @ 1 MHz	70 @ 1 MHz
Current dissipation (mA)	12	2–20	50 mW/3.3 V	100 mW/3.3 V
Core area (mm^2)	0.28	0.48	0.26	0.26

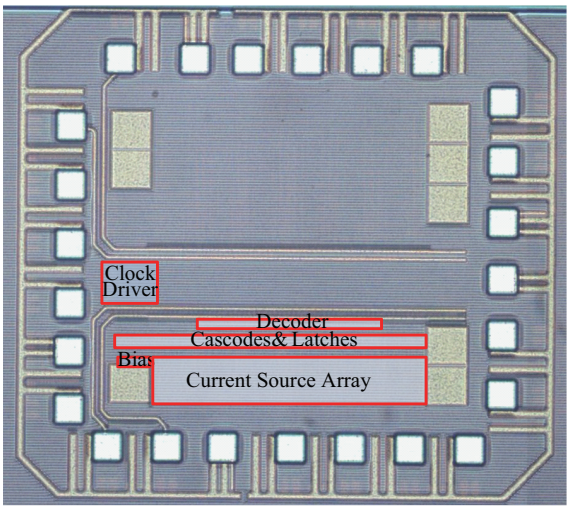

Fig. 7. Microphotograph of the chip.

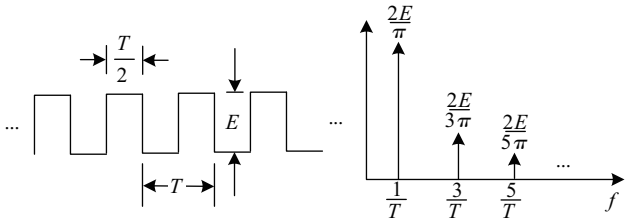

Fig. 8. Periodically alternate signal and its spectrum.

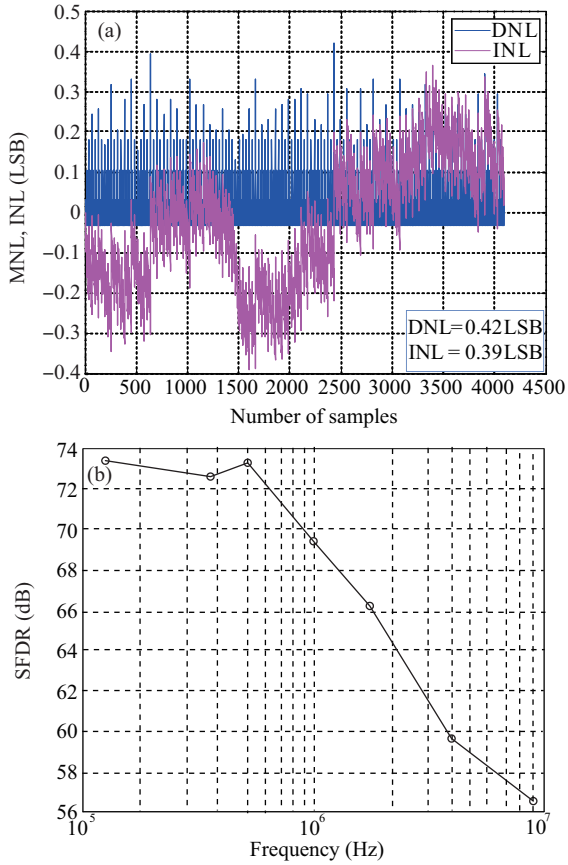

Fig. 9. Measured (a) DNL, INL and (b) SFDR when the clock is 100 MHz.

cost works is shown in Table 2. From Table 2, the presented DAC exhibits excellent DNL and INL.

Compared with Ref. [10], which achieved good performance at very high signal frequencies, the SFDR drops quickly at high frequency in this work. One of the main reasons for this is that the output impedance is not high enough at high frequency. Reference [10] gives the expression of SFDR:

$$\mathrm{SFDR} = \frac{4g_{\mathrm{L}} + 2Ng_0}{Ng_0}, \tag{5}$$

where N is the number of unit current sources, and g_{L} and g_0 are the transconductance of the load resistor and the unit current source, respectively. Based on Eq. (5), SFDR deteriorates as g_0 goes up. The sizable transistor has a large parasitic capacitor which increases g_0 as the frequency goes up. Therefore, high frequency performance suffers. Another reason is that the printed circuit board (PCB) used in the chip test is not reliable at high frequency. To solve these problems, future work is to be done. Firstly, the output impedance can be boosted by active cascode. And some good schemes, such as the one proposed in Ref. [9], can be used to obtain good harmonic performance at high frequency. On the other hand, the test-on-chip technique can be adopted to cancel the interference from PCB during testing.

5. Conclusions

A 12-bit current steering digital-to-analog converter with a new switching scheme has been proposed. This scheme elim-

inates both linear and quadratic gradient errors. The effectiveness of the scheme has been verified by applying it to the measured error profile of a 12-bit DAC. The measured DNL and INL are 0.42 LSB and 0.39 LSB, respectively, and the measured SFDR is 73.3 dB at a 520 kHz output signal when the frequency of the clock is 100 MHz. 12-bit linearity is achieved in a core area of 0.28 mm^2, and it operates from a single 1.8 V power supply.

References

[1] Van der Plas G, Vandenbussche J, Sansen W, et al. A 14-bit intrinsic accuracy Q^2 random walk CMOS DAC. IEEE J Solid-State Circuits, 1999, 34: 1708

[2] Pelgrom M J M, Duinmaijer A C J, Welbers A P G. Matching properties of MOS transistors. IEEE J Solid-State Circuits, 1989, 24: 1433

[3] Lakshmikumar K R, Hadaway R A, Copeland M A. Characterization and modeling of mismatch in MOS transistors for precision analog design. IEEE J Solid-State Circuits, 1986, SC-21: 1057

[4] Lin C H, Bult K. A 10 bit, 500 MSample/s DAC in 0.6 mm^2. IEEE J Solid-State Circuits, 1998, 33: 1948

[5] Deveugele J, van der Plas G, Steyaert M, et al. A gradient-error and edge-effect tolerant switching scheme for a high-accuracy DAC. IEEE Trans Circuits Syst I, 2004, 51(1): 191

[6] Cong Y, Geiger R L. Switching sequence optimization for gradient error compensation in thermometer-decoded DAC arrays. IEEE Trans Circuits Syst II, 2000, 47(7): 585

[7] Yu Z, Chen D, Geiger R. 1-D and 2-D switching strategies achieving near optimal INL for thermometer-coded current steering DACs. Proc IEEE ISCAS, May 2003: 909

[8] Luschas S, Lee H S. Output impedance requirements for DACs. Proc IEEE ISCAS, May 2003, 1: I-861

[9] Lin C H, van der Goes F, Westra J, et al. A 12 b 2.9 GS/s DAC with IM3 < –60 dBc beyond 1 GHz in 65 nm CMOS. ISSCC Dig Tech Paper, Feb 2009: 74

[10] Zhong S, Tan N. A 12-bit 150-Msamples/s current-steering DAC. Proc IEEE Asia Pacific Conference on Circuits & Systems, Macao, China, Dec 2008

[11] Lee B, Kim B, Lee J, et al. A small chip area 12-b 300 MS/s current steering CMOS D/A converter based on a laminated-step layout technique. 18th European Conference on Circuit Theory and Design, Aug 2008: 882

[12] Moon J, Song M, Shin S, et al. Design of a laminated current cell relocation 12-bit CMOS D/A converter with a high output impedance technique and a merged switching logic. Analog Integrated Circuits and Signal Processing, 2010, 63(3): 407