A 10-bit 200-kS/s SAR ADC IP core for a touch screen SoC*

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Abstract: Based on a 5 MSBs (most-significant-bits)-plus-5 LSBs (least-significant-bits) C–R hybrid D/A conversion and low-offset pseudo-differential comparison approach, with capacitor array axially symmetric layout topology and resistor string low gradient mismatch placement method, an 8-channel 10-bit 200-kS/s SAR ADC (successive-approximation-register analog-to-digital converter) IP core for a touch screen SoC (system-on-chip) is implemented in a 0.18 μm 1P5M CMOS logic process. Design considerations for the touch screen SAR ADC are included. With a 1.8 V power supply, the DNL (differential non-linearity) and INL (integral non-linearity) of this converter are measured to be about 0.32 LSB and 0.81 LSB respectively. With an input frequency of 91 kHz at 200-kS/s sampling rate, the spurious-free dynamic range and effective-number-of-bits are measured to be 63.2 dB and 9.15 bits respectively, and the power is about 136 μW. This converter occupies an area of about 0.08 mm^2. The design results show that it is very suitable for touch screen SoC applications.

Key words: analog-to-digital converter; SAR; touch screen SoC; CMOS integrated circuits; low power
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1. Introduction

As human-machine interfaces, touch screens are widely used in many applications, such as PDAs (personal digital assistants), mobile phones, portable instruments, and remote control systems. In a touch screen SoC (system-on-chip), the TSC (touch screen controller) is a crucial block. It is used to detect the pressure on the touch panel, measure the touch coordinates and communicate with the processor. During the coordinates' measurement, not very high speed but low power and accurate A/D conversion is necessary. Due to its inherent simple architecture, small area, low power and easiness to be integrated with other IC blocks, the SAR A/D converter is very popular for the TSC application[1−4].

Though many touch screen products have been produced by many corporations such as TI, ADI, and ATLab, there are very few papers that describe the touch screen SAR A/D converters. In Ref. [1], a 9.05-bit 0.25 mm^2 touch screen SAR ADC (successive-approximation-register analog-to-digital converter) with 1.4 LSB (least-significant-bit) INL (integral non-linearity) is realized based on a 0.18 μm CMOS process. Reference [2] describes the low-power, high speed and high resolution approaches for SAR ADC design and presents an R–C combination based SAR A/D converter that can be utilized in TSC applications. But in the two previous works, the touch screen system and consideration of TSC SAR ADC design is not mentioned, and the performance of the converter in Ref. [1] needs to be further improved. With the design technique and technology improvement, more functions and module blocks can be integrated together. Then, as touch screen SoCs' fundamental building blocks, SAR A/D converters face challenges to realize low power and high performance with even smaller areas. Therefore, further research in this field is still very necessary. In this paper, the typical principle and important design consideration of the TSC are included and a low power 10-bit SAR A/D converter IP core is realized for a touch screen SoC based on the SMIC 0.18 μm CMOS logic process. Comparison with some previous works shows that the proposed converter features a high performance and is very suitable for the touch screen SoC application.

2. Description of the touch screen system

Figure 1 shows the function diagram of a typical touch screen system. The touch panel is used to sense the touch on the panel and send the touch information to the TSC. When the TSC recognizes the touch information, it determines the touch point location in two coordinate directions and sends them to the processor through the bus. After getting the information sent from the TSC, the processor does its operation properly and sends out commands to control the TSC's next operation.

The SAR A/D converter is the main circuit block of the TSC. It is used to digitize the analog signals from the touch panel. Touch screen SoCs have no stringent requirement on the sampling rate of the embedded SAR A/D converter because the touch on the panel is always not with high frequency. But low power, small area and high resolution are always necessary for touch screen SoC applications[2]. To satisfy this requirement, a 10-bit low power, small area 200-kS/s SAR ADC based on 0.18 μm CMOS is realized in the following sections.

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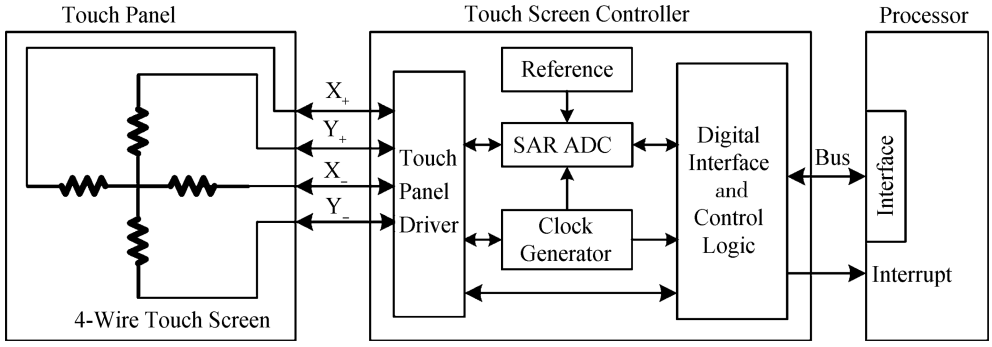

Fig. 1. Function diagram of the touch screen system.

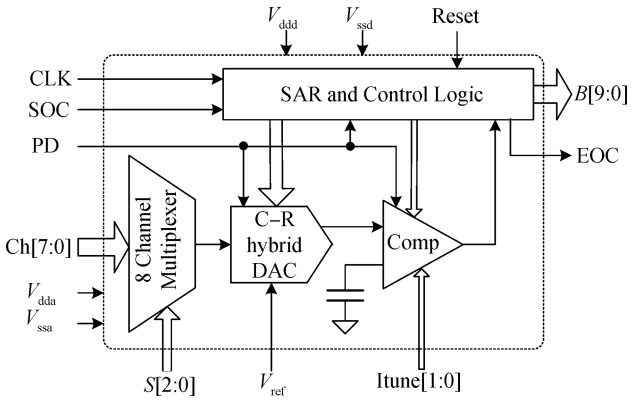

Fig. 2. Function diagram of the proposed 10-bit SAR ADC.

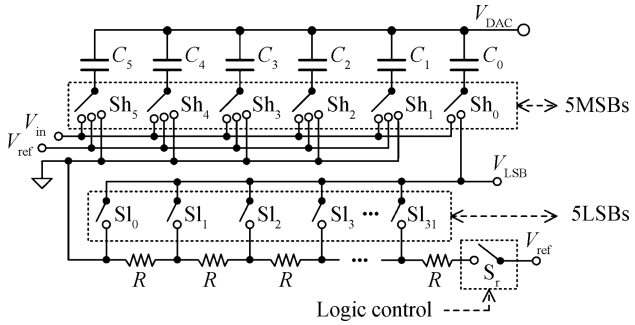

Fig. 3. Internal D/A conversion network of the 10-bit SAR ADC.

3. Design of the SAR A/D converter

Figure 2 shows a function diagram of the 8-channel 10-bit SAR A/D converter proposed in this paper. This converter is mainly composed of an 8-channel multiplexer, a C–R hybrid D/A conversion network, a pseudo-differential comparator and the SAR control logic circuit. In Fig. 2, $V_{\rm dda}$ represents the 1.8 V analog supply while $V_{\rm ddd}$ is the 1.8 V digital supply. CLK is the clock of this converter and SOC (start of conversion) represents the signal that controls sampling. Ch[7:0] is the eight input channels which are controlled by the selecting signal S[2:0]. $V_{\rm ref}$ represents the voltage reference of the converter. Itune[1:0] is used to control the bias current provided for the comparator. EOC is used for ending the conversion and B[9:0] is the 10-bit digital output. When the Reset signal is 1, the digital output B[9:0] is reset to all zeros 000…0. PD is the power down signal which has a normal state of 0, and when it is set to 1, the converter should stop its operation and consume no power.

The operation of the SAR A/D converter is based on a "binary search" algorithm. Under the control of the channel selection signal S[2:0], one of the eight input signals is selected by the "8 channel multiplexer" as the SAR ADC input. The input signal is sampled by the C–R hybrid D/A conversion network which has an inherent sample and hold function. Then, the sampled signal is compared with the output of the D/A converter sequentially under the control of the SAR logic circuit. The reference voltage produced by the D/A converter at a particular stage can be calculated with the formula: $B_{N-1}V_{\rm ref}/2^1 + B_{N-2}V_{\rm ref}/2^2 + B_{N-3}V_{\rm ref}/2^3 + \cdots + B_kV_{\rm ref}/2^{N-k}$, where N is the resolution of the converter and $0 \leqslant k \leqslant N-1$. During the decision of B_k, $B_k = 1$ is assumed initially, then the reference voltage produced by the D/A converter will be $B_{N-1}V_{\rm ref}/2^1 + B_{N-2}V_{\rm ref}/2^2 + \cdots + 1\times V_{\rm ref}/2^{N-k}$. This value is compared with the sampled input signal. If the result of the comparator shows that this reference voltage is smaller than the sampled input signal, $B_{\rm k} = 1$ is true; otherwise, B_k should be 0. With this method, B_{N-1}–B_0 can be generated sequentially.

3.1. Low power D/A conversion network

In this SAR A/D converter, a 5 MSBs + 5 LSBs C–R hybrid D/A conversion network is utilized, as shown in Fig. 3. The 5 MSBs are realized by a capacitor array while the 5 LSBs are realized by a resistor string. Due to the inherent sample and hold function of the capacitor array, no additional S/H circuit is needed. Compared with traditional charge redistribution and voltage division structures, this approach makes it easier to realize small area, high resolution and low power simultaneously, which is more significant in embedded SoC applications.

In Fig. 3, $C_5 = 2C_4 = 4C_3 = 8C_2 = 16C_1$, $C_1 = C_0$. In the sampling step, $V_{\rm in}$ is sampled by capacitors C_0–C_5 with switches $\rm Sh_0$–$\rm Sh_5$ connected to $V_{\rm in}$. During the conversion step, capacitor C_0 is connected to ground by $\rm Sh_0$ and $\rm Sl_0$, and capacitors C_1–C_5 are switched to $V_{\rm ref}$ or ground with the control of the SAR logic circuit. Then, B_9–B_5 can be generated. After B_9–B_5 are generated, the resistor string is used to generate B_4–B_0 with the switches $\rm Sl_0$–$\rm Sl_{31}$ controlled by the SAR logic circuit. Then, with the approximation principle of the SAR A/D converter, at the end of the conversion step, we have: $V_{\rm in}2^5C_0 = V_{\rm ref}(B_{10-1}2^{5-1}C_0 + B_{10-2}2^{5-2}C_0 + \cdots + B_{10-5}C_0) + V_{\rm LSB}C_0$. With the substitution of $V_{\rm LSB}$ =

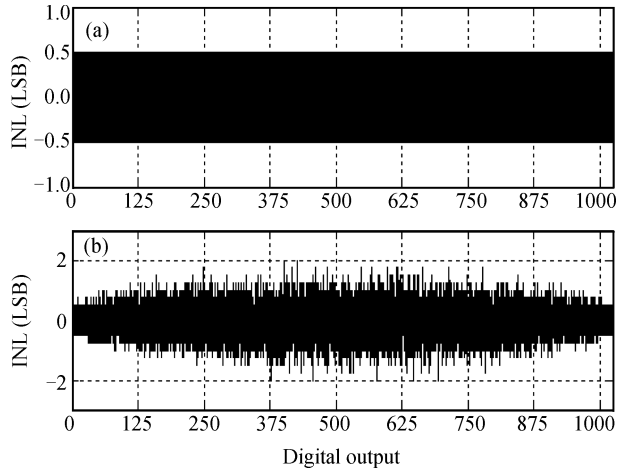

Fig. 4. Capacitor's mismatch. (a) $\sigma_c/C_0 = 2^{-7.5}$ (b) $\sigma_c/C_0 = 2^{-8.5}$.

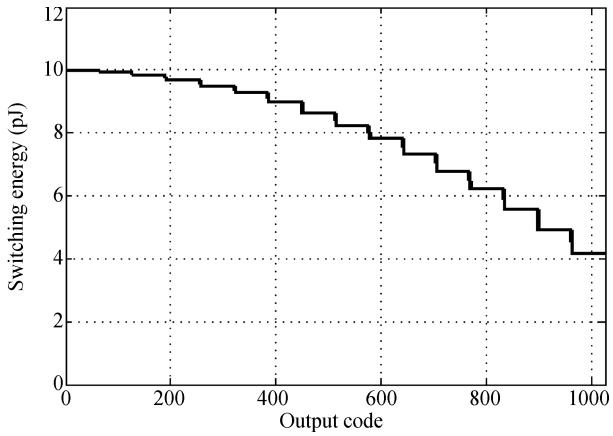

Fig. 5. Switching energy of the capacitor array.

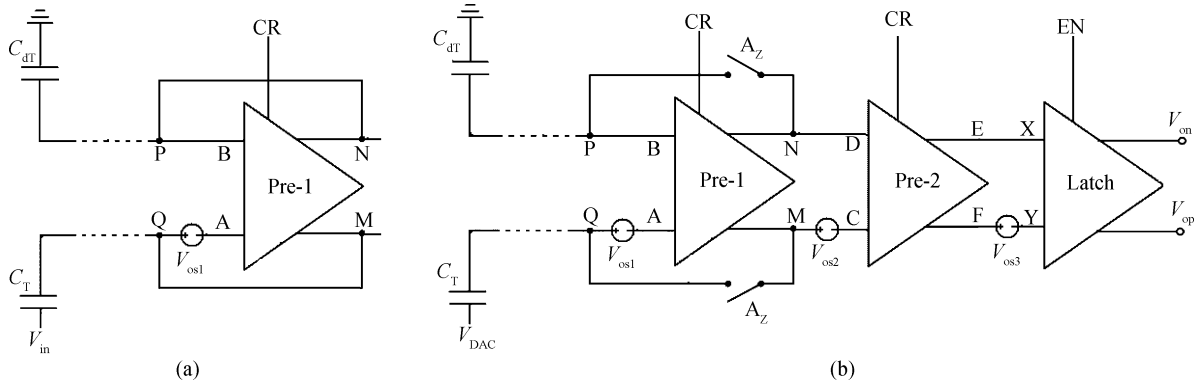

Fig. 6. SAR ADC comparator. (a) Sampling phase. (b) Approximation phase.

V_{ref} ($B_{5-1}2^{-1} + B_{5-2}2^{-2} + \cdots + B_1 2^{-(5-1)} + B_0 2^{-5}$), we can approximate V_{in} as below:

$$V_{in} = V_{ref}\left(\sum_{i=1}^{5} B_{10-i} \times 2^{-i} + \sum_{i=5+1}^{5+5} B_{10-i} \times 2^{-i}\right) = V_{ref}\sum_{i=1}^{10} B_{10-i} \times 2^{-i}. \quad (1)$$

The power dissipation of the 5MSBs' capacitor array is optimized through modeling by Matlab. Under the consideration of the passive components' matching performance, the smallest capacitors as possible are selected. With the analysis approach proposed in Ref. [5] and assuming that capacitor values are normally distributed with mean C_0 and standard deviation σ_c, then if a 5-bit capacitor array is used to generate the 5 MSBs of a 10-bit ADC, σ_c/C_0 should be no more than $2^{(5-1)/2-10}$. Based on this discussion, the conditions of $\sigma_c/C_0 = 2^{-7.5}$ and $\sigma_c/C_0 = 2^{-8.5}$ are both verified by Matlab models. Figure 4 shows the verification results which can prove that σ_c/C_0 should be less than 2^{-8}. By using almost the smallest 120 fF metal finger capacitor as the unit capacitor to satisfy the matching requirement described above, the energy dissipation of the capacitor array is shown in Fig. 5.

For 200 kS/s sampling rate, the conversion period is 5 μs. Thus, the maximum power dissipation of the capacitor array is only about 2 μW. It appears at the smallest output code, where only down transitions happen[2]. Except for the low power capacitor array, another highlight is that the resistor string is in the power down state during sampling and generating the 5 MSBs. Then, more than half of the reference power is saved. This is realized by switch S_r controlled by the control logic circuit, as shown in Fig. 3. Also, the low sampling rate of the SAR A/D converter makes it possible to choose large resistors for further reducing the reference power.

3.2. Pseudo-differential comparator

In this paper, the comparator is realized with two cascaded preamplifier stages followed by a latch stage as shown in Fig. 6. The negative port of the comparator is connected to the D/A converter while the positive port is connected to a dummy capacitor array. With this pseudo-differential architecture, the errors caused by clock feed-through and charge injection can be considered as common-mode interferences, so the performance is improved. This comparator is combined with the SAR ADC sample-and-hold function. By using the first stage preamplifier offset cancellation, the total equivalent input offset is reduced, which is of significance because the comparator offset affects the ADC offset directly[6].

In Fig. 6, the total capacitance of the 5-bit capacitor array C_T equals $32C_0$. The capacitance C_{dT} is used for reducing the input offset cased by the charge injection and clock feedthrough of switches A_z. In the sampling mode, the comparator is auto-zeroed with A_z turned on. The input signal V_{in} is

sampled by C_T. $V_P = V_Q = V_{CM}$, where V_{CM} represents the common mode voltage. By the end of the sampling mode, with A_z turned off, the input signal information has been held at the positive port as a charge form. In the comparison mode, based on the comparator output, the output of the D/A converter is controlled by the digital logic to approximate the sampled input successively.

In the sampling phase shown in Fig. 6(a), we can get: $-A_1(V_B - V_A) = V_N - V_M = V_P - V_Q$. Here, A_1 represents the gain of the first preamplifier. With $V_B = V_P = V_{CM}$ and $V_A = V_Q - V_{OS1}$, we can get: $-A_1(V_P - V_Q + V_{OS1}) = V_P - V_Q$. After rearrangement, we have:

$$V_Q = V_P + \frac{A_1 V_{OS1}}{A_1 + 1} = V_{CM} + \frac{A_1 V_{OS1}}{A_1 + 1}. \quad (2)$$

By the end of the approximation phase, V_X should be equal to V_Y. Taking the offset of the second stage preamplifier V_{os2} and the latch offset V_{os3} into consideration, at the nodes P and Q we have $V'_P = V_{CM}$ and:

$$V'_Q = V_{CM} + V_{OS1} + \frac{V_{OS2}}{A_1} + \frac{V_{OS3}}{A_1 A_2}. \quad (3)$$

Based on the charge conservation at node Q in the sampling and approximation phase, we have:

$$(V_Q - V_{in})C_T = (V'_Q - V_{DAC})C_T. \quad (4)$$

With the substitution of Eqs. (2) and (3) into Eq. (4), we can get $V_{in} = V_{DAC} - V_{os}$, where the total equivalent input offset of the comparator V_{os} can be calculated as below:

$$V_{OS} = \frac{V_{OS1}}{A_1 + 1} + \frac{V_{OS2}}{A_1} + \frac{V_{OS3}}{A_1 A_2}. \quad (5)$$

It is obvious from Eq. (5) that the offset of the first stage preamplifier is divided by $A_1 + 1$, and the equivalent input offset of the comparator is dramatically reduced. This advantage is compatible with the operation of the SAR ADC and is achieved without any additional circuit complexity.

The comparator in this design is composed of two preamplifiers with cross-coupled positive feedback[7] and a low power regenerative dynamic latch[8]. Attention must be paid that the tail current of the preamplifiers is a critical design variable for the comparator. Noise, speed and power consumption of the preamplifier are all related to the current. It is important to find an optimal compromise between a small bias current for low power dissipation and a large value to minimize noise and maximize the comparison rate. With the consideration above, the current of the comparator is made to be adjustable under the control of Itune[1:0] shown in Fig. 2.

4. Design results and discussion

This SAR A/D converter is realized based on SMIC 0.18 μm 1P5M CMOS logic process. Figure 7 shows the layout photograph of the ADC. To improve the technology compatibility, metal finger capacitors are adopted to form the capacitor array. With the consideration of the matching performance and the power dissipation of the resistor string, P^+ doped polysilicon resistors are utilized. To achieve a good performance, the resistor string is sided by dummies to maintain the same

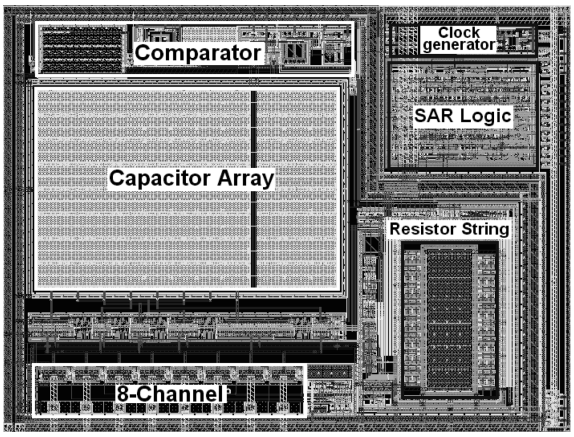

Fig. 7. Layout photograph of the converter.

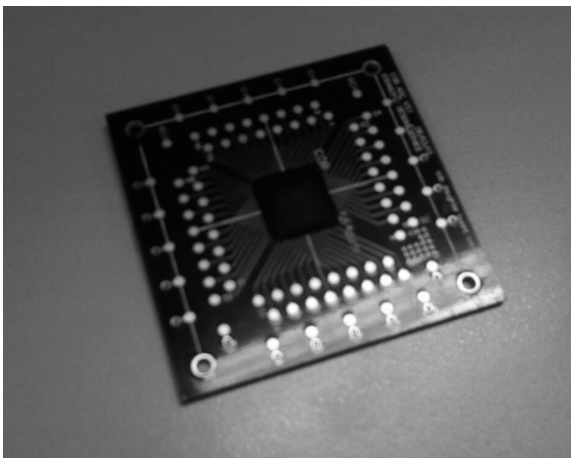

Fig. 8. Photograph of the SAR ADC testing chip.

environment on both sides, and the capacitor array is routed with an axially symmetric layout topology to reduce the mismatch. Dummy capacitors are also placed on the perimeter of the capacitor array. Since not too many capacitors are used in the design, the wiring complexity caused by the axially symmetric method can be acceptable. The active area of this SAR A/D converter IP core is 333×250 μm^2.

Figure 8 shows the 10-bit SAR ADC test chip, which is packaged in a 64-pin COB (chip-on-board) type. The DC characteristics of this converter are measured with the histogram testing method[9]. With a 1.8 V power supply and about 57.2 kHz input, the DNL and INL of this converter are measured to be about 0.32 LSB and 0.81 LSB respectively. During the AC performance measurement, the non-coherent sampling method is utilized. Before DFT, the windowing technique is used to avoid spectral leakage. Figure 9 shows an 8000 point DFT spectrum for a 91 kHz single-ended sinusoidal input signal sampled at 200 kS/s. The ENOB is 9.15 bits. The SFDR and THD are measured to be 63.2 dB and 62.7 dB respectively. Figure 10 gives the variation of the SNDR and SFDR with the input frequency. The SNDR is above 56 dB within the Nyquist input frequency band. Including the output drivers, the power dissipation of this converter is just 136 μW.

To evaluate the performance of the proposed 10-bit SAR A/D converter, a comparison with some previous works is

Table 1. Comparison with some previous works.

Reference	Process	Resolution	Sampling rate (MS/s)	Power (mW)	Area (mm^2)	ENOB	FOM (pJ/conv. step)
Ref. [1]	0.18 μm CMOS	10	2	3.1	0.25	9.05	2.92
Ref. [3]	0.35 μm CMOS	10	2	3	0.4	8	5.86
Ref. [4]	—	12	0.125	0.750	—	11	2.93
Proposed	0.18 μm CMOS	10	0.2	0.136	0.08	9.15	< 1.2

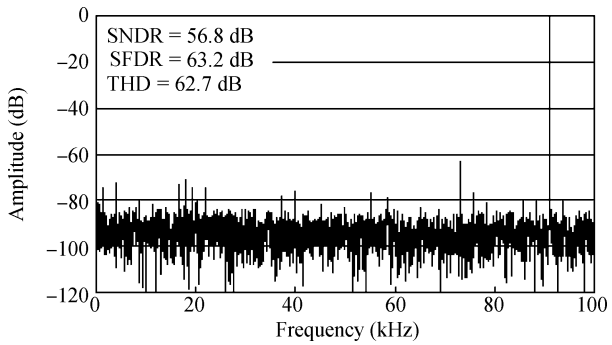

Fig. 9. 8000 point DFT @ 200 kS/s with 91 kHz input.

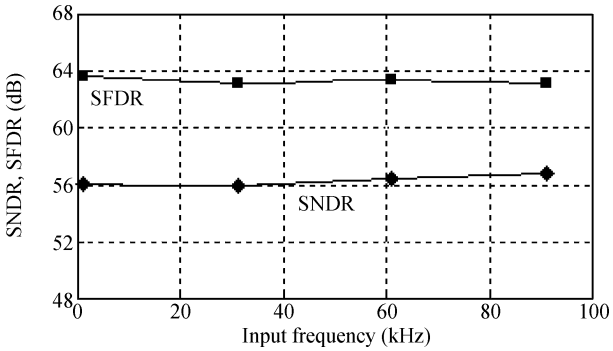

Fig. 10. SNDR and SFDR versus input frequency.

shown in Table 1. In the comparison, the FOM (figure-of-merit) = $P_{\rm diss}/(2^{\rm ENOB} \times f_{\rm sample})$ is used. $P_{\rm diss}$ is the power dissipation of the converter, and the ENOB is measured at the sampling rate of $f_{\rm sample}$.

From Table 1, the SAR A/D converter proposed in this paper is characterized by its small area, low power and relatively high signal-to-noise-and-distortion ratio, and also features a better FOM than ADS7843 (Ref. [4]) from Texas Instruments. From the comparison above, this proposed SAR ADC has the best FOM of the four. Low power and high resolution A/D conversion is realized within a small area, which is of more significance for applications such as portable systems and touch screen SoCs.

5. Conclusion

Based on 0.18 μm 1P5M CMOS logic process, by using 5 MSBs-plus-5 LSBs C–R hybrid DAC circuit, low-offset pseudo-differential comparator, resistor string low-mismatch placement and capacitor array axially symmetric layout method, an 8-channel 10-bit 200-kS/s SAR ADC IP core is realized for touch screen systems. With 1.8 V power supply, the DNL and INL are measured to be 0.32 LSB and 0.81 LSB respectively. Including the output drivers, the power dissipation of this converter is just measured to be just 136 μW. The total area of this SAR ADC IP core is just 0.08 mm^2. The measurement results show that this converter achieves high performance and can satisfy the touch screen SoC requirements. With the rapid improvement of SoC technology, much more unit IC blocks can be integrated on a chip. Low power, high resolution and small area unit circuits for SoC applications are more significant than before, and the high performance SAR A/D converter realized in this paper is important for the embedded IP core.

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