A low-power and low-phase-noise LC digitally controlled oscillator featuring a novel capacitor bank

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Abstract: A monolithic low-power and low-phase-noise digitally controlled oscillator (DCO) based on a symmetric spiral inductor with center-tap and novel capacitor bank was implemented in a 0.18 μm CMOS process with six metal layers. A third new way to change capacitance is proposed and implemented in this work. Results show that the phase noise at 1 MHz offset frequency is below –122.5 dBc/Hz while drawing a current of only 4.8 mA from a 1.8 V supply. Also, the DCO can work at low supply voltage conditions with a 1.6 V power supply and 4.1 mA supply current for the DCO's core circuit, achieving a phase-noise of –121.5 dBc/Hz at offset of 1 MHz. It demonstrates that the supply pushing of DCO is less than 10 MHz/V.

Key words: digitally controlled oscillator; DCO; IC-tank; IC oscillator
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1. Introduction

The ever increasing demand for communication systems to reduce their cost and power consumption gives the reason for the explosive growth in the global wireless access device market. A great variety of cordless mobile devices is developing quickly throughout the world. Current generation transceivers usually feature low-level integration and relatively high cost. The demand for low cost and low power favors the implementation of high-level integrated and digitally intensive transceivers[1].

A digitally controlled oscillator (DCO), which was proposed for wireless applications recently[2−4], generates a signal whose frequency can be directly controlled by its digital tuning words. It is regarded as one of the most critical blocks in all-digital phase-locked loops (ADPLL)[5]. Compared with a traditional VCO (voltage controlled oscillator), the DCO is much less sensitive to voltage headroom reduction as well as substrate and power line noise coupling. Therefore, it is considered to be a more advisable and appropriate selection for integrated RF transceivers than a traditional LC VCO or a ring oscillator-based DCO.

This paper gives the idea of a novel third way to change capacitance, describes the DCO design, and presents the experimental results.

2. A new way to change capacitance: serial-parallel topology transformer

Up to now, basically, there are only two types of way to change capacitance. The first type is carried out by changing the voltage of a voltage-controlled capacitor; while the second type is by controlling a capacitor whether or not active in an oscillator resonant loop. A third way to change capacitance (Fig. 1) is proposed and implemented in this test chip. This is composed of three capacitors and two switches. When the two switches are turned off, the three capacitors work in serial. While the two switches are turned on, the three capacitors work in parallel. Assuming the three capacitors have the same value C when in serial state, an equivalent capacitance $C/3$ is achieved (Fig. 1(b)); while in parallel state, a total capacitance of $3C$ is achieved (Fig. 1(c)).

3. LC digitally controlled oscillator (DCO)

The function of the DCO is to generate a clock signal whose frequency is proportional to the digital code. A DCO is very similar to a voltage controlled oscillator except that the DCO frequency is tuned digitally while the VCO's frequency is tuned by an analog signal. In this work, a LC-tank based oscillator is used together with a digitally tuned capacitor as the tuning unit, as illustrated in Fig. 2. The analog part of this DCO is a capacitance-controlled oscillator (CCO), which can be the same as that of a VCO.

A schematic of the DCO is shown in Fig. 2, in which the LC tank consists of a metal inductor and the capacitance tuning block. A cross-couples PMOS/NMOS pair forms a negative resistor to inject energy to the LC tank to compensate the LC tank's energy loss.

In order to meet the specifications under the given power consumptions, the cross coupled DCO with a current source is usually used in the CMOS IC design. This topology has an advantage in that it has a symmetric waveform, which leads to reduction of $1/f$ noise upconversion[6], and it has less oscillation frequency variation caused by supply voltage since it utilizes a current source.

The transconductance (g_{m}) of the above topology is determined by the current consumption and the geometry of the devices. Since this topology reduces the voltage headroom due to the presence of a current source, the devices need to be large to get enough g_{m} to start an oscillation. NP-DCO, NMOS and

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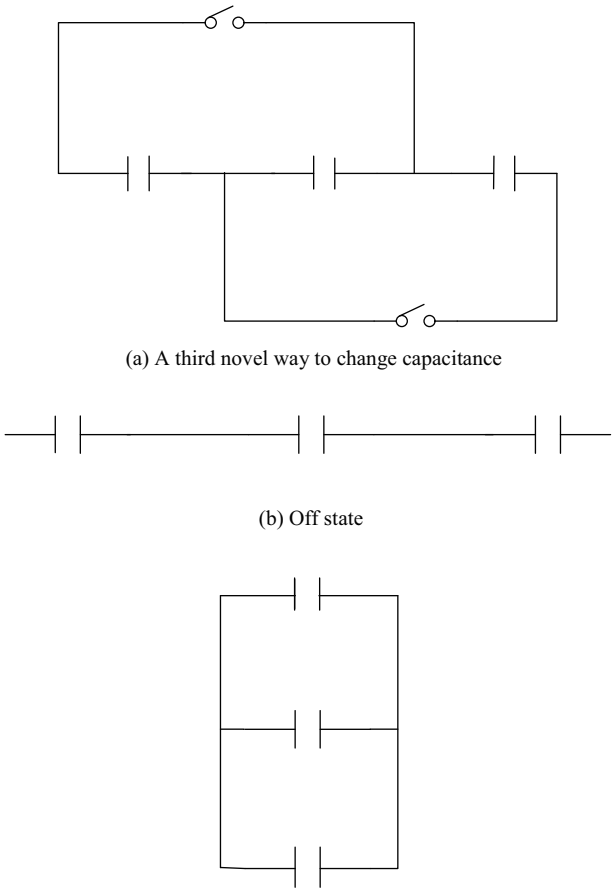

(a) A third novel way to change capacitance

(b) Off state

(c) On state

Fig. 1. A third way to change capacitance.

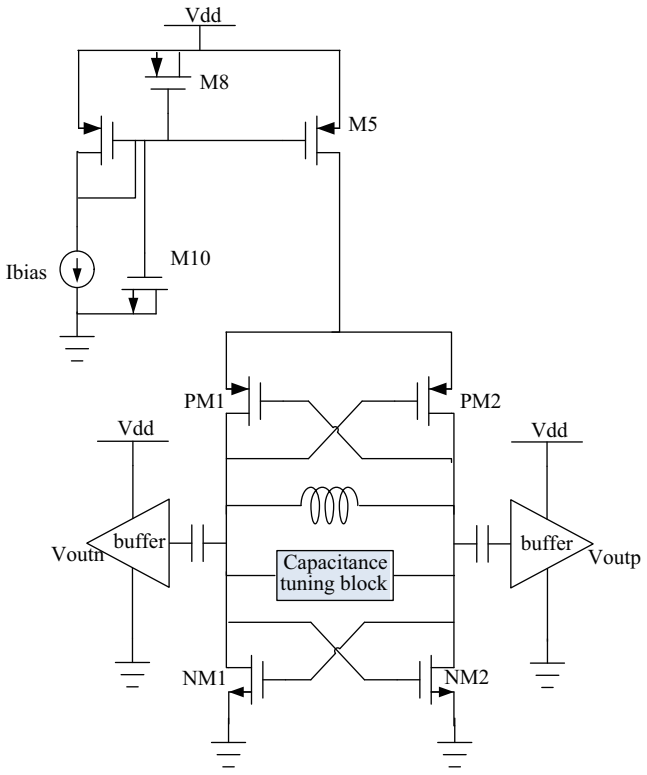

Fig. 2. Schematic of our DCO.

PMOS devices are scaled to have the same g_m to get a symmetric waveform, which results in reduced upconverted $1/f$ noise.

The digital control of the frequency is achieved by connecting a stack of tiny pMOS varactors in parallel to the tank of an LC oscillator. Each cell can be individually set in high or low capacitance state by setting the control voltage of the varactor to digital high or digital low. This bank is layout matched to the array, in order to achieve an accurate ratio, critical for stability and jitter performance. Special care has to be taken in the layout to minimize the fixed parasitic capacitance of the array.

A simplified schematic of our DCO is shown in Fig. 2. It is similar to that in Ref. [7], except that it uses a digitally controlled varactor array rather than a single differential varactor pair. In order to avoid frequency pulling by the transmitter and to easily generate LO I/Q signals, the DCO is tuned to oscillate twice the RF signal frequency needed for the mixer. A differential architecture is used to avoid supply and substrate noise coupling, which is serious in integrated conditions. An NMOS–PMOS cross-coupled structure is employed here, which is preferred in low power applications because it can produce a large g_m. The two cross-coupled transistor pairs, NM1–2 and PM1–2, produce a negative resistance to cancel the effective parasitic resistance of the LC tank. The inductor plays a critical role in the phase noise performance of the LC tank. A single completely symmetrical inductor with a higher quality factor (Q) is optimally designed. A digitally controlled PMOS current source is exploited here in order to guarantee that the oscillator operates in the current-limited regime and to improve its power supply rejection ratio (PSRR).

The array is composed of weighted PMOS varactors, whose flat high-capacitance inversion region and low-capacitance depletion region are individually used. The selection between these two regions is controlled by the multi-bit digital frequency tuning words (FTW) in the two-level buses. By setting the MOS varactors in the two flat regions rather than in the compressed linear region, the capacitance sensitivity of the DCO due to noise and operating point shifts is lowest. The PMOS varactors are chosen here because of their good isolation properties.

FTW input bits individually set the capacitance of the varactors so as to establish the expected DCO frequency. As shown in Fig. 3, the 17-bit unit-weighted coarse bank is activated during power-up and under the control of predetermined PVT (process-voltage-temperature) FTW, in order to calibrate the large oscillating frequency uncertainty due to process, voltage and temperature variations and acquire the desired operational channel. A fine bank (Fig. 4) is used to implement actual PLL tracking. In order to achieve good frequency tuning linearity and to avoid binary switching noise, unit-weighted MOS varactor cells are used in the fine bank. The fine bank is activated during actual PLL tracking. The fine bank consists of small unit-weighted PMOS varactors. PMOS varactors in the fine bank are controlled to switch alternately between the two flat capacitance regions.

To reduce the phase noise, we designed an LC tank with high Q, composed of a symmetric spiral inductor with a center-tap and an accumulation-mode MOS (A-MOS) varactor. The

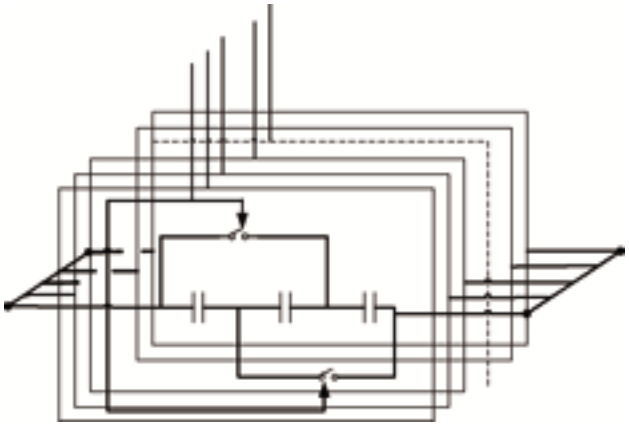

Fig. 3. Coarse bank.

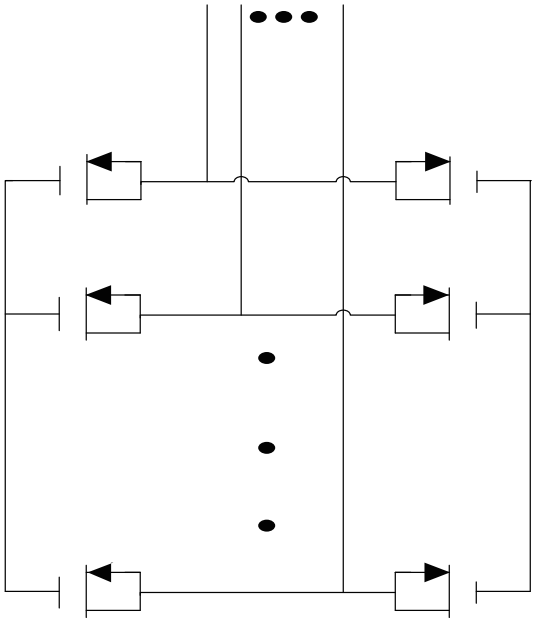

Fig. 4. Fine bank.

selection of on-chip inductors is crucial to the design of low-phase-noise DCO. In our design, a proper inductor is chosen from an inductor library of widespread values and different qualities by iteration. In addition, the two cross-coupled transistor pairs, NM1–2 and PM1–2, are chosen here to get a symmetric waveform to reduce the upconverted $1/f$ noise. The pMOS transistor current source can attain a lower close-in noise than the nMOS transistors[9, 10].

The noise contribution of the current source has a significant effect on the DCO's phase noise through upconversion. The degradation in phase noise due to bias noise is shown to be a function of MOS device sizing. By virtue of this dependency, bias noise contributions to phase noise can be minimized by design besides through filtering. Rael originally postulated that noise factor F takes the form of

$$F = 1 + \frac{4\gamma RI}{\pi V_{\rm o}} + \gamma\frac{4}{9}g_{\rm mbias}R. \quad (1)$$

This is to say that the smaller the product of the current source transconductance and the tank resistance, the smaller

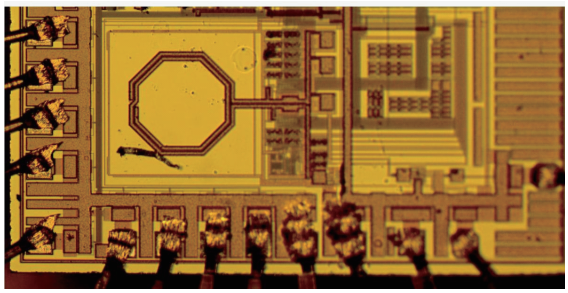

Fig. 5. Chip photograph of DCO.

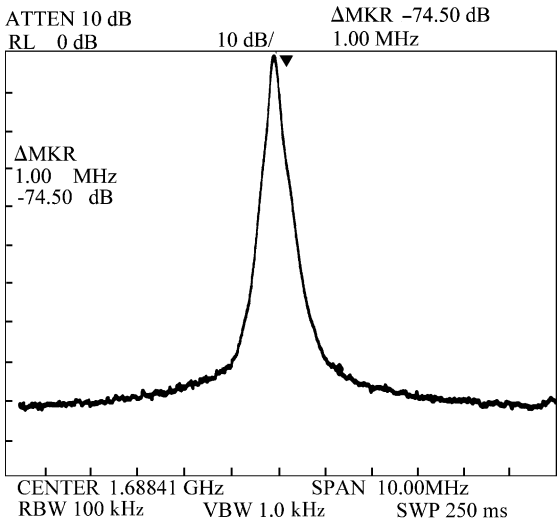

Fig. 6. Close-in spectrum of DCO @ 1.68 GHz.

the contribution of the current source to the oscillator noise factor F. So, it is advisable to reduce the current source device transconductance as a more viable alternative. For a current source device with a larger W/L, the overdrive is smaller and as a result, the phase noise is lower than that with a smaller W/L. In addition, a larger current source transistor reduces the device flicker noise, which is inversely proportional to the transistor[11,12].

By optimizing the proportion among the dimensions of M5, M2 and adding two S–D shortconnected transistors M8, M10 to filter out any noise from the reference circuit, a great improvement in phase noise performance can be achieved.

4. Experiment results

The DCO test chip was fabricated in a commercial 0.18 μm CMOS process. The measurement was performed on an FR-4 PCB test fixture. An HP8591 spectrum analyzer was used to measure the spectral density of the proposed DCO. The measured spectral densities gave the fundamental frequency of 1.68 GHz and the output power was around –4 dBm.

Figure 5 shows the micrograph of the fabricated chip. All pads are ESD protected and the onchip inductors are implemented with a top metal to get a higher Q. Figure 6 shows the output spectrum at 1.68 GHz. Figure 7 suggests that the supply pushing of DCO is less than 10 MHz/V.

From the delta-mode marker in Fig. 6, we get a phase noise

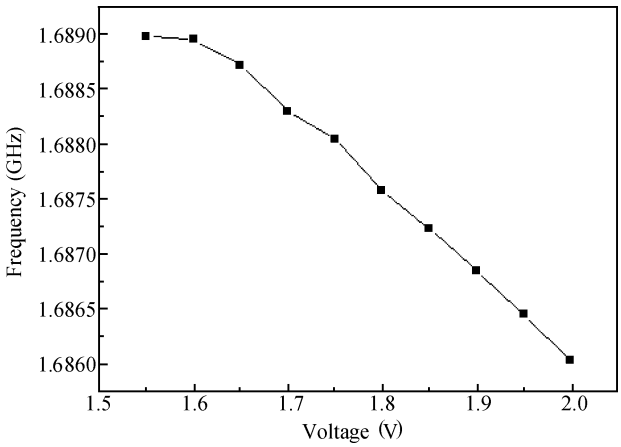

Fig. 7. Supply pushing of DCO.

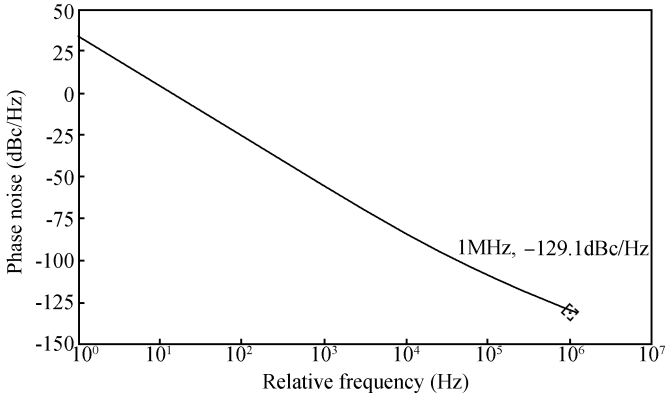

Fig. 8. Figure of phase noise.

of about –122.5 dBc/Hz at 1 MHz offset from the following equation [–129.1 dBc/Hz @ 1 MHz offset in Fig. 8 (simulation)],

$$L(f_{\text{offset}}) = 10\lg\frac{P_{\text{SSB}}}{P_{\text{S}}} = P_{\text{m}} + C_{\text{m}} - 10\lg\frac{B_{\text{m}}}{1\ \text{Hz}} - P_{\text{s}}, \quad (2)$$

where $L(f_{\text{offset}})$ is the phase noise at offset frequency f_{offset} from the carrier (in dBc/Hz), B_{m} is the measurement bandwidth (in Hz), C_{m} is the calibration coefficient of the testing system (about 2–3 dB), P_{m} is the noise power in the measurement bandwidth (in dBm), and P_{S} is the signal power (in dBm)[8].

5. Conclusion

A fully integrated low power and low phase noise LC digitally controlled oscillator (DCO) using a novel type capacitor tuning bank is presented in this paper. The fabricated DCO operates between 1.3 and 1.9 GHz. From a 1.68 GHz carrier, phase noise measurements show a phase-noise of –122.5 dBc/Hz at an offset of 1 MHz with a 1.8 V power supply and a 4.8 mA supply current for the DCO's core circuit. Also, it can work at low supply voltage conditions with a 1.6 V power supply and a 4.1 mA supply current for the DCO's core circuit, achieving a phase-noise of –121.5 dBc/Hz at an offset of 1 MHz. The supply pushing of DCO is less than 10 MHz/V.

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