8.64–11.62 GHz CMOS VCO and divider in a zero-IF 802.11a/b/g WLAN and Bluetooth application*

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Abstract: A fully integrated VCO and divider implemented in SMIC 0.13-μm RFCMOS 1P8M technology with a 1.2 V supply voltage is presented. The frequency of the VCO is tuning from 8.64 to 11.62 GHz while the quadrature LO signals for 802.11a WLAN in 5.8 GHz band or for 802.11b/g WLAN and Bluetooth in 2.4 GHz band can be obtained by a frequency division by 2 or 4, respectively. A 6 bit switched capacitor array is applied for precise tuning of all necessary frequency bands. The testing results show that the VCO has a phase noise of –113 dBc @ 1 MHz offset from the carrier of 5.5 GHz by dividing VCO output by two and the VCO core consumes 3.72 mW. The figure-of-merit for the tuning-range (FOM_T) of the VCO is –192.6 dBc/Hz.

Key words: CMOS integrated circuit; voltage controlled oscillators; phase noise; wireless LAN
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1. Introduction

With the high speed development and portable application of multi-mode transceivers, low cost and low power have become a major research area. The 2.4 GHz ISM band is the most widely used band for wireless LAN and Bluetooth application. And higher data rates can be achieved in an 802.11a WLAN standard, which can cover the band of 5–5.8 GHz. This makes the multi-band transceiver very attractive[1−3].

In this paper we propose a VCO and a high frequency divider. The VCO can cover the 8.64–11.62 GHz range, which can meet the requirements of an 802.11a WLAN after division by two, 802.11b/g and Bluetooth after division by four. The trade off between tuning range and parasitical effect at high frequency is carefully considered.

2. Design of the high-frequency wide-band VCO

2.1. Design consideration

A VCO worked at twice the LO frequency is commonly used in the application of a transceiver with zero-IF architecture. This is a suitable solution for the injection-pulling problem and can generate the quadrature output after a divider, high frequency VCO can make the inductor small to save the area as well. On the other hand, this makes the design of the VCO difficult: in some applications, just like an 802.11a WLAN, twice the LO signal can reach up to 11 GHz, and if a multi bit switched capacitor array is used to cover the wide band, the parasitic capacitance of the switches can make the frequency inaccurate. Table 1 shows the system frequency range of WLAN and Bluetooth standards.

Phase noise is another important parameter for the VCO. This can contribute to the phase noise of high frequency in the frequency synthesizer so it is of vital importance. But the phase noise will be reduced by 6 dB if the frequency of the VCO increases twofold as shown in Leeson's formula[4],

$$L(\Delta\omega) = 10\lg\left\{\frac{2FkT}{P_s}\left[1+\left(\frac{\omega_0}{2Q_L\Delta\omega}\right)^2\right]\times\left(1+\frac{\Delta\omega_{1/f^3}}{|\Delta\omega|}\right)\right\}. \quad (1)$$

where F is the device noise factor at the operating power, P_s is the oscillator output power, Q_L is the loaded quality factor, ω_0 is the oscillator carrier frequency, $\Delta\omega$ is the frequency offset from the carrier and $\Delta\omega_{1/f^3}$ is the flicker corner frequency. The phase noise can be optimized at one frequency or a narrow band, but it is difficult to do this at a wide band.

2.2. Circuit implementation

Figure 1 shows the schematic of the VCO. All the parasitic capacitance and inductor may affect the accuracy of the working frequency, especially for the high frequency VCO, so they should be carefully considered here. Some strategies to improve the performance of the VCO, especially the method to reduce the parasitic effect in the circuit, are discussed in

Table 1. VCO tuning range requirement.

Standard	Frequency range (GHz)	VCO tuning range (GHz)	Prescaler
802.11a low band	5.15–5.35	10.36–10.64	/2
802.11a high band	5.725–5.825	11.49–11.61	/2
802.11b/g	2.4–2.48	9.6–9.92	/4
Bluetooth	2.4–2.5	9.608–9.92	/4

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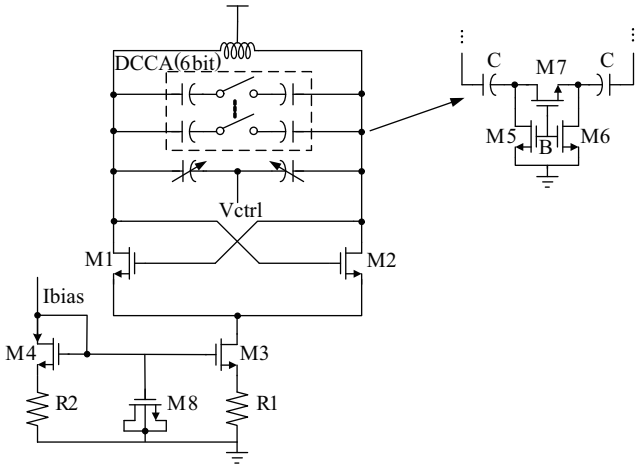

Fig. 1. VCO core schematic.

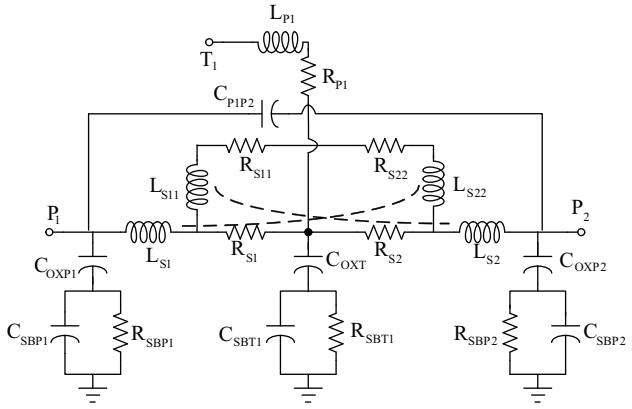

Fig. 2. Differential inductor equivalent circuit.

Section 2.2.1, while Section 2.2.2 introduces the design of the inductor.

2.2.1. Strategies in the circuit

As is shown in Fig. 1, the negative resistance is formed by pure NMOS to reduce the parasitic effect. The length of M1 and M2 should be minimized to reduce the capacitance of the common source point, and then the up-conversion gain becomes less to alleviate the effect of the $1/f$ noise. The large gate width of the switch as well as the large number of control bits may increase off-state parasitic capacitance, which cannot be used in high frequency VCO, while if a small gate width is chosen, the on-state resistance will degrade the Q value of the tank in Eq. (1), so does the phase noise. There is an optimum gate width and number of control bits for a specific operating frequency and tuning range.

In our design, a six binary-weighted capacitor array is chosen to perform coarse tuning to cover the necessary band, and the NMOS transistors M5, M6 are added to provide a DC reference point to the switch in on-state. Then the off-state capacitance can be approximated as

$$\begin{aligned}\frac{1}{C_{\text{off}}} &= \frac{1}{C} + \frac{1}{C_{\text{D5}} + C_{\text{D7}}} \\ &\approx \frac{1}{C} + \frac{1}{C_{\text{DB5}} + C_{\text{DG5}} + C_{\text{DB7}} + C_{\text{DG7}}}.\end{aligned} \tag{2}$$

C_{D5} and C_{D7} are the drain capacitance of M5 and M7, respectively. C_{DB} is the junction capacitance between the drain and the substrate. A multi-finger structure is adopted in the layout to reduce this capacitance by reducing the area of the drain. C_{DG} in Eq. (2) is just the overlap capacitance because there is no channel formed in the off-state. C = 20 fF is used in the least significant bit to achieve a good tuning characteristic in our design while considering M7's effect on the quality factor of the capacitance path:

$$Q_{\text{c}} \approx \frac{1}{\omega C R_{\text{on}}} = \frac{W_7}{L}\frac{\mu_{\text{n}} C_{\text{ox}}(V_{\text{GS}} - V_{\text{T}})}{\omega C}. \tag{3}$$

The size of M5 and M7 are chosen to make the total parasitic capacitance ($C_{\text{D5}} + C_{\text{D7}}$) less than 10 fF and not degrade the quality factor much at the same time.

The common mode output voltage of the VCO is 1.2 V, so the voltage between the two nodes of the varactor is relatively large. Additional voltage bias is needed if accumulation-MOS varactors are used. Then the parasitic capacitance is increased on the output node, which has a detrimental effect on the performance of the high frequency VCO. As for the inversion-MOS varactor, voltage between the source/drain and the gate is needed to make the carriers inverse in the channel, so no additional voltage bias is needed. It is adopted here to achieve fine tuning for its monotonic C–V characteristic when the control voltage is 0.2–1.0 V, which is just the output voltage of the filter in the frequency synthesizer.

Symmetrical spirals are applied to increase the quality factor of the LC tank and to get an area optimized, which will be discussed in the next part.

At high frequencies, the current wave form may be approximated by a sinusoid and the tank amplitude can be approximated as

$$V_{\text{tank}} \approx I_{\text{tail}} R_{\text{eq}}. \tag{4}$$

This means that it operates in the current-limited regime: I_{tail} and R_{eq} are the tail current and the equivalent parallel resistance of the tank[5], respectively. As the amplitude increases, the tail transistor will be in the triode region and the VCO will work in the voltage-limited regime. The optimized phase noise can be determined between the two regimes[6]. Our circuit is designed to operate in the current-limited regime to use the current with maximum efficiency. While considering the wide tuning range, because

$$R_{\text{eq}} = Q\omega_0 L = \frac{(\omega_0 L)^2}{r_{\text{s}}}. \tag{5}$$

R_{eq} will change a lot as the frequency change, so does the signal's amplitude, and the tail transistor may work in the triode region, which will degrade the phase noise. R1 in Fig. 1 is put here to stabilize the tail current to prevent this from happening. From another aspect, the transconductance of M1 and M2 is 4–5 times larger than $1/R_{\text{eq}}$ to ensure the oscillation of the VCO. The tail-current transistor, M3 in Fig. 1, should be properly sized since up-conversion of the transistor's $1/f$ noise will contribute to the phase noise of the VCO[5].

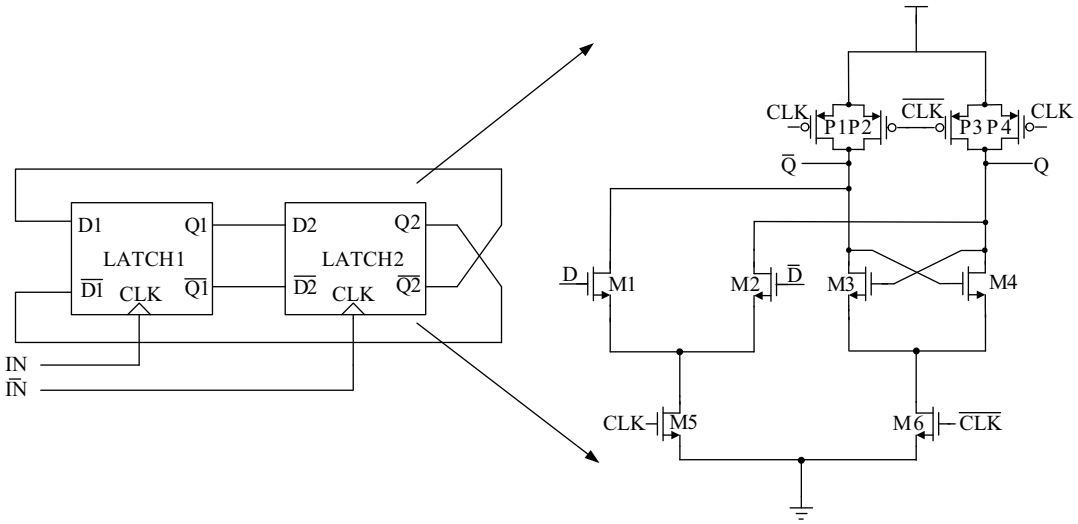

Fig. 3. Block schematic of ring oscillator and circuit schematic of D latch.

2.2.2. Inductor design

Several problems should be considered during the design of the inductor working at 10 GHz. First, a smaller inductor, which is a necessity in our design, will probably be affected by the parasitic inductor and the value of the inductor will not be stable if the working frequency is close to the self-resonant frequency (SRF). Then it will suffer from substrate coupling more seriously and will exhibit a low quality factor. To alleviate all of this, a symmetrical spiral inductor is adopted. Compared to two single-ended inductors, its winding capacitance is reduced to improve the SRF, as shown in Eq. (6):

$$\mathrm{SRF} \approx \frac{1}{2\pi\sqrt{L(C_{\mathrm{inter}} + C_{\mathrm{sub}})}}, \tag{6}$$

where C_{inter} represents the inter-winding capacitance and C_{sub} is the parasitic capacitance between the metal winding and the substrate. Both capacitances are relatively small for the symmetrical spiral inductor. A higher quality factor can also be achieved due to the lower substrate coupling, and the area can be minimized as well. Top thick metal was used to build the octagonal inductor and we chose an optimum width for the inductor, considering the skin effect. Space between the adjacent metal should be minimized to reduce the energy loss.

The S-parameter of the inductor was simulated in the advance design system (ADS) first and the equivalent circuit was built (Fig. 2). The circuit is optimized for a three-terminal inductor based on[7] to fit the characteristic curve. L_{p1} and R_{p1} represent the parasitic inductor and resistance of the centre terminal, respectively. C_{P1P2} is the inter-winding capacitance, which contributes more to the SRF in Eq. (6) for our inductor. R_{s1} and R_{s2} are series resistors including the skin effect. According to the simulation, with a SRF of about 80 GHz, the inductor is roughly 0.7 nH, including the parasitic effects and the quality factor is around 18 for the frequency range of 8.6–11.6 GHz.

3. Design of the divider

To generate the quadrature signals, the ring oscillator was adopted. The circuit is depicted in Fig. 3.

The first divider after the VCO is the most critical part because it should work properly at the highest frequency of the synthesizer and it must also cover a wide range if a wide band VCO is used. In our design, the divider should work at 8.6–11.6 GHz, covering about 3 GHz. The phase noise can be expressed as[8]

$$L_{\omega} = 8\pi^2\left(1 + \frac{\gamma}{\alpha} + \frac{\gamma_{\mathrm{T}} g_{\mathrm{mT}} R_{\mathrm{L}}}{2\alpha_{\mathrm{T}}}\right)\frac{kTC_{\mathrm{L}}}{I_{\mathrm{B}}^2} f_{\mathrm{out}} Q, \tag{7}$$

if the tail current source exists. The three polynomials in the brackets can represent the noise contribution from the load transistors, the input differential pair and the tail current generator. I_{B} and C_{L} represent the total current of the divider and the load capacitance, respectively. There is no tail current generator in our design, so the phase noise can be improved, and that can also help to solve the problem of the signal swing as the power voltage becomes lower in deep sub-micron technology.

The transistors M1 and M2 compose the logic pair to sample the input signal when CLK is high and M3 and M4 form the latch pair to hold the signal. M6 is added here to reduce the signal swing and also decrease the capacitive load at node Q/$\overline{Q}$, thus improving the operation speed. But in a lower frequency range, M6 will discharge the output node and this will affect the setting of positive feedback formed by M3 and M4. So P1 and P4 are introduced to inject current periodically to counteract this effect[9]. The size of P1 and P4 is less than that of P2 and P3 to make the load resistant, so does the RC time constant, less in the latch mode than that in the sample mode to achieve the maximum operating frequency. The self-resonance frequency is set to 6 GHz, about $f_{\mathrm{vco}}/2$, to make the divider work well at high frequency. The length of all the transistors is minimized to reduce the load capacitance.

4. Experimental results

The implemented VCO and divider have been integrated into SMIC 0.13-μm RFCMOS 1P8M technology with a 1.2 V power supply. Figure 4 shows the chip photomicrograph. The

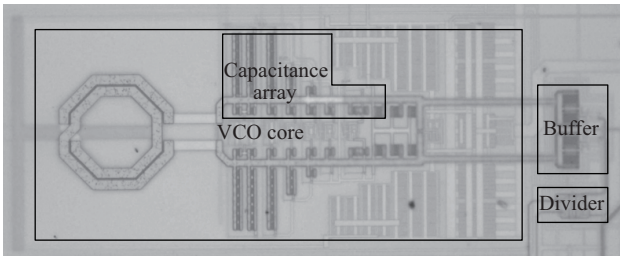

Fig. 4. Chip photomicrograph of VCO and divider.

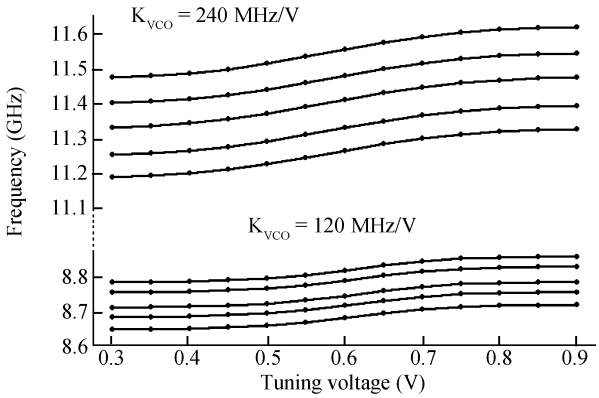

Fig. 5. VCO tuning range.

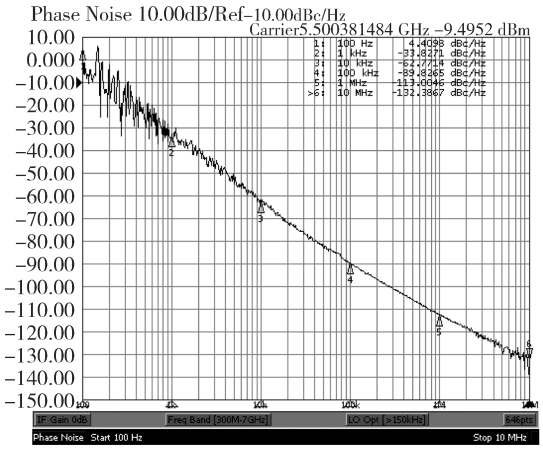

Fig. 6. Phase noise at 5.50 GHz output. Notice that the data are acquired at the output of the divider.

size of the VCO core is about 200 × 450 μm^2. The signal after the divider was measured using an Agilent E5052A signal source analyzer. Changing different switches in the printed circuit board (PCB) to adjust the capacitor array, the tuning characteristics are shown in Fig. 5. 8.64–11.62 GHz was covered with a good overlap characteristic and it was about 30% of the centre frequency. The tuning range can meet the requirement well and the sensitivity of the VCO varies from 120 to 240 MHz/V. This proves the accuracy of the inductor and capacitance values in the design.

The phase noise degrades as the frequency increases. The worst case phase noise of the VCO and divider was measured and is shown in Fig. 6 when the VCO was operating at 11 GHz. The phase noise is –89.8 dBc/Hz at 100 kHz offset and –113

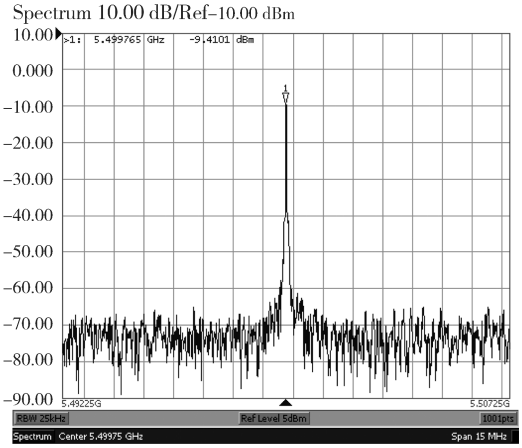

Fig. 7. Frequency spectrum at 5.50 GHz output.

dBc/Hz at 1 MHz offset. The quality factor of the inductor will affect the phase noise significantly, so the result illustrates the quality factor of the inductor to some extent. Figure 7 shows the spectrum of the output.

A widely used figure of merit (FOM) for VCO is defined as[10]

$$\mathrm{FOM} = \mathrm{PN}\{\Delta f\} - 20\lg\frac{f_0}{\Delta f} + 10\lg\frac{P_\mathrm{w}}{1\mathrm{mW}}, \qquad (8)$$

where $\mathrm{PN}\{\Delta f\}$ is the phase noise at the offset of Δf from the carrier f_0. P_w is the DC power consumption in mW. The FOM of the VCO is about –183.1 dBc/Hz and, considering the tuning range, there is also $\mathrm{FOM_T}$[10] to evaluate the performance of the VCO because it is difficult to optimize the phase noise in a wide tuning range:

$$\mathrm{FOM_T} = \mathrm{FOM} - 20\lg\frac{\mathrm{FTR}}{10}, \qquad (9)$$

where FTR is the frequency tuning range, which is about 30% in our VCO, and $\mathrm{FOM_T}$ is about –192.6 dBc/Hz.

Table 2 lists a performance comparison between this work and other published high frequency VCOs (wide band VCO[11−13] and narrow band VCO[14−17]), focusing on the FOM, $\mathrm{FOM_T}$ and so on.

5. Conclusion

A high frequency wide band VCO and a divider have been fabricated in a SMIC 0.13-μm RFCMOS 1P8M process. A 6-bit switched capacitor array enabled the L-C VCO to have the frequency tuning range of 30%, from 8.64 to 11.62 GHz. Tested after the divider, the phase noise was as low as –113 dBc @ 1 MHz from 5.5 GHz carrier. The power consumption was only 3.72 mW under a 1.2 V power supply. These lead the figure of merit of the VCO to achieve –192.6 dBc/Hz if the tuning range is considered.

Therefore the VCO and the divider are good candidates for the multi-mode synthesizer in Zero-IF 802.11a/b/g WLAN and Bluetooth applications.

Table 2. Summary and comparison of performance with other high frequency VCOs.

Ref VCO	Center frequency (GHz)	Phase noise @ 1 MHz (dBc/Hz)	FOM (dBc/Hz)	FOM_T (dBc/Hz)	Power (mW)	Technology
Chiu[11]	26	–102.9	–179	–181.8	18.6	0.18 μm CMOS
Chen[12]	40	–108.6	–193	–181.79	6.0	0.18 μm CMOS
Yusuke[13]	28	–112.9	–190.9	–187.42	12	0.13 μm CMOS
Baek[14]	8.0	–117	–181.3	NA	24	0.18 μm CMOS
Ko[15]	10.0	–118.7	–187.9	NA	11.88	0.18 μm CMOS
Oh[16]	11.22	–109.4	–182	NA	6.84	0.18 μm CMOS
Park[17]	11.55	–110.8	–183	NA	8.1	0.18 μm CMOS
This work	5.5 (VCO +divider)	–113				0.13 μm CMOS
	11	(–113+5)*	–183.1	–192.6	3.72	

* The simulation speculated that the phase noise would be improved by about 5 dBc/Hz @ 1 MHz after the divider.

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