A low power 3.125 Gbps CMOS analog equalizer for serial links*

Ju Hao(巨浩)†, Zhou Yumei(周玉梅), and Jiao Yishu(矫逸书)

(Institute of Microelectronics, Chinese Academy of Sciences, Beijing 100029, China)

Abstract: A CMOS analog equalizer is designed to meet the different high speed communication specifications, such as USB 2.0, PCI-E and rapid IO. The proposed circuit architecture could facilitate the wide frequency scale ranging from 1 to 3.125 Gbps by adjusting the locations of pole and zero, so that the circuit can change its response accordingly as the channel characteristic alters. In order to balance the parasitic capacitors in the internal point, symmetric switches are addressed to generate the equal load for differential signals. A prototype chip was fabricated in 0.13-μm 1P8M mix-signal CMOS technology. The actual area is 0.49×0.5 mm^2, and the analog equalizer operates up to 3.125 Gbps over 3 m RG-58 coaxial cable and 50 cm FR4-PCB trace. The overall power dissipation is approximately 14.4 mW.

Key words: analog equalizer; RG-58; CMOS
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1. Introduction

As transmission speed increases, channel loss is becoming more and more severe. This will cause inter symbol interference (ISI) and restrict the transmission rate[1]. There are many methods reported to overcome the limitation. The most popular method is to adopt pre-emphasis in the output of the transmitter[2−4]. Another method is to utilize an equalizer to compensate the channel's loss. Receiver equalization can be categorized into two methods: discrete-time equalization and continuous-time equalization. In the digital domain, the equalization relies on the recovered clock, which is not the case for the clock data recovery (CDR) in the receiver. So the cross-couple architecture will make the adaptation more complex and unstable. In Ref. [5], an open loop equalizer filter is proposed, and the unstable low frequency gain is produced because of increased bandwidth. Moreover, some scholar gave negative resistor feed back[6] and g_m-matched diode-connected transistor[7] to fix the gain. However, these approaches could not give a good performance as they are mismatched to the high frequency boosting path. In addition, the pre-emphasis and equalization are combined to equalize the channel loss[8].

Based on these reasons, an analog equalizer is selected as our target, which is often used in CDR[9]. In this paper, an analog equalizer was designed to equalize the loss of the channel and it offers an optimized method to eliminate the parasitic capacitor in the critical path through connecting a same scaled MOS switch, which could increase the low-frequency gain and high-frequency boosting. The merged path utilized to balance the low frequency gain and high frequency boosting is more flexible to choose different factors to equalize. Compared with conventional topology, it is a novel idea to implement the principle of equalization in the receiver.

2. Limitation of low pass channel characteristic

Figure 1 shows the attenuation characteristic of a low pass channel[10−12]. When a signal with well-defined quality transfers in the channel, flat loss stays constant for all the signal frequency. This results from the system attenuation from the transmitter to the receiver, and is unrelated to frequency. However, the channel will give rise to different losses for different signal frequency gradients. Compared with low-frequency gradients, high-frequency gradients suffer from great loss, which is due to the low pass characteristic of the channel.

If G_{TX} presents the transmitter gain of signal, G_{CH} refers to the gain of the channel and G_{RX} is the gain of the analog equalizer in the receiver front-end, and the transfer function can be presented as

$$H(s) = 20 \lg G_{TX}(s) G_{CH}(s) G_{RX}(s). \quad (1)$$

In order to compensate the losses, which include flat loss and frequency dependent loss, we should design a circuit whose response should have some gain to compensate flat loss, and the high-frequency should have great gain to expiate fre-

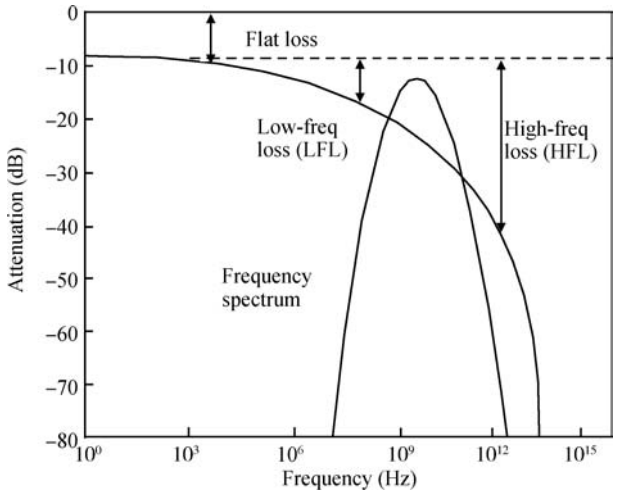

Fig. 1. Attenuation characteristic of low pass channel.

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† Corresponding author. Email: juhao0122@163.com
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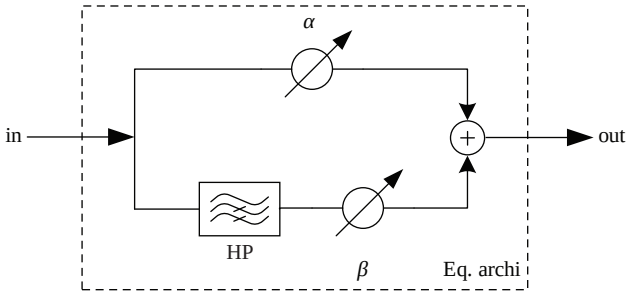

Fig. 2. Block diagram of conventional equalizer.

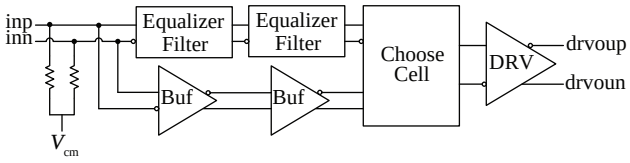

Fig. 3. Overall architecture.

quency dependent on the channel. In other words, it is a high pass filter.

Figure 2 is a block diagram of a conventional equalizer. The received signal from the channel goes through two separate paths: the gain path and the high-frequency boosting path. The output signal is the combination of the two paths. Although it can implement the basic function of the equalizer, it has some deficits in the realized application. Firstly, factors α and β are often manually adjusted to adapt the different signal or different channel. This will result in the overestimate or underestimate of the loss of the channel. Secondly, the bandwidth of the high pass filter (HP) is fixed, so it will lead to the limitation of the signal speed. We should implement an equalizer that could cover a wide frequency in different communication specifications.

3. Circuit design

The proposed analog equalizer topology was adopted in the serial link receiver. In order to give an insight into the outcomes of equalization and equalization-free topologies, a choose circuit is addressed to compare the eye diagrams of the two. Figure 3 shows the straightforward principle of the architecture.

The common mode voltage is added to the architecture through the matched resistors, which equals the characteristic impedance of the test board. We cascade two equalizing filters in order to boost the low and high frequency gain. The buffer has the same gain as the equalizing filter in the low frequency, so we could compare two signals from separate paths.

3.1. Equalizer filter

The equalizer is based on conventional source follower architecture topology, as shown in Fig. 4.

The overall transfer function is as follows:

$$H(s) = \frac{-g_{\mathrm{m}}R_{\mathrm{L}}(1+sRC)}{1+\dfrac{1}{2}g_{\mathrm{m}}R+sRC}. \tag{2}$$

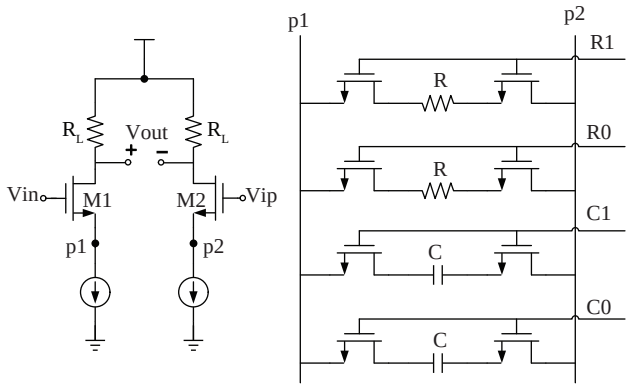

Fig. 4. Topology of proposed analog equalizer.

So the pole is $f_{\mathrm{z}} = \frac{1}{2\pi RC}$ and the zero is $f_{\mathrm{p}} = (1 + \frac{1}{2}g_{\mathrm{m}}R)\frac{1}{2\pi RC}$.

MOS switches are used to add or subtract resistors or capacitors to and from the equalizer circuit. Switches are symmetric for the two paths. As a result, the parasitic capacitors in points p1 and p2 are the same if we set all switches to have the same size. The circuit can adjust the low-frequency gain and high-frequency boosting gain by connecting MOS switches. The main advantage is that the parasitic capacitors in point p1 and p2 can be considered as astride the capacitor between p1 and p2. The AC simulation curve is illustrated in Fig. 5.

The diagram shows the good performance of the proposed equalizer topologies based on the conventional architectures. The low-frequency gain is adjusted by resister switches, while capacitor switches regulate the high frequency boosting.

3.2. Choose cell

The choose cell is brought into play by controlling the tail current. The CLK and CLKB signals are complementary control ports, as shown in Fig. 6. The main concern about the architecture is keeping the two branches symmetric, so it will recur to detailed layout design. Post-simulation results show that the choose cell has a good performance to output signal of different paths.

4. Measure setup and results

Figure 7 is a photomicrograph of the prototype chip. The output driver buffer is contained to detect the signal's eye diagram after equalization. The chip was fabricated in a Charter 0.13-μm eight-metal mix signal CMOS process. The actual area of the chip is 0.49×0.5 mm^2 and the power dissipation is 14.4 mW with a 1.5-V supply voltage. An Agilent pulse generator 81134A sends (2^7–1) a pseudorandom bit sequence (PRBS) to the chip through an RG-58 coaxial cable and a PCB trace. The outputs of the chip connect to an Agilent Digital Signal Analyzer DSA 91304A. The pulse generator creates (2^7–1) a PRBS at 3. Figure 8 shows the eye diagram of the output of a 3 m RG-58 coaxial cable and a 50 cm PCB trace at 1.25 Gbps. From the outcome of the test, we can see that the eye height is closed because of the loss of coaxial cable. Figure 9 shows the eye diagram after equalization at 1.25 Gbps, and it gives a good signal quality for the following CDR or digital signal processing. Figures 10 and 11 show the eye diagram of the signal

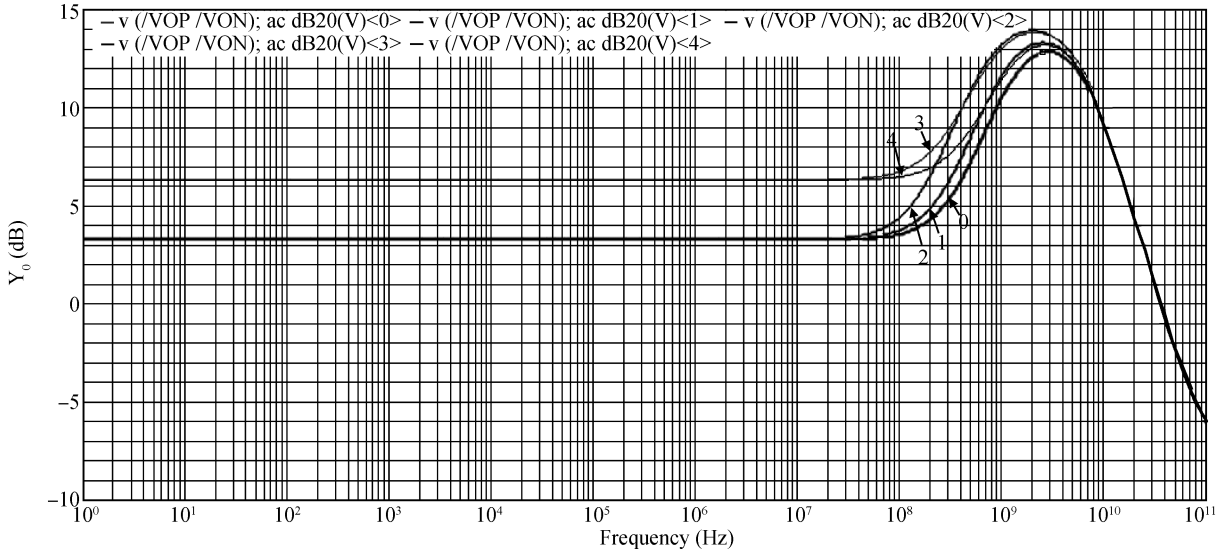

Fig. 5. Simulation curve of analog equalizer.

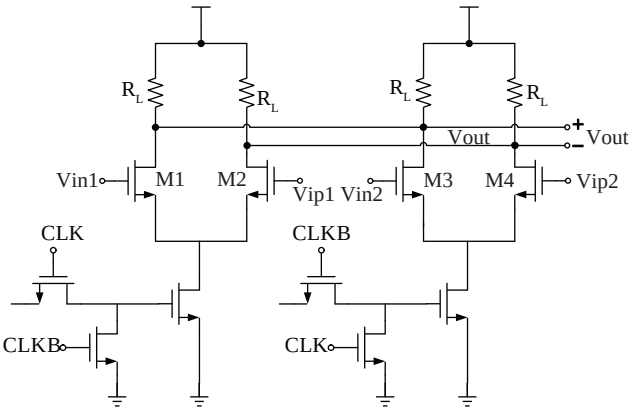

Fig. 6. Topology of the choose cell.

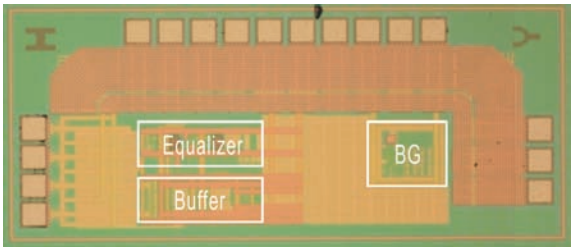

Fig. 7. Photomicrograph of the prototype chip.

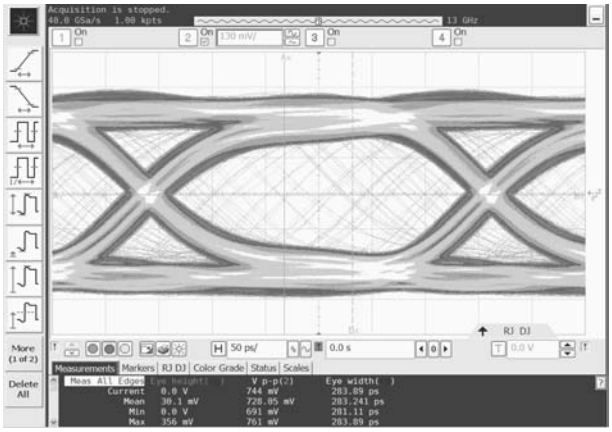

Fig. 8. Eye diagram of PCB trace (50 cm) at 1.25 Gbps.

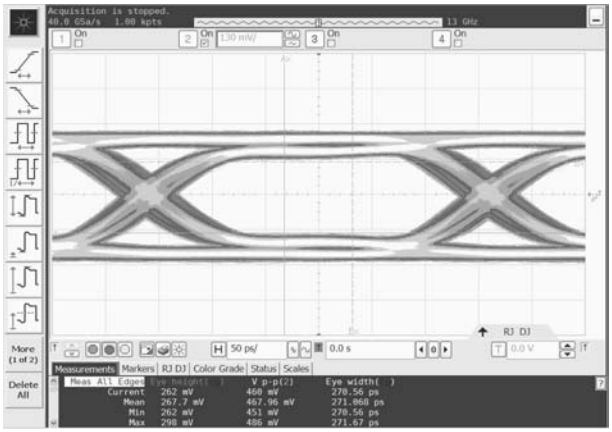

Fig. 9. Eye diagram after equalization at 1.25 Gbps.

before and after equalization at 2.5 Gbps. As the data rate is up to 3.125 Gbps, the test result also gives a good eye diagram of the received signal after equalization, as is shown in Figs. 12 and 13.

From the measurement result, the attenuation of the channel becomes more and more severe as the data rate improves. Compared with the eye diagram of the signal before equalization, the proposed equalization could compensate the attenuation of the transferring channel effectively at different data rate. In addition, the differential amplitude of the transfer signal could reach as low as 200 mV peak-to-peak, which will meet many high speed communication specifications, such as USB 2.0, PCI-E and rapid IO.

5. Conclusion

A low power 3.125 Gbps CMOS analog equalizer for a serial link is proposed based on conventional architecture.

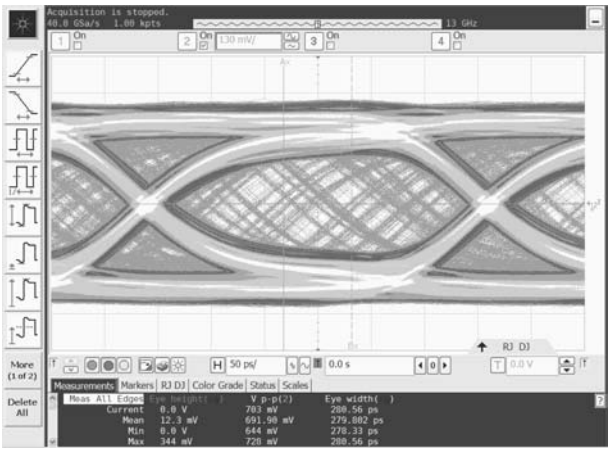

Fig. 10. Eye diagram of PCB trace (50 cm) at 2.5 Gbps.

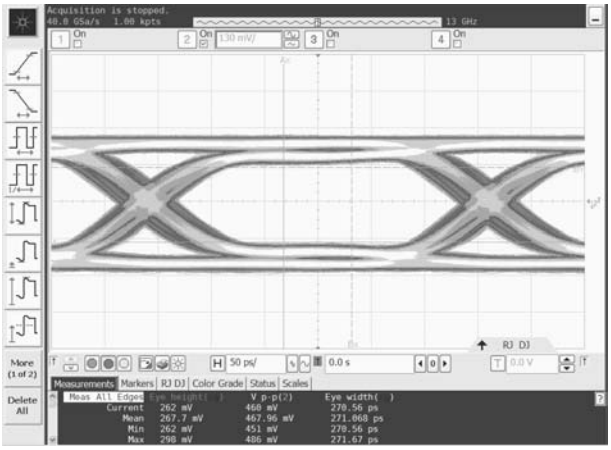

Fig. 11. Eye diagram after equalization at 2.5 Gbps.

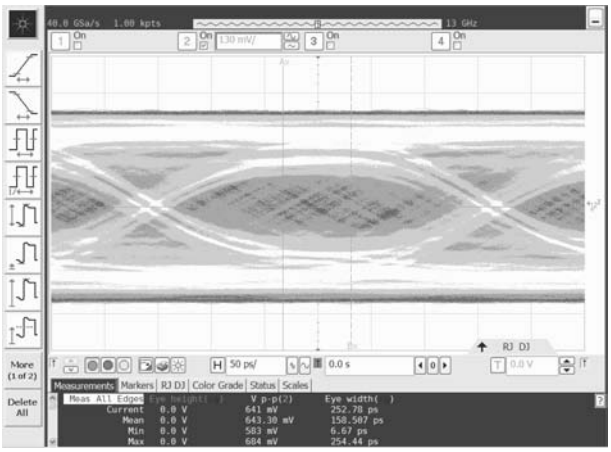

Fig. 12. Eye diagram of PCB trace (50 cm) at 3.125 Gbps.

The equalizer topology could merge low-frequency and high-frequency paths together, eliminating the effect of the parasitic capacitor. The merged paths could collaborate with each other to adjust the low-frequency gain and high-boosting level. The implemented chip can operate up to 3.125 Gbps through a 3 m RG-58 coaxial cable and a 50 cm FR4 PCB trace.

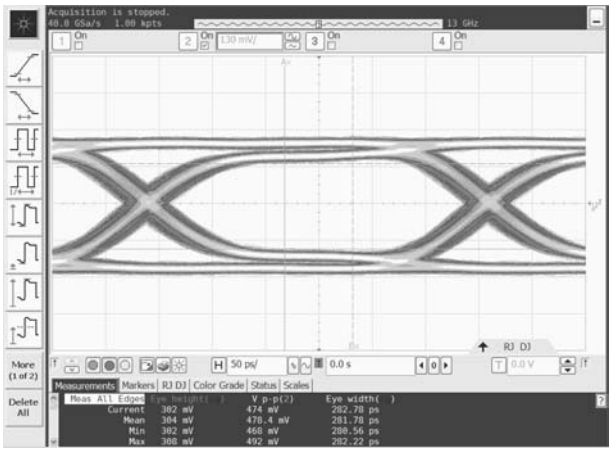

Fig. 13. Eye diagram after equalization at 3.125 Gbps.

Table 1. Measurement summary.

Parameter	Value
Data rate	3.125 Gbps
Supply voltage	1.5 V
Current consumption	9.6 mA (without output buffer)
Chip area	0.49×0.5 mm^2 (including pads)
Technology	0.13 μm CMOS

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