Design of high efficiency dual-mode buck DC–DC converter*

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Abstract: A buck DC–DC switching regulator with high efficiency is implemented by automatically altering the modulation mode according to load current, and it can operate with an input range of 4.5 to 30 V. At light load current, the converter operates in skip mode. The converter enters PWM mode operation with increasing load current. It reduces the switching loss at light load and standby state, which results in prolonging battery lifetime and stand-by time. Meanwhile, externally adjustable soft-start minimizes the inrush supply current and avoids the overshoot of output voltage at initial startup. The regulator is fabricated by a 0.6 μm CDMOS process. The test results show that, under the condition of 3.3 V output, the efficiency is up to 64% at 5 mA and the maximum efficiency is 95.5%.

Key words: high efficiency; soft-start; skip mode; PWM mode
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1. Introduction

With the rapid development and continuous innovation of integrated circuit (IC) technology, switching DC–DC converters are widely used in network systems, PC equipment and portable devices. However, the power dissipation of these products is highly increased with the improvement in their performance. Hence, more attention has been paid to how to increase the output current and raise conversion efficiency. In addition, PC devices have a wide load current range, which has been up to A level. For prolonged battery lifetime and standby time, a DC–DC converter that can keep high efficiency in a wide load current range is needed[1,2].

The power dissipation of DC–DC converters can be divided into three parts: conduction loss, switching loss and quiescent dissipation. The conduction loss includes dissipation caused by the equivalent series resistance (ESR) of the inductance and the capacitor, and the conduction resistance of the power transistors. The switching loss is introduced by charging and discharging the parasitic capacitance of the power transistors when the drive circuit moves. The quiescent dissipation is mainly caused by the quiescent current of the chip.

The common method to solve the above problems involves reducing the switching frequency at light load, which can degrade the switching loss. Then the efficiency of the converter can maintain a similar level with a heavy load; for instance, PWM/PFM multi-mode modulation[3−7]. The disadvantage of this method is that the switching frequency varies with load, which makes the circuit complicated. Based on widely used PWM control construction, a buck DC–DC switching regulator with high efficiency is implemented by automatically altering the modulation mode according to the load current in this paper. The converter operates in skip mode at light load current and enters PWM mode operation with increasing load current. It reduces the power dissipation at light load and standby state, which results in prolonging battery lifetime and standby time. In addition, a novel compound comparator is adopted in the design, which not only simplifies the circuit but also decreases the quiescent dissipation. Also, an externally adjustable soft-start minimizes the inrush supply current and the output overshoot at initial startup.

2. Circuit design

2.1. Architecture of the proposed buck DC–DC converter

Figure 1 shows the diagram and off chip components of the proposed DC–DC converter. Inductor L and capacitor $C_{\rm out}$ in dashed line compose a low pass filter (LPF), which forms the feedback network with $R_{\rm FB1}$ and $R_{\rm FB2}$. The block of regulator, OSC and bandgap reference (BGR) are basic parts in chip. The structure of slope compensation, error amplifier (EA), PWM comparator, skip controller, load current detector, logic control, power MOS Mup and Mdown together make up the critical circuit, which controls the skip mode and PWM mode.

2.2. Design of compound comparator and control loop of PWM

In Fig. 1, the PWM comparator and RS flip-flop in logic form the PWM modulator. The non-inverting input of the PWM comparator is a superimposed voltage $V_{\rm S}$, which is generated by a DC current signal, slope compensation current and sense current through a resistor. This can be expressed by

$$V_{\rm S} = I_{\rm DC}R_1 + I_{\rm slope}R_1 + I_{\rm sense}R_1. \quad (1)$$

The first term generates a fixed reference voltage, which provides a proper DC operating point. The second item is slope compensation, which rises with increasing duty cycle and ensures the stability of the current loop. The last part changes linearly with the inductor current. $I_{\rm sense}$ is generated by the

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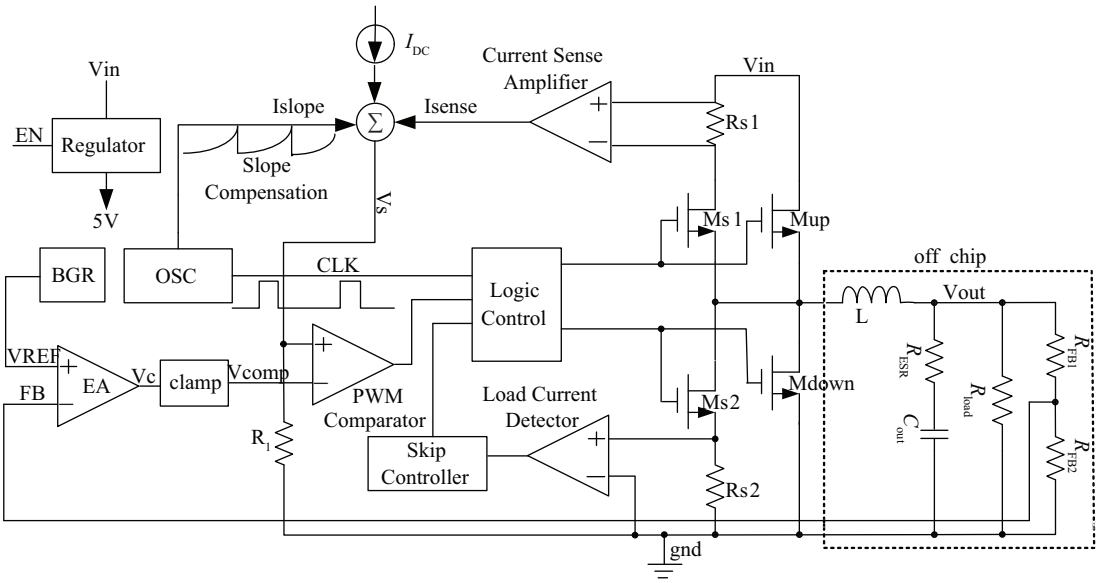

Fig. 1. Architecture of the proposed buck DC–DC converter.

sense resistor R_{s1} and the current sampling amplifier. The inverting input of the PWM comparator is V_{comp}, which is the output of the error amplifier V_C through a clamp module. The clamp block has a high-threshold V_H and a low-threshold V_L. Under normal circumstances, the error signal V_C is located between the high and the low threshold. Hence there is no need to clamp it. At this time the peak inductor current is decided by V_C. To prevent large inductor current damage, inner power transistor Mup. Therefore, V_C is high clamped. When V_C is higher than V_H, the peak inductor current is decided by V_H. In contrast, when V_C is lower than V_L, the peak inductor current is decided by V_L. When the rising edge of CLK comes, it begins a cycle of the PWM comparator, turning on Mup and turning off Mdown. The inductor current I_L ramps up with the slope of $(V_{in} - V_{out})/L$. When V_s is higher than V_{comp}, the output of the PWM comparator triggers the RS flip-flop, turning off Mup and turning on Mdown. At this time, the inductor current I_L ramps down with the slope of V_{out}/L until the next CLK arrives. In each cycle, when $I_L < I_{out}$, V_{out} decreases, and vice versa. So, in the stable state, V_{out} has a slight fluctuation in each cycle and produces what we call ripple.

A novel compound comparator is used during the realization of the circuit, which can achieve the logic function of three comparators. However, its power dissipation only equals one traditional comparator. Figure 2 shows the structure of the compound comparator, where $(W/L)_{1-4} = 40\ \mu$m/1 μm, $(W/L)_{5,8} = 15\ \mu$m/5 μm, $(W/L)_{6,7,9,10} = 5\ \mu m/5\ \mu$m, $I_{bias} = 12\ \mu$A. For $V_L < V_H$, the work principle can be described as follows. If $V_{comp} < V_L$, the transistor M4 turns on and M2 turns off, then M1 and M2 form differential pairs. When V_S is up to V_L, the output of comparator V_{oishut} is high and the main switch transistor turns off. If $V_L < V_{comp} < V_H$, the transistor M3 turns on and M4 turns off, then M1 and M2 make up of differential pairs. When V_S climbs up to V_L, V_{oishut} is high and the main switch transistor is off. If $V_{comp} > V_H$, the transistor M4 turns off, then M1 and M3 consist of differential pairs. When V_S rises to V_H, V_{oishut} is high and turns off the main switch transistor. On the basis of the above analysis, the output of the compound comparator can be described with a truth table (see Table 1).

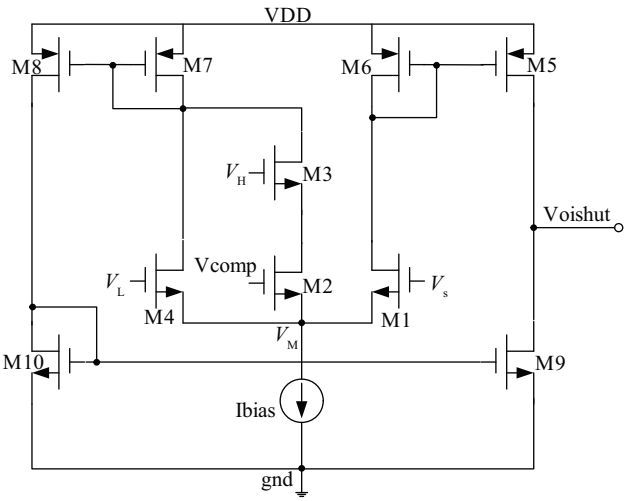

Fig. 2. Micrograph of the chip.

Table 1. Truth table of the proposed compound comparator.

Input (V_S, V_L, V_H, V_{comp})		Output (V_{oishut})
$V_{comp} < V_L < V_H$	$V_S < V_L$	0
	$V_S > V_L$	1
$V_L < V_{comp} < V_H$	$V_S < V_{comp}$	0
	$V_S > V_{comp}$	1
$V_L < V_H < V_{comp}$	$V_S < V_H$	0
	$V_S > V_H$	1

However, the differential pairs of the compound comparator have a mismatch for inconsistent circumstances. It can be proved that the ultimate error occurs at $V_{comp} = V_H$, and the corresponding ideal transition threshold of V_S is V_{comp}. So the actual transition threshold V_{sth} can be obtained when the current through M6 and M7 equals

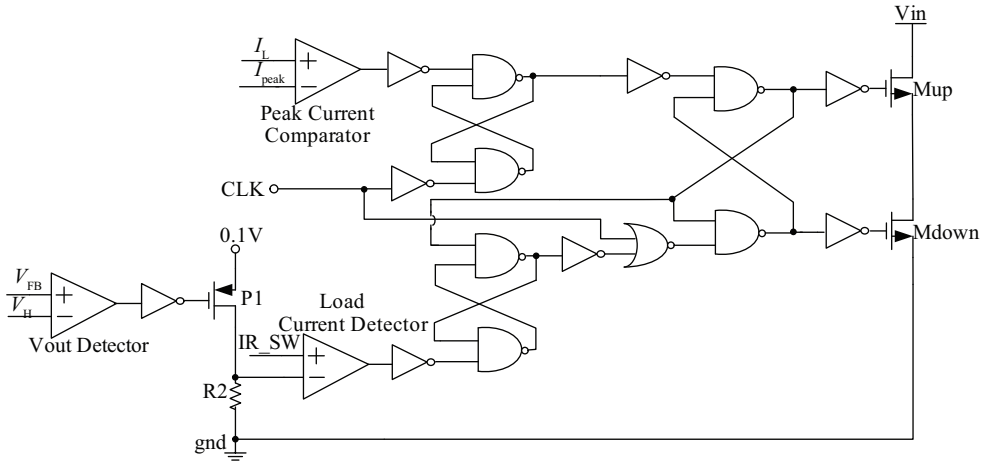

Fig. 3. Block diagram of skip mode loop.

$$V_{\rm sth} = V_{\rm M} + V_{\rm THN} + \sqrt{\frac{I_{\rm bias}}{\mu_{\rm N} C_{\rm ox}(W/L)_{1\sim4}}}, \quad (2)$$

where $V_{\rm THN}$ is the threshold voltage of NMOS, $\mu_{\rm N}$ and $C_{\rm OX}$ stand for the surface mobility of NMOS and the capacitance per unit area of the gate oxide, respectively. $V_{\rm comp}$ can be expressed as

$$V_{\rm comp} = V_{\rm M} + V_{\rm THN} + \sqrt{\frac{2I_{\rm bias}}{\mu_{\rm N} C_{\rm ox}(W/L)_{1\sim4}}}. \quad (3)$$

So the threshold error $\Delta_{\rm max}$ is

$$\Delta_{\rm max} = V_{\rm comp} - V_{\rm sth} = (\sqrt{2}-1)\sqrt{\frac{I_{\rm bias}}{\mu_{\rm N} C_{\rm ox}(W/L)_{1\sim4}}}. \quad (4)$$

Equation. (4) indicates that $\Delta_{\rm max}$ can be reduced by lowering $I_{\rm bias}$ or increasing $(W/L)_{1-4}$. But lowering $I_{\rm bias}$ will degrade the output slew rate of the comparator simultaneously, and increasing $(W/L)_{1-4}$ will add input capacitance. All these should be considered in the design. However, the feedback loop of the DC–DC converter can adjust $V_{\rm C}$ promptly and achieve a dynamic balance, so the effect of threshold drift will not be obvious. In addition, the high and low clamp don't need to be accurate in practice, so it is easy to realize the desired compound comparator. When $V_{\rm comp}$ is 2 V, the compound comparator will trigger as $V_{\rm s}$ climbs to 2.01 V with a slope of 1 V/μs, and the transmission delay is only 12 ns, which satisfies the design requirement. Moreover, the transmission delay changes slightly with $V_{\rm comp}$ fluctuation.

2.3. Realization of skip mode

The principle diagram of this converter working at skip mode is shown in Fig. 3, which is mainly composed of a peak current comparator (PCC), a $V_{\rm out}$ detector, a load current detector (LCD) and a logic circuit. $I_{\rm peak}$ is the peak current of inductance, which is proportional to $V_{\rm in}$. IR_SW is a reversed signal detected of low-side switch. $V_{\rm H}$ is the high threshold of $V_{\rm FB}$, set as 1 V (where the reference voltage is 0.925 V). Thus

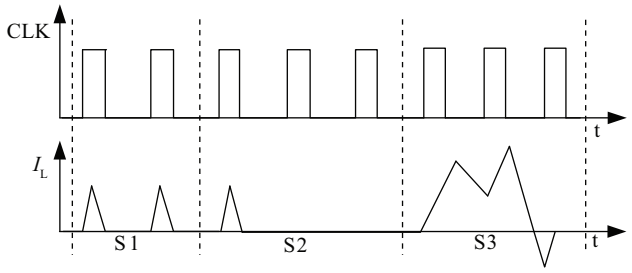

Fig. 4. Sketch waveform of skip mode.

the high threshold $V_{\rm out\_high}$ of output voltage can be expressed as

$$V_{\rm out\_high} = \left(1 + \frac{R_{\rm FB1}}{R_{\rm FB2}}\right) V_{\rm H}. \quad (5)$$

At the beginning cycle of the skip mode, $I_{\rm L} < I_{\rm peak}$, the upside transistor Mup turns on, thereby $I_{\rm L}$ ramps up and $V_{\rm out}$ rises. When $I_{\rm L}$ goes up to $I_{\rm peak}$, the output of the PCC is high, turning off Mup and turning on the downside transistor Mdown. Meanwhile, $I_{\rm L}$ ramps down and $V_{\rm out}$ begins to drop for $I_{\rm L} < I_{\rm load}$. The output of the LCD is high and turns off Mdown when $I_{\rm L}$ comes down to zero. If the next rising edge is coming and the output of the PCC is low, the high-side switch Mup turns on and works repeatedly (see state S1 in Fig. 4). Conversely, the chip will skip this cycle and keep $I_{\rm L} = 0$ (see state S2 in Fig. 4). Sometimes the inductor current doesn't fall to zero in the former cycle and Mup turns on in the latter cycle. As a result, $I_{\rm L}$ and $V_{\rm out}$ will rise persistently. If $V_{\rm out} > V_{\rm H}$, the output of the LCD is high and transistor P1 turns on, so the noninverting input of the comparator connects 0.1 V voltage and the inductor current can flow reversely. So the output voltage can be returned to normal and the overshoot phenomenon will be avoided (see state S3 in Fig. 4).

3. Test results

This converter has been implemented with a 0.6 μm CDMOS process. Figure 5 shows the micrograph of the chip. The high-side of the photo shows the power MOS switches and the low-side shows the control circuit.

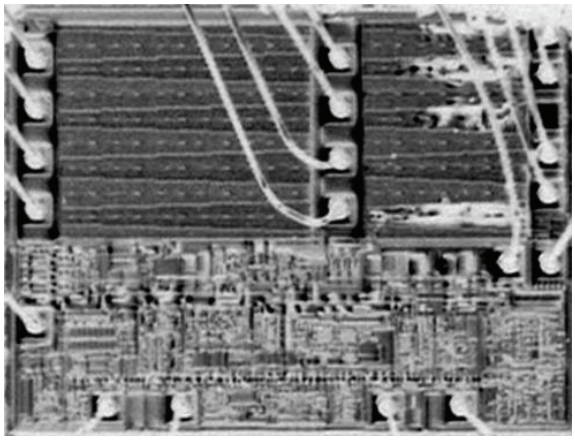

Fig. 5. Micrograph of the chip.

Table 2. Performance comparison summary of the chips.

Parameter	MP1484	Proposed
Inductor (off chip) (μH)	10	10
Output capacitor (μF)	20	44
Frequency (kHz)	340	340
Quiescent current (μA)	1300	450
Ripple voltage @ 1 A (mV)	20	16
Efficiency @ 200 mA, V_{in} = 5 V, V_{out} = 3.3 V (%)	94	95
Efficiency @ 200 mA, V_{in} = 12 V, V_{out} = 3.3 V (%)	82	89

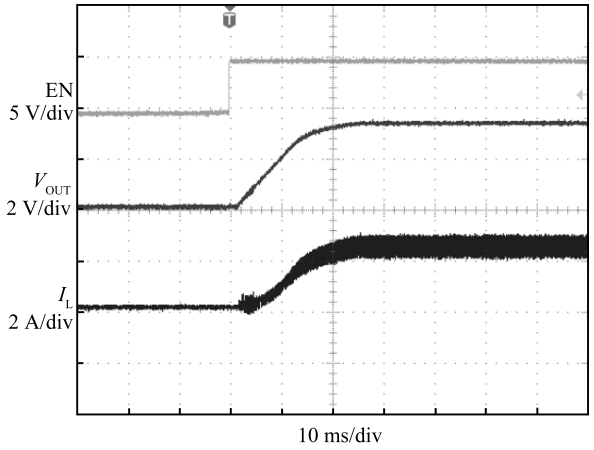

Fig. 6. Test waveform of soft-start. V_{in} = 12 V, V_{out} = 3.3 V, I_{out} = 2 A.

Table 2 shows a performance comparison of a fabricated chip and an MP484 with the same control mode under the conditions of 3.3 V output and room temperature.

Figure 6 gives the soft-start waveform through connecting an external 10nF capacitor under the condition of V_{in} = 12 V, V_{out} = 3.3 V, I_{out} = 2 A, which shows that the inductor current and output can realize start-up smoothly.

Figure 7 shows the result at light load for the case of load current with 30 mA. The converter will skip several cycles after working one or some period. The lower the load current, the more cycles the chip skips. It can be deduced that the chip operates in the skip mode and the ripple voltage is 22 mV.

Figure 8 shows the result at heavy load for the case of a load current with 2 A. It can be calculated that the chip operates steadily in PWM mode and the ripple voltage is only 16 mV.

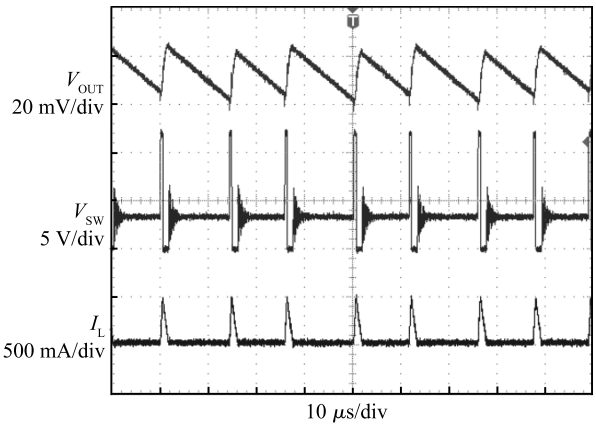

Fig. 7. Test waveform in skip mode. V_{in} = 12 V, V_{out} = 3.3 V, I_{out} = 30 mA.

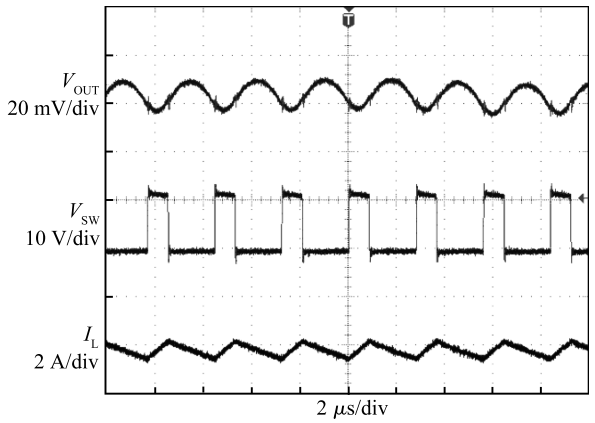

Fig. 8. Test waveform in PWM mode. V_{in} = 12 V, V_{out} = 3.3 V, I_{out} = 2 A.

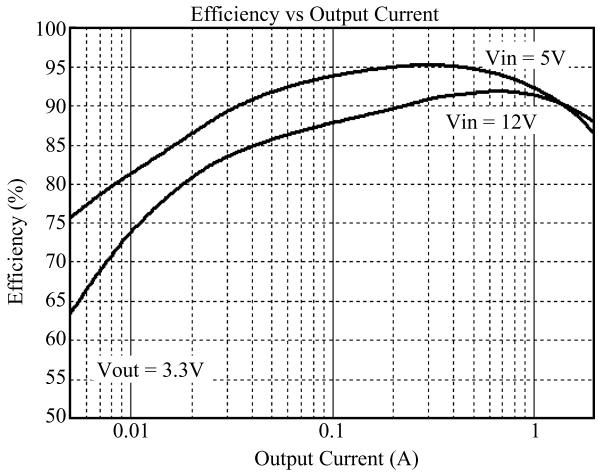

Fig. 9. Efficiency curve of the converter.

Figure 9 gives the efficiency curve of the converter. The result shows when the chip works between skip mode and PWM mode, the efficiency at light load has been improved greatly for reduced switching loss at this point. So the maximum efficiency can be up to 95.5% and the efficiency at 5 mA can be kept at 64%.

4. Conclusion

By automatically altering the modulation mode according to the load current, a buck DC–DC switching regulator with high efficiency is implemented using a 0.6 μm CDMOS technology. The test results show that the converter can switch between PWM mode and skip mode according to the load current. The maximum conversion efficiency is up to 95.5% and it can keep 64% at 5 mA of load current. This reduces the power dissipation at light load and standby state, which results in prolonging battery lifetime and standby time. The externally adjustable soft-start minimizes the inrush supply current and avoids the overshoot of output voltage at initial startup. Meanwhile, the circuit is simple and easy to implement, which has significance for the design of other mixed-signal circuits.

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