Mathematical modeling of nanoscale MOS capacitance in the presence of depletion and energy quantization in a poly-silicon gate

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Abstract: A model has been developed to study the effect of depletion and energy quantization at the poly-silicon/oxide interface on the behavior of a nanometer scale n-MOSFET. A model of inversion charge density, including the inversion layer quantization using the variation approach in the substrate, has also been produced. Using the exact calculations of the polygate potential under the depletion and quantization conditions, a C–V model has been developed. All the results have been compared with the numerical models reported in existing literature and they show good agreement.

Key words: BSIM; inversion layers; MOS devices; quantization; poly-depletion; poly-quantization
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1. Introduction

MOSFET modeling is facing difficulties in achieving the accurate description of extremely scaled down devices. The reason is that many complicated new phenomena are emerging that are not easy to describe. One such phenomenon arising out of down scaling the MOSFET is the failure of classical physics at the nanometer (nm) scale. As complementary metal oxide semiconductor (CMOS) technology scales down aggressively, it approaches a point where classical physics is not sufficient to explain the behavior of a MOSFET. At this classical physics limit, quantum mechanics has to be taken into account to accurately assess the overall performance of a MOSFET. Therefore, to predict the behavior of these devices and fabricate them at the nanometer scale, a thorough understanding of quantum mechanical effects (QME) is a must. Simple analytical models of MOSFETs including QME are needed for the computer-aided design of digital and analog integrated circuits at the nanometer scale containing thousands to millions of transistors on a silicon chip. One of the major effects in nanoscale MOSFETs is the inversion layer quantization. Accurate modeling of energy quantization in the substrate has received considerable attention, resulting in semi-analytical models. However, much less research has been carried out on energy quantization in poly-silicon gates at the nanometer scale. Those models developed so far are mainly numerical. Moreover, the oxide/poly-silicon interface has always been described classically. In this paper, an attempt is made to study the inversion layer quantization in the substrate by including the effect of inversion layer quantization and depletion in the poly-silicon gate also.

2. MOSFET models

First, the charge based models include the basic simulation program with integrated circuit emphasis (SPICE) Level 1, Level 2, Level 3 and BSIM (Berkeley short channel insulated gate field effect transistor model) models and the other advanced models, such as BSIM 4 and 5[1−5]. Second, the potential based models include the surface potential (SP) model, MOS model 11 and hiroshima starc insulated gate field effect transistor model (HiSIM) model[6−9]. Third, the conductance based models include the Enz, Krummenacher, Vittoz (EKV) model[10]. In the modeling research area, attempts are being made to include the QME in these standard models also. The other models that include the energy quantization effects though empirical in nature are the Hansch model[11], Van Dort model[11], inversion charge model[12], etc. A conclusion that can be inferred is that, although attempts are being made to include QME in MOSFET models all over the world in the integrated circuit (IC) industry, a model largely analytical in nature including QME in all sections of the nanoscale MOSFET is still to be developed.

3. Energy quantization modeling

Solving the Poisson equation in the inverted MOSFET substrate channel, we get the total charge density Q_s[13],

$$Q_s = -(2qN_a e_{si} e_o)^{1/2}\left[\phi_s + V_t e^{-2\phi_f/V_t}\left(e^{\phi_s/V_t} - 1\right)\right]^{1/2}, \tag{1}$$

where q is the electron charge, e_{si} is the silicon relative permittivity, e_o is the permittivity of free space, ϕ_s is the surface potential, ϕ_f is the Fermi potential, N_a is the substrate concentration and $V_t = kT/q$ is the thermal potential.

Similarly, the depletion charge Q_b is approximated as

$$Q_b = -(2e_{si}e_o q N_a \phi_s)^{1/2}. \tag{2}$$

Therefore, the inversion charge density Q_{inv} is given by Eqs. (1) and (2),

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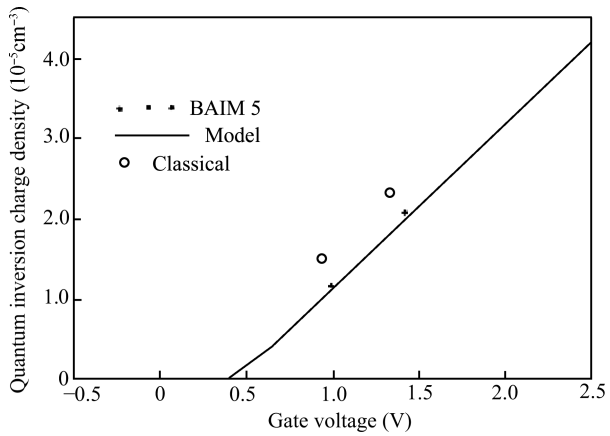
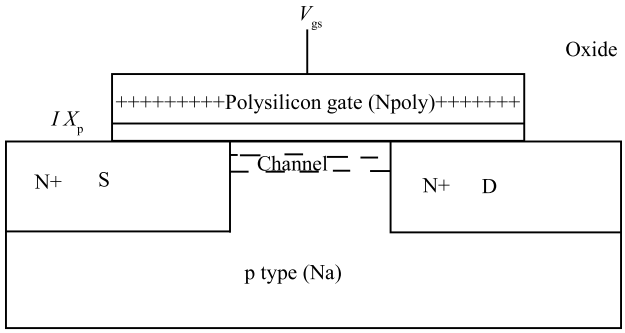


Fig. 1. Simulated results of quantum mechanical inversion charge density with gate voltage under the following model parameters: substrate doping 10^{18}cm^{-3} and oxide thickness 1.5 nm.



1. N+ (Source), N+ (drain) and the p type (substrate) are grounded.
2. t_{ox} = Oxide thickness = 5.0 nm.
3. +++++++ is the polydepletion width = X_p.
4. V_{gs} = Gate voltage.

Fig. 2. Poly-silicon gate depletion in a MOSFET.

$$Q_{\text{inv}} = -\gamma C_{\text{ox}}\left[\left(\phi_{\text{s}} + \frac{kT}{q}\exp\frac{q\left(\phi_{\text{s}} - 2\phi_{\text{f}}\right)}{kT}\right)^{1/2} - (\phi_{\text{s}})^{1/2}\right], \tag{3}$$

where γ is the body effect parameter = $(2qN_{\text{a}}e_{\text{si}}e_{\text{o}})^{1/2}/C_{\text{ox}}$ and C_{ox} is the unit area oxide capacitance (F/cm^2).

The main problem with Eq. (3) is that the surface-potential has to be evaluated explicitly in all the regions of electron inversion, and then only can Equation (3) be solved. An explicit solution has been evaluated in Ref. [14].

The wave function solution of Schrödinger's equation is given by using the variation approach[15],

$$\psi(x) = \frac{b^{3/2}x}{\sqrt{2}}\exp\left(\frac{-bx}{2}\right), \tag{4}$$

where b is a constant and given by

$$b = \left[\frac{48\pi^2 m^* q^2}{e_{\text{si}}\text{e}_{\text{o}}h^2}\left(0.33Q_{\text{inv}} + Q_{\text{dep}}\right)\right]^{1/3},$$

where m^* is the effective quantization mass.

The corresponding shift in the energy[14] is given by

$$E_{\text{o}} = \frac{3h^2b^2}{8m^*}. \tag{5}$$

Hence the shift in the surface potential is

$$\delta\phi = E_{\text{o}}/q. \tag{6}$$

Equation (6) is then included in the explicit surface potential expression given by[13]

$$\phi_{\text{s}} = f + a, \tag{7}$$

where

$f = \phi_{\text{f}} + 0.5\phi_{\text{swi}} - 0.5\left[(\phi_{\text{swi}} - 2\phi_{\text{f}})^2 + 0.0016\right]^{1/2}$, $a = 0.025\ln\left\{\left[x - y\left(1 + 100y^2\right)^{-1/2}\right]^2(0.16\gamma)^{-2} - 40f + 1\right\}$, $\phi_{\text{swi}} = \left[\left(V_{\text{gs}} - V_{\text{fb}} + 0.25\gamma^2\right)^{1/2} - 0.5\gamma\right]^2$, ϕ_{swi} is the weak inversion surface potential, $x = V_{\text{gs}} - V_{\text{fb}} - f$, and $y = \phi_{\text{swi}} - f$.

The quantum surface potential is given by

$$\phi_{\text{sqm}} = 2\phi_{\text{f}} + \delta\phi. \tag{8}$$

Using the surface potential model Eq. (7) in Eqs. (2) and (3), we can calculate explicitly the inversion charge density and the depletion charge density. The shift in the surface potential due to inversion layer quantization in the substrate can hence be calculated from Eq. (6). Using Eqs. (6)–(8), the quantum depletion charge density Eq. (2) and inversion charge density Eq. (3) can be evaluated for the quantum mechanical case.

The results in Fig. 1 match quite closely the BSIM 5 results[15]. The results show that the energy quantization leads to reduced inversion charge densities and increased electrostatic potential in the substrate. It has been analytically proved that the classical theory overestimates the value of the inversion layer charge density as compared to the quantum mechanical charge density.

4. Poly-silicon depletion

Poly-silicon gates are used in nanometer MOSFETs instead of metal gates in order to minimize the work function difference in the MOSFET, hence to reduce the flat band voltage and thus the threshold voltage. The poly-silicon gates are of n-type in n-MOSFETs. So, as the gate voltage is increased, the potential drops across the poly-silicon gate also. This causes the charge carriers in the gate to become depleted and expose the donor ions. This causes depletion in the gate and is called the poly-silicon gate depletion effect, as shown in Fig. 2. This potential thus reduces the effective voltage in the oxide and the substrate. The reduced voltage in the substrate causes less inversion charge and ultimately less drain current, which is a big cause of concern for the circuits.

Various models[16–18] have already been reported for estimating the poly-silicon gate depletion potential, but most of them are either empirical or too complex in a modeling procedure. The applied gate to source voltage is distributed across the poly-silicon gate, oxide and silicon substrate, as shown in Fig. 3.

Applying the voltage equality at the poly-silicon gate, we get

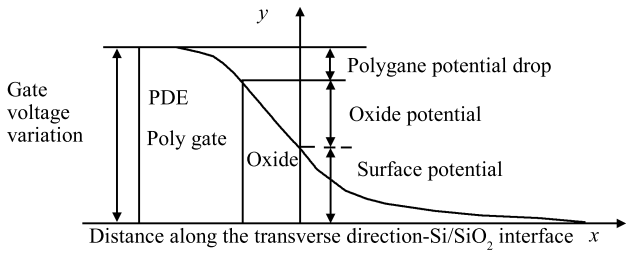


Fig. 3. Variation in potential in the poly-silicon gate.

$$V_{gs} = V_{ox} + V_{fb} + \phi_{sqm} + V_p, \tag{9}$$

where V_{ox} is the oxide potential, V_{fb} is the flat band voltage, V_p is the poly-silicon gate potential, V_{bs} is the Body voltage = 0 and $V_{gb} = V_{gs}$.

The poly-silicon gate potential is also expressed in terms of a polygate electrical field as

$$V_p = X_d E_p, \tag{10}$$

where E_p is the electric field in the poly-silicon gate and X_d is the depletion thickness in the poly-silicon gate.

Using gauss law by equating charges at the oxide and substrate interface, we get

$$e_{si} E_p = e_{ox} E_{ox}, \tag{11}$$

where e_{ox} is the relative permittivity of silicon oxide.

From Eqs. (9)–(11), we get

$$V_p = X_d (e_{ox}/e_{si}) E_{ox}. \tag{12}$$

Also, the oxide electrical field is

$$E_{ox} = V_{ox}/t_{ox}, \tag{13}$$

and the depletion depth in the uniformly doped polygate is

$$X_d = (2e_o e_p V_p / q N_{poly})^{1/2}. \tag{14}$$

From Eqs. (11)–(14), we get

$$V_p = 0.25\left[-\gamma_p + \left\{\gamma_p^2 + 4\left(V_{gs} - V_{fb} - \phi_{sqm}\right)\right\}^{1/2}\right]^2, \tag{15}$$

where γ_p is the body coefficient of the poly-silicon gate = $(2qe_o e_p N_{poly})$, e_p is the relative permittivity of polygate, and N_{poly} is the polygate doping concentration.

5. Poly-silicon energy quantization

When the gate voltage is applied, a potential drop across the poly-silicon gate causes depletion in the poly-silicon gate also. Due to strong electrical fields, the energy levels in the poly-silicon gate are also quantized at the poly-silicon gate/SiO_2 interface. Hence, there is a shift in the poly-silicon gate potential at the poly-gate/SiO_2 interface. This shift can be analyzed in a way similar to the shift in surface potential in the MOSFET channel using the variation approach. Various models have been reported in Refs. [19, 20], but most of these models are numerical and hence complex, and cannot be included in the circuit simulators.

The inversion charge density is not so high in poly-silicon gates as the doping concentration is very high-of the order of 1×10^{20} cm^{-3}. Neglecting inversion charge density in the poly-silicon gate, we get from Eq. (4) the change in poly-silicon gate potential (δV_p) due to energy quantization and hence adding the poly quantization potential in the surface poly potential. The shift in the poly gate potential can be evaluated as.

Equation (4) can be changed for the case of inversion layer quantization in the polygate as

$$\text{bpoly} = \left[\frac{48\pi^2 m^* q^2}{\varepsilon_{si}\varepsilon_0 h^2} Q_{dep}\right]^{1/3}. \tag{16}$$

The corresponding shift in the energy[14] is given by

$$E_{o\_poly} = \frac{3h^2 \text{bpoly}^2}{8m^*}. \tag{17}$$

Hence the shift in the surface potential is

$$\delta V_p = E_{o\_poly}/q. \tag{18}$$

The shift in polygate potential is evaluated as

$$V_{pQM} = V_p + \delta V_p. \tag{19}$$

So, Equation (16) affects the inversion charge density in the substrate as obtained in Eq. (18),

$$Q_{inv\_FQ} = C_{ox}\left(V_{gs} - V_{fb} - \phi_{sQM} - V_{pQM}\right) - Q_{bQM}, \tag{20}$$

where the depletion charge density considering inversion layer quantization in the substrate is

$$Q_{bQM} = -(2e_{si}e_o q N_a \phi_{sQM})^{1/2}. \tag{21}$$

Equation (14) is upgraded for the inversion layer quantization in the polygate also as

$$X_{dQM} = (2e_o e_p V_{pQM}/qN_{poly})^{1/2}. \tag{22}$$

The full capacitance model can be derived as

$$C_{fQM} = \left(1/C_{ox} + 1/C_s + 1/C_{pdqm}\right)^{-1}, \tag{23}$$

where C_{invqm} and C_{deplqm} are the inversion layer capacitance and depletion layer capacitance in the presence of inversion layer quantization in the substrate. C_{deplqm} is obtained by differentiating Eq. (2) and including $\phi_s = \phi_{sqm}$. Cinvqm is obtained by differentiating Eq. (3) and including $\phi_s = \phi_{sqm}$. The other term C_{pdqm} is $e_o e_{si}/X_{dqm}$, where X_{dqm} is found from Eq. (20).

The effect of poly-depletion and poly-quantization has been included in the calculation of C–V characteristics by effectively increasing the gate oxide thickness. Then, the computations are performed and the results are obtained. The results in Fig. 4 have been obtained using doping concentration $N_a = 1 \times 10^{18}$ cm^{-3} and the gate oxide = 5.0 nm and the poly-doping $N_{poly} = 1 \times 10^{20}$ cm^{-3}. The gate capacitance

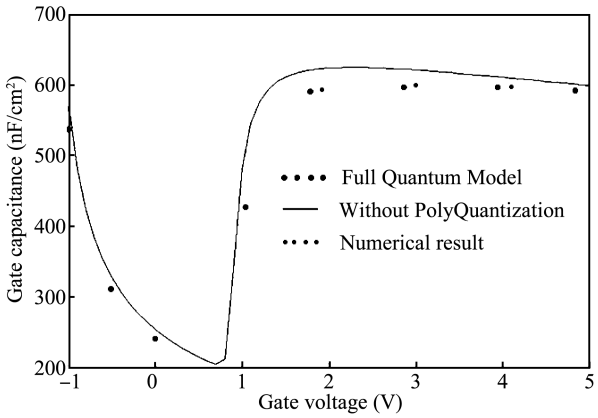


Fig. 4. Simulation results of gate capacitance, including poly-quantization and depletion, without poly-quantization but including poly-depletion and substrate quantization.

computed with energy quantization applied to both substrate and poly-silicon decreases from results obtained with substrate quantization only. This is due to the decreased inversion charge density in the substrate and increased poly-silicon potential. The results computed agree well with the existing numerical results, as reported in Ref. [19].

6. Conclusion

A detailed study has been carried out to evaluate the effect of poly-silicon depletion and quantization effects on C–V characteristics of a nanoscale MOSFET. Based on the variation approach, all these parameters have been derived. The total gate capacitance with quantum mechanical effects decreases as compared to the gate capacitance without considering poly-silicon quantization. This is due to a reduced charge density at the interface between the substrate and the oxide.

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