Nanoscale strained-Si MOSFET physics and modeling approaches: a review

Amit Chaudhry[1, †], J. N. Roy[2], and Garima Joshi[1]

(1 University Institute of Engineering and Technology, Panjab University, Chandigarh 91160047, India)
(2 Solar Semiconductor Private Limited, Hyderabad 91510001, India)

Abstract: An attempt has been made to give a detailed review of strained silicon technology. Various device models have been studied that consider the effect of strain on the devices, and comparisons have been drawn. A review of some modeling issues in strained silicon technology has also been outlined. The review indicates that this technology is very much required in nanoscale MOSFETs due to its several potential benefits, and there is a strong need for an analytical model which describes the complete physics of the strain technology.

Key words: mobility; SiGe; strained-Si; technology CAD
DOI: 10.1088/1674-4926/31/10/104001 **EEACC:** 2570

1. Introduction

CMOS (complementary metal oxide semiconductor) technology has contributed significantly to the microelectronics industry, thus playing an important role in the overall development of all countries. The performance and density of a CMOS chip can be improved through device scaling, which is inevitable as also propounded by Moore law, which says that the transistor density on a CMOS chip doubles approximately after every one and a half years[1, 2]. Continuing with Moore law, the gate length of the MOSFET will eventually shrink to 10 nm in 2015[3, 4]. Seeing the trend of down scaling, continuous improvements in the VLSI MOSFET device models are required so that the exact behavior of deep sub-micron and nanometer scaled MOSFETs can be described with accuracy.

For the last six decades, the semiconductor industry has been working hard to miniaturize the structure of the MOSFET to the nanoscale because of the need to accommode more transistors on a single chip, thus performing multi tasks and also resulting in the reduced cost of chip production. The success and progress of nanoelectronics depends on some technological changes to sustain CMOS technology. MOSFET physics and modeling is facing difficulties in achieving an accurate description of such scaled down devices. The reason is that many complicated new phenomena are arising, such as a reduction in carrier mobility, and the failure of classical physics in nanoscale MOSFETs. The accurate modeling of these adverse effects and their remedial actions is very much required. But as we scale down the MOSFET, carrier mobility decreases due to the high vertical electrical fields in the substrate. This reduces the speed of the device. To control these effects, strained silicon technology has evolved in the past few years as a replacement for silicon in substrates and also in poly-gates. It is perceived that strain engineering improves performance without further scaling of the gate dielectric thickness, junction depth or other transistor dimensions.

This paper is organized as follows. Section 2 deals with the types of stresses in microelectronic devices. Section 3 deals with the physics of a strained silicon MOSFET. Section 4 details the effect of strain on the silicon band structure. Section 5 deals with the standard models used in the industry for micro and nanoscale MOSFETs. Section 6 discusses some modeling issues in the strained silicon MOS technology. Conclusions are given in Section 7.

2. Stress

Stress that acts to shorten an object is called compressive stress, while stress that acts to lengthen an object is called tensile stress. Normally, it is perceived that the stress produces strain in that very direction. But the fact is that strain occurs in all directions with the application of unidirectional stress. Stress/strain relationships are guided by Hook's law. The following subsections illustrate the types of stresses occurring in semiconductor materials and devices.

2.1. Thermal mismatch stress

Thermal mismatch stress occurs when two materials with different thermal coefficients of expansion are heated and expand/contract at different rates. During thermal processing, thin film materials like polysilicon, SiO_2 and silicon nitride expand and contract at different rates compared to the silicon substrate according to their thermal expansion coefficients[5]. This causes a strain in the lattice of silicon substrate.

2.2. Intrinsic stress

Intrinsic stress or process stress is generated due to some process parameters and variations, i.e. film deposition rate, film thickness and temperature. During deposition, thin oxide films are either stretched or compressed to fit the substrate on which they are deposited[6].

2.3. Dopant induced stress

During the doping process, a local lattice expansion or contraction occurs due to the introduction of dopant atoms in the lattice. The amount of strain depends on the varying atomic sizes and bond lengths of the atoms of silicon and the dopant atoms[7].

† Corresponding author. Email: amit_ chaudhry01@yahoo.com
Received 14 April 2010, revised manuscript received 9 May 2010

2.4. Biaxial or global stress

A silicon film grown over a relaxed SiGe substrate produces biaxial stress. Due to the lattice mismatch between the Si and Ge atoms, tensile biaxial stress is generated in the over grown Si film, which enhances the performance of NMOS and PMOS. When a silicon film is deposited on a SiGe buffer layer, the film is forced to adopt the greater lattice constant of the SiGe, hence the Si film is under biaxial (longitudinal and transverse) tension[7].

2.5. Uniaxial or local stress

Uniaxial stress is caused by depositing a tensile silicon nitride capping layer on the MOSFET device structure. This approach is useful for NMOS devices, whereas for PMOS devices, the compressive strains are produced from the SiGe source and drains in the channel. As a result, the channel stress becomes dependent on the polysilicon gate. The lattice mismatch in the hetero-layer compresses the silicon lattice, which consequently compresses the device channel. Even the introduction of germanium into the source and drain of the MOSFET causes uniaxial strain in the direction parallel to the channel[7]. The biggest advantage of uniaxial strain is the achievement of higher mobility at relatively lower stress than in the case of biaxial stress.

The stress is also a favorable step in fabricating the MOSFET. This is due to the same chemical properties of strained Si and unstrained Si, and thus high quality gate oxides and good MOS interface properties are obtained easily by oxidizing strained-Si films.

3. Physics of strained MOSFETs

When a layer of a crystal is grown over another layer, a strain is developed in the upper layer due to the mismatch of the lattice constants of the two layers to achieve the high speeds without scaling down the devices. The strain is a very useful parameter in devices as carrier mobility significantly increases by altering the band structure at the channel. The alteration of the band structure in the channel layer provides a lower effective mass and also suppresses intervalley scattering, which is a prime cause of enhancement of carrier mobility and the drive current. The mobility becomes roughly twice that of a conventional Si substrate[8–10]. The conduction band splitting has been shown in Fig. 1. Each energy level of silicon is composed of six equal energy lobes in three dimensions. These are named as two perpendicular $\Delta 2$ states and four $\Delta 4$ states parallel to the plane. When a stress is applied, the $\Delta 2$ states and $\Delta 4$ states are split up into lower and higher energy states. This band alteration gives an alternate lower site for electrons to reside, i.e. $\Delta 2$. The difference in the energy valleys causes repopulation of the electrons in the lower mass valleys. The effective mass of electrons in the lower energy states is less than the higher states. Due to this, the electron mobility increases. Besides this, the inter-valley phonon scattering between the lower and upper states is suppressed due to the strain induced larger energy difference. The mathematical equation (1) proves this theory.

Mathematically, carrier mobility is described by

$$\mu = q\tau/m^*, \tag{1}$$

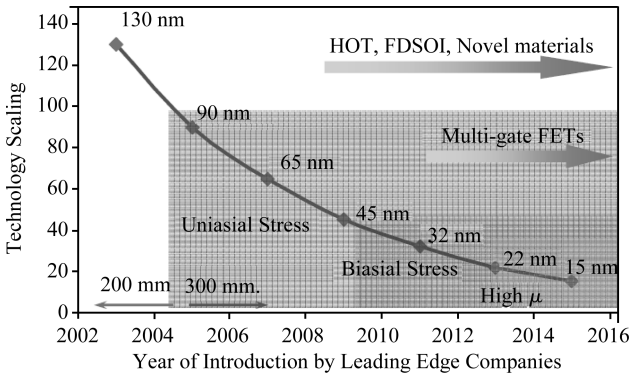

Fig. 1. Introduction of strain in various nanoscale technologies with the year of implementation[11].

where $1/\tau$ = scattering rate and m^* = conductivity effective mass.

The mobility is directly related to the carrier velocity 'v' and the applied external electric field 'E', as shown by

$$v = \mu E. \tag{2}$$

It can be seen that increasing the carrier mobility increases the velocity, which is directly proportional to the switching speed of the device and the drain current.

This process is especially useful at nanometer scales where the carrier mobility is affected the most, as explained earlier in Section 1. The introduction of different types of strains, i.e. biaxial and uniaxial in various technologies at nanoscale, is shown in Fig. 1.

4. Effect of strain on band structure

There are basically two types of band alignments in the lattice, such as type Ⅰ and type Ⅱ alignments. When a thin film with a larger lattice constant, e.g. SiGe, is grown on a substrate with a smaller lattice constant (e.g. silicon), the film maintains the in-plane lattice constant of the substrate and is under a biaxial compressive strain. This is known as the type Ⅰ band alignment where virtually all the entire band alteration occurs in the valence band only and with minimal band alteration in the conduction band. This type of structure is favorable for hole confinement and is a basic alignment for p-MOSFETs.

Meanwhile, a smaller lattice constant silicon epilayer will be under biaxial tension when grown on a larger lattice constant relaxed-SiGe substrate. In this case, type II band alteration occurs and the structure has several advantages over the more common type I band alignment, as a large band alteration is obtained in both the conduction and valence bands, relative to the relaxed-SiGe layer[12]. This allows both electron and hole confinements, making it useful for both n- and p-type devices for strained-Si/SiGe based CMOS technology. Since strained-Si provides type 2 alignment, a significant improvement in carrier mobility can be achieved. Strained silicon is used to increase n-type and p-type MOSFET drive currents by 10% and 25%, respectively[12].

For hole transport, the valence band structure of silicon is much more complex. The valence band comprises three bands: heavy-hole, light-hole and split-orbit bands[13–16], as shown in

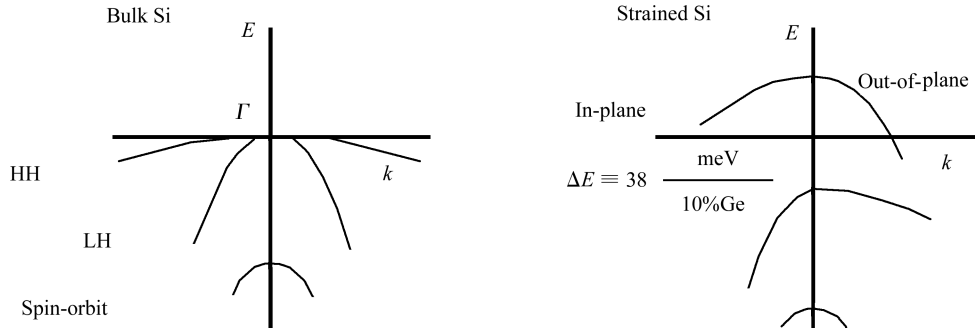

Fig. 2. Energy band splitting due to biaxial strain in valence bands.

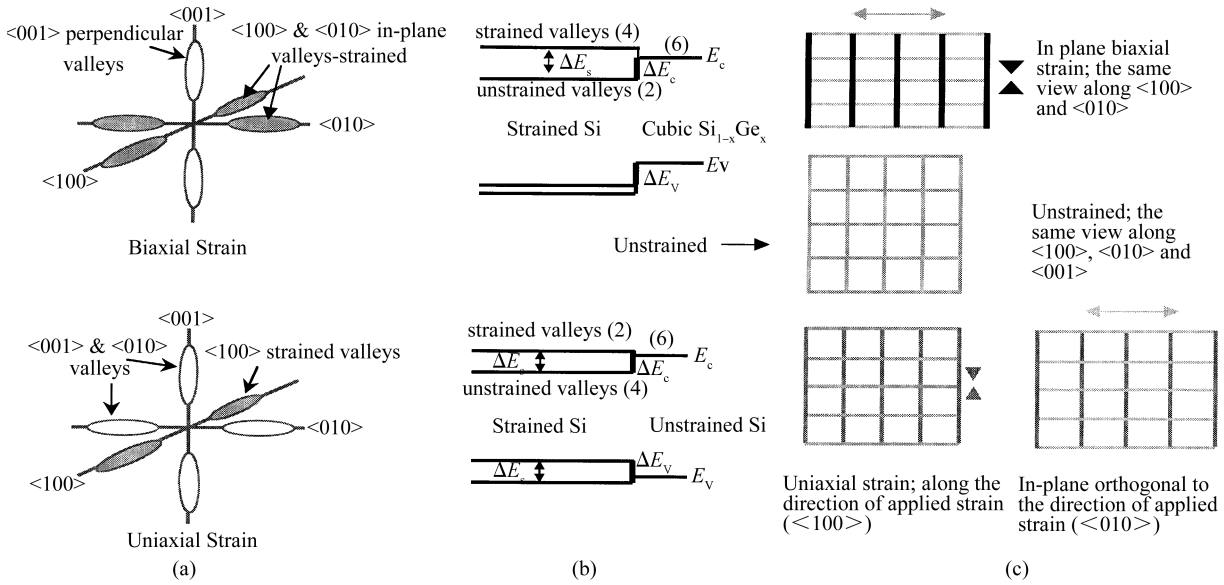

Fig. 3. Comparison of (a) biaxial and (b), (c) uniaxial strains.

Fig. 2. Application of strain causes high band warping. When the strain is applied, the valence band energy states get split up into light-hole and heavy-hole bands. The holes now occupy the low energy states, which reduces their effective mass. This increases mobility under strain. A detailed description of uniaxial and biaxial strains is given in Figs. 3(a), 3(b) and 3(c).

Besides some merits of strain technology, there are some drawbacks in this technology to actually implement it in CMOS fabrication process. The main problems, such as integration of strained technology with the existing unstrained silicon technology, and reduction in the threshold voltage and increase in the off state currents in the nanoscale MOSFETs[17], need to be resolved.

5. Current standard MOSFET models

Some semiconductor industry standard compact models, such as charge, potential and conductance based models, are reviewed here.

5.1. Charge based MOSFET model

The charge based modeling approach is one of the basic and primitive modeling approaches. It is based on the computation of the inversion charge density in the MOSFET channel in terms of the terminal voltages, i.e. gate and drain voltages[18, 19]. This model is a regional model because it explains the behavior of the MOSFET separately in all regions of its operation. So, these models require smoothing parameters, they are somewhat empirical in the interfacing regions and, thus the device behavior is not described accurately.

The prominent charge based models are level 1, level 2, level 3, BSIM1, HSPICE level 28, BSIM2[19], BSIM3, BSIM4[19] and BSIM5. BSIM 5 is used for sub-100 nm CMOS circuit simulation[20]. This model is applicable to deep submicron region, and attempts have been made to include the modeling of strained silicon technology in the latest SPICE models. BSIM4 considers the influence of stress on mobility, velocity saturation, threshold voltage, body effect and DIBL effect. But the equations expressed are mostly empirical and no analytical models have been given. Moreover, no proper stress/strain relationships with the device parameters have been given.

5.2. Potential based MOSFET model

This model approach is more accurate than the charge based models. It is based on the calculation of the potential in the channel of a MOSFET to determine the I–V and C–V characteristics. Some of the models based on this approach are SP models by Penn-state University, USA[21],

Table 1. Comparison of two basic compact MOSFET models.

Property	Charge based models	Potential based models
Strain silicon modeling	Basic model analytical, but an empirical correction of strain parameters and equations	Basic model analytical, but no modeling of strain has been done

HISIM (Hiroshima-University, STARC IGFET model)[22–24] valid down to sub-100 nm MOSFETs. This model is applicable to the deep sub-micron region and attempts have been made to include the modeling of strained silicon technology.

5.3. Conductance based MOSFET model

This modeling approach is suitable for low power, short channel applications for analog design. It is known as the EKV (Enz–Krummenacher–Vittoz) model[25], which has been developed by the Swiss Federal Institute of Technology, Switzerland. This model keeps the substrate as the reference rather than the source, as observed in the potential based and charge based models. Due to its complexity, it is much less used for modeling purposes. Moreover, no stress modeling has been done in this model.

In all the approaches mentioned above, attempts have been made to model MOSFETs for strained silicon technology. But most of the models that have been proposed are either empirical or semi empirical in nature. Therefore, there is a need for a more physics based approach to accurately explain the behavior of the device. Table 1 shows the comparison summary of some of the advanced models discussed above. The table clearly shows that though most of the industry standard models include the strained silicon technology, these models are not capable of predicting the complete model of the nanoelectronic devices. This is because the models include a modeling process that is empirically, semi-empirically or numerically unsuitable for circuit simulation purposes.

6. Modeling issues in strained silicon technology

6.1. Electron mobility

The electron mobility models in unstrained silicon technology need to be upgraded to accommodate effects such as band alterations, scattering and mass calculations, thickness of the strained silicon and SiGe layers, and germanium concentration dependence. Various empirical models are available in the existing compact models[26]. A complete analytical model incorporating strain parameters still needs to be developed.

6.2. Hole mobility

The hole mobility models in unstrained silicon technology need to be upgraded to accommodate effects such as valence band alterations, scattering and mass calculations, thickness of the strained silicon and SiGe layers, and germanium concentration dependence. Various numerical models are available in existing compact models[27]. But a complete analytical model incorporating strain parameters still needs to be developed.

6.3. Threshold voltage shift

The shift in the surface potential due to the strain changes the threshold voltage. Important parameters, such as the effect of strain, short-channel effects, strained-silicon doping, strained-silicon thin-film thickness and gate work function need to be modeled analytically to predict the impact of strain on the threshold voltage.

6.4. Energy quantization in strained Si

Energy quantization effects in silicon substrates at nanoscale MOSFETs also influence the strained silicon MOSFETs. The shift in the inversion charge centroid in strained silicon depends on the germanium mole fraction, the doping concentration and the width of the strained-Si layer. Various numerical and empirical models[28–31] have been reported in the literature but much less work has been done to model the problem analytically.

6.5. Poly SiGe gate

SiGe polygate MOSFETs exhibit a reduced poly-gate-depletion effect. Poly-SiGe films are grown at lower temperatures and the work function of these films can be adjusted by varying the Ge concentration[32, 33]. The grain size, grain orientations, defects and surface roughness are important characteristics for applications of the SiGe films. Proper modeling of these factors is needed to evaluate their effect on the electrical characteristics of the device.

6.6. Tunneling currents in strained Si

As the MOSFETs are scaled down to nanometer levels, the gate oxide leakages tend to be very high. Various numerical and empirical models[34–37] have been reported in the literature to study gate oxide leakage in strained silicon devices but much less work has been done to model the problem analytically.

6.7. Hybrid orientation technology

Dual channel hetero-structure CMOS devices use both n-type and p-type channels. In the case of Si ⟨001⟩, the hole mobility is much less than the electron mobility[38, 39]. It requires the width of p-type regions at least two times larger than the n-type channels to generate the desired drive current in CMOS circuits. If we fabricate p-type channels in Si ⟨110⟩, the hole mobility is increased, which gets further boosted if tensile strains are applied. This process yields to some extent the driving capability of both types of transistors to be the same without increasing the size of the p-MOS transistors. A thorough understanding of these devices is required using a compact model, which still needs to be developed.

7. Conclusion

In this paper, a review of strained Si MOSFET physics, modeling issues and approaches has been carried out. Strained silicon may be perceived as a potential technology to cure the problems of nanoscale transistors, but there is a strong need to understand its physics, its problems (like integration with the existing technology) and a suitable physics based analytical model which accurately describes the strained silicon MOSFET behavior at the nanometer scale in all regions of its operation.

Acknowledgments

The authors thank the Director, UIET, Panjab University,

Chandigarh, India for allowing them to carry out the work. The authors would like to thank Panjab University, Chandigarh, India for providing an excellent research environment to complete this work. The authors wish to thank all individuals who have contributed directly or indirectly to complete this research work. The authors would like to thank the Department of information technology, New Delhi, India for financial assistance for the project on nanoscale and low temperature electronics.

References

[1] Schaller R R. MOORE'S law: past, present and future. IEEE Spectrum, June 1997: 53

[2] Moore G E. Cramming more components onto integrated circuits. Proc IEEE, 1998, 86(1): 82

[3] Zeitoff P M, Chung J E. A perspective from the 2003 ITRS-MOSFET scaling trends, challenges and potential solutions. IEEE Circuits and Devices Magazine, 2005: 4

[4] International technology roadmap for semiconductors (ITRS). Semiconductor International Association, 2003

[5] Senturia S D. Microsystem design. Norwell, MA: Kluwer Academic Publishers, 2001

[6] Freund L B, Suresh S. Thin film materials: stress, defect formation and surface evolution. Cambridge, UK: Cambridge University Press, 2003

[7] Maiti C K, Chattopadhyay S, Bera L K. Strained silicon heterostructure field effect transistors. New York: Taylor and Francis, 2007

[8] Vogelsang T, Hofmann R K. Electron transport in strained Si layers on $Si_{1-x}Ge_x$ substrates. Appl Phys Lett, 1993, 63: 186

[9] Takagi S, Hoyt J, Welser J, et al. Comparative study of phonon-limited mobility of two-dimensional electrons in strained and unstrained Si metal–oxide–semiconductor field-effect transistors. J Appl Phys, 1996, 80: 1567

[10] Welser J, Hoyt J, Takagi S. Strain dependence of the performance enhancement in strained-Si n-MOSFETs. IEDM Technical Digest, 1994: 373

[11] http://www.sematech.org

[12] Armstrong G, Maiti C. Strained-Si channel heterojunction p-MOSFETS. Solid-State Electron, 1998, 42(4): 487

[13] Fischetti M V, Ren Z, Solomon P M, et al. Six-band k·p calculation of the hole mobility in silicon inversion layers: dependence on surface orientation, strain, and silicon thickness. J Appl Phys, 2003, 94: 1079

[14] Fischetti M V, Gámiz F, Hänsch W. On the enhanced electron mobility in strained-silicon inversion layers. Appl Phys Lett, 2002, 92: 7320

[15] Fischetti M V, Laux S E. Band structure, deformation potentials, and carrier mobility in strained-Si, Ge, and SiGe alloys. J Appl Phys, 1996, 80: 2234

[16] Oberhuber R, Zandler G, Vogl P. Subband structure and mobility of two-dimensional holes in strained-Si/SiGe MOSFETs. Phys Rev B, 1998, 58: 9941

[17] Chuang C, Bernstein K, Joshi R V, et al. Scaling planar devices focussing on planar device structures and strained silicon for handling silicon issues in the deep sub-100 nm regime. IEEE J Electron Circuits Devices, 2004, 20(1): 16

[18] Foty D. MOSFET modeling with SPICE, principles and practice. Prentice Hall, 1997

[19] Foty D. Perspectives on analytical modeling of small geometry MOSFETs in SPICE for low voltage/low power CMOS circuit design. Journal of Analog Integrated Circuits and Signal Processing, 1999, 21: 229

[20] Xi X, He J, Dunga M, et al. BSIM5 MOSFET model. Proc 7th International Conference on Solid-State and Integrated Circuits and Technology, Beijing, China, 2004: 920

[21] Gildenblat G, Wang H, Chen T L, et al. SP: an advanced surface-potential-based compact MOSFET model. IEEE J Solid-State Circuits, 2004, 39(9): 1394

[22] Miura-Mattausch M, Ueno H, Mattausch H J, et al. HiSIM: self-consistent surface-potential MOS model valid down to sub-100 nm technologies. MSM Workshop, April 2002

[23] HiSIM 1.1.1 User's manual. Semiconductor Technology Academic Research Centre (STARC)

[24] Suetake M, Suematsu K, Nagakura H, et al. HiSIM: a drift diffusion-based advanced MOSFET model for circuit simulation with easy parameter extraction. Proc International Conference Simulation of Semiconductor Processes and Devices, SISPAD, Seattle, WA, USA, 2000: 261

[25] Enz C, Krummenacher F, Vittoz E. An analytical MOS transistor model valid in all regions of operation and dedicated to low-voltage and low-current applications. Journal of Analog Integrated Circuit Signal Processing, 1995, 8: 83

[26] Walczak J, Majkusia B. Electron mobility and drain current in strained-Si MOSFET. Journal of Telecommunications and Information Technology, March 2007: 84

[27] Neizvestnyi I, Gridchin V. The use of stressed silicon in MOS transistors and CMOS structures. Journal of Russian Microelectronics, 2009, 38(2): 83

[28] Roldan J, Gamiz F, Lopez-Villanueva J A, et al. Strained-Si on $Si_{1-x}Ge_x$ MOSFET inversion layer centroid modeling. IEEE J Electron Devices, 2001, 48(10): 2447

[29] Yang R, Jinsheng L, Jing T, et al. Simulation and comparison of MOS inversion layer quantum mechanics effects in SiGe p-MOSFET and Si PMOSFET. Microelectron J, 2004, 35(2): 145

[30] Hargrove M, Hargrovey M J, Henningy A K, et al. Quantum mechanical modeling of the charge distribution in a $Si/Si_{1-x}Ge_x/Si$ p-channel MOSFET. IEEE Proceedings of Electron Device Meeting, 2001: 30.3.1

[31] Nguyen C, Pham A T, Jungemann C, et al. Study of charge carrier quantization in strained Si n-MOSFETs. Journal of Material Science in Semiconductor Processing, 2005, 8: 363

[32] Rodrfguez A, Rodrıguez A, Olivares T, et al. Nucleation site location and its influence on the microstructure of solid-phase crystallised SiGe films. J Appl Phys, 2001, 90: 2544

[33] Anteney I M, Parker G J, Ashburn P, et al. Electrical properties of *in situ* phosphorus- and boron-doped polycrystalline SiGeC films. Appl Phys Lett, 2000, 77: 561

[34] Yan L, Olsen S H, Kanoun M. Gate leakage mechanisms in strained Si devices. J Appl Phys, 2006, 100: 104507

[35] Yang X, Lim J, Sun G, et al. Strain induced changes in the gate tunneling currents in p-channel metal–oxide–semiconductor field effect transistors. Appl Phys Lett, 2006, 88: 052108

[36] Yan L, Olsen S H, Escobedo-Cousin E O, et al. Improved gate oxide integrity of strained Si n-channel metal oxide silicon field effect transistors using thin virtual substrates. J Appl Phys, 2008, 103: 094508

[37] Rocette F, Garros X, Reimbold G, et al. Strain sensitivity of gate leakage in strained-SOI nMOSFETs: a benefit for the performance tradeoff and a novel way to extract the strain induced band offset. J Microelectron Eng, 2009, 86: 1897

[38] Maiti T, Satyasopan M, Pinaki C, et al. CMOS performance enhancement in hybrid orientation technologies. Journal of Computational Electronics, 2008, 7: 181

[39] Yang M, Chan V, Chan K, et al. Hybrid orientation technologies. IEEE Trans Electron Devices, 2006, 53: 965