Short locking time and low jitter phase-locked loop based on slope charge pump control*

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Abstract: A novel structure of a phase-locked loop (PLL) characterized by a short locking time and low jitter is presented, which is realized by generating a linear slope charge pump current dependent on monitoring the output of the phase frequency detector (PFD) to implement adaptive bandwidth control. This improved PLL is created by utilizing a fast start-up circuit and a slope current control on a conventional charge pump PLL. First, the fast start-up circuit is enabled to achieve fast pre-charging to the loop filter. Then, when the output pulse of the PFD is larger than a minimum value, the charge pump current is increased linearly by the slope current control to ensure a shorter locking time and a lower jitter. Additionally, temperature variation is attenuated with the temperature compensation in the charge pump current design. The proposed PLL has been fabricated in a kind of DSP chip based on a 0.35 μm CMOS process. Comparing the characteristics with the classical PLL, the proposed PLL shows that it can reduce the locking time by 60% with a low peak-to-peak jitter of 0.3% at a wide operation temperature range.

Key words: phase-locked loop; loop bandwidth; phase margin; phase frequency detector; slope charge pump current
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1. Introduction

The PLL is one of the most important function blocks in modern microprocessors. Among the various PLLs, the charge pump PLL (CPPLL) has the widest pull-in range and the smallest zero capture phase error, which has become the mainstream in recent years. Nowadays, high performance clock synthesizers are often required to fast lock-in time and low jitter. Meanwhile, fast frequency switching of frequency synthesizers is one of the challenges in modern wireless communications. How fast the communication channels can be switched and how fast the system can be turned on/off depend on the lock-in time. In order to realize the fast settling process of the PLL frequency synthesizer, dynamic loop bandwidth methods were proposed in Refs. [1–4]. However, these methods cannot avoid the design tradeoff between the locking time and the phase noise or reference spurs. Other, fractional-N PLL frequency synthesizers were also proposed in Ref. [5], but the additional fractional spurs and high-frequency quantization noise limit the increase in loop bandwidth, hence the locking speed.

In this paper, a fast-settling frequency synthesizer with fast start-up and slope charge pump current control is presented, on the basis of which, a better stability, a shorter locking time and lower jitter are obtained. A novel linear charge pump current, especially with the temperature compensation, is designed for an auxiliary tuning loop to accelerate the lock-in, dependent on the output of the PFD. Also, the output of the loop filter can be preset with a small initial voltage by the fast start-up circuit. The proposed PLL has been fabricated in a kind of DSP chip based on a 0.35 μm CMOS process, and the comparison of the performances of the other designs are presented, which shows the improved characteristics of our design.

2. Locking time, jitter versus loop bandwidth

A conventional CPPLL consists of five major blocks: the phase frequency detector (PFD), the charge pump (CP), the loop filter (LF), the voltage controlled oscillator (VCO) and the frequency divider. As is shown in Fig. 1, for the 3rd-order CPPLL, using linear approximations, the open loop transfer function of the PLL can be calculated by:

$$H_{\text{open}}(s) = \frac{K_\phi K_{\text{VCO}} Z(s)}{Ns}, \tag{1}$$

$$H_\phi = \frac{I_{\text{P}}}{2\pi}, \tag{2}$$

$$Z(s) = \left(R_1 + \frac{1}{sC_1}\right) // \frac{1}{sC_2}, \tag{3}$$

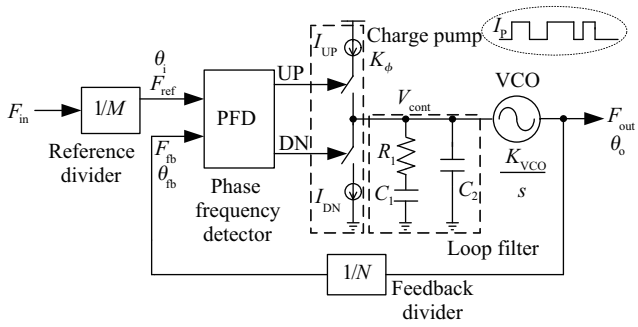

Fig. 1. Structure of a conventional CPPLL.

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where K_ϕ is the gain of CP, $K_{\rm VCO}$ is the gain of VCO, and $I_{\rm P}$ is the charge pump current. $Z(s)$ is the gain of LF. Then we can get the close loop bandwidth transfer function:

$$H_{\rm close}(s) = \frac{\dfrac{I_{\rm P}K_{\rm VCO}}{2\pi N(C_1+C_2)}(1+sNR_1C_1)}{s^2+s\dfrac{I_{\rm P}K_{\rm VCO}R_1C_1}{N(C_1+C_2)}}. \quad (4)$$

Defining the natural pulsation $\omega_{\rm n}$ and the damping factor ζ as

$$\omega_{\rm n} = \sqrt{\frac{I_{\rm P}K_{\rm VCO}}{2\pi N(C_1+C_2)}}, \quad \zeta = \frac{R_1C_1}{2}\sqrt{\frac{I_{\rm P}K_{\rm VCO}}{2\pi N(C_1+C_2)}}, \quad (5)$$

then we can get the loop bandwidth $\omega_{\rm c}$:

$$\omega_{\rm c} = 2\omega_{\rm n}\zeta, \quad (6)$$

$$\omega_{\rm c} = R_1C_1\frac{I_{\rm P}K_{\rm VCO}}{2\pi N(C_1+C_2)}. \quad (7)$$

Now consider a PLL which is initially locked at frequency 0, and then the system is changed to cause the PLL to switch to frequency $f_{\rm out}$. This is equivalent to changing the reference frequency from 0 to $f_{\rm out}/N$. Using inverse Laplace transforms, the time frequency response is obtained, from which the lock time of the PLL is derived as

$$t_{\rm locking} = \frac{-\ln\left(\dfrac{k}{f_{\rm out}}\sqrt{1-\zeta^2}\right)}{\omega_{\rm n}\zeta}, \quad (8)$$

where $t_{\rm locking}$ is the locking time and k corresponds to the maximum tolerance of the frequency at which the PLL is considered to be locked. So, the lock time is inversely proportional to the loop bandwidth $\omega_{\rm c}$, which is proportional to $I_{\rm P}$. In other words, to modulate the lock time we can modulate the charge pump current and so the loop bandwidth.

Depending on the close loop transfer function, the PLL phase detector and reference signal are typically the dominant noise source within the loop bandwidth, and the noise of the VCO is often the dominant noise source outside the loop bandwidth. Larger charge pump gains yield lower leakage dominated spurs at the critical frequency. When the charge pump is in the tri-state state, it is ideally high impedance. However, there will be some parasitic leakage through the CP, VCO, and LP capacitors. Of these leakage sources, the CP tends to be the dominant one. In addition to the discussion above, the input jitter is another critical source of output jitter of the PLL[6]. Since every jitter source has a certain bandwidth in the PLL loop, we can reduce the loop bandwidth to reject these jitter. But this method for low jitter is in contradiction to the way to achieve a short locking time. So, in this paper, there is a solution to this problem dependent on the adaptive loop bandwidth. When the output frequency is out of the nominal state, the charge pump current is increased to reduce the charging time or discharging time. But when the output frequency is captured, the charge pump current is kept at a certain value to obtain low jitter.

As discussed above, there are several advantages compared to other solutions shown in Refs. [1–5]: (1) The charge pump current is adjusted by the output frequency state adaptively to obtain a very short locking time. (2) Once the output frequency is normal, the charge pump current can return the fixed value to achieve low jitter. These two crucial problems can be solved at the same time. (3) The circuit introduced occupies only a small part of the whole chip, as shown in the fourth part. (4) With temperature compensation, an accurate current with a zero coefficient of temperature is generated to ensure a short locking time and low jitter in a wide operating temperature.

3. Proposed PLL architecture

3.1. System design

From Section 2, by the nature of the PLL, its locking time and noise are constrained by the bandwidth. It is often difficult to design a PLL that can achieve a fast locking time with low jitter due to the tradeoffs between the loop bandwidth and the phase noise. One method to reduce the locking time is to vary the PLL bandwidth as a function of the desired output frequency. Several techniques for adaptive bandwidth PLLs have been developed[7–9]. However, complicated filter structures, such as active filters and current model filters, were used in those designs. In this paper, a fast start-up and a slope current are added to the output and input of the charge pump linearly, which is controlled by the output of the PFD. The wider the pulse of the charging current is, the larger the slope current is, which will lead to the fast response to $V_{\rm cont}$. The proposed architecture is shown in Fig. 2. With this technique, we can optimize the loop performance, including the damping factor and the loop gain, over the entire operating frequency range by the variable loop bandwidth.

$$\omega_{\rm n} = \sqrt{\frac{(I_{\rm b}+I_{\rm slope})K_{\rm VCO}}{2\pi N(C_1+C_2)}}, \quad (9)$$

$$\zeta = \frac{R_1C_1}{2}\sqrt{\frac{(I_{\rm b}+I_{\rm slope})K_{\rm VCO}}{2\pi N(C_1+C_2)}}, \quad (10)$$

$$\omega_{\rm c} = R_1C_1\frac{(I_{\rm b}+I_{\rm slope})K_{\rm VCO}}{2\pi N(C_1+C_2)}, \quad (11)$$

where $I_{\rm b}$ is the basic charging current, which is to ensure the minimum charge pump current. $I_{\rm slope}$ is the slope current controlled by the PFD, which is important to control the adaptive bandwidth. Also, the fast start-up circuit is very useful in a short locking time. Its operating principle is described in the following sections.

3.2. Fast start-up circuit design

To reduce the locking time, firstly, we designed a novel fast start-up circuit, which decreases the locking time and improves the transient response. When the PLL is enabled, the output of the loop filter $V_{\rm cont}$ will be charged to a certain level to start up the voltage controlled oscillator, so, the rising time of $V_{\rm cont}$ is a part of the locking time. Since $V_{\rm cont}$ is an important point in the start-up of the PLL, we can give an initial value to reduce the rising time of $V_{\rm cont}$ directly. The fast start-up circuit can be designed as shown in Fig. 3. The core circuit is the loop filter composed of R_1, C_1 and C_2. $V_{\rm EN}$ is the enable signal of this block. If the fast start-up function is needed, $V_{\rm EN}$ is

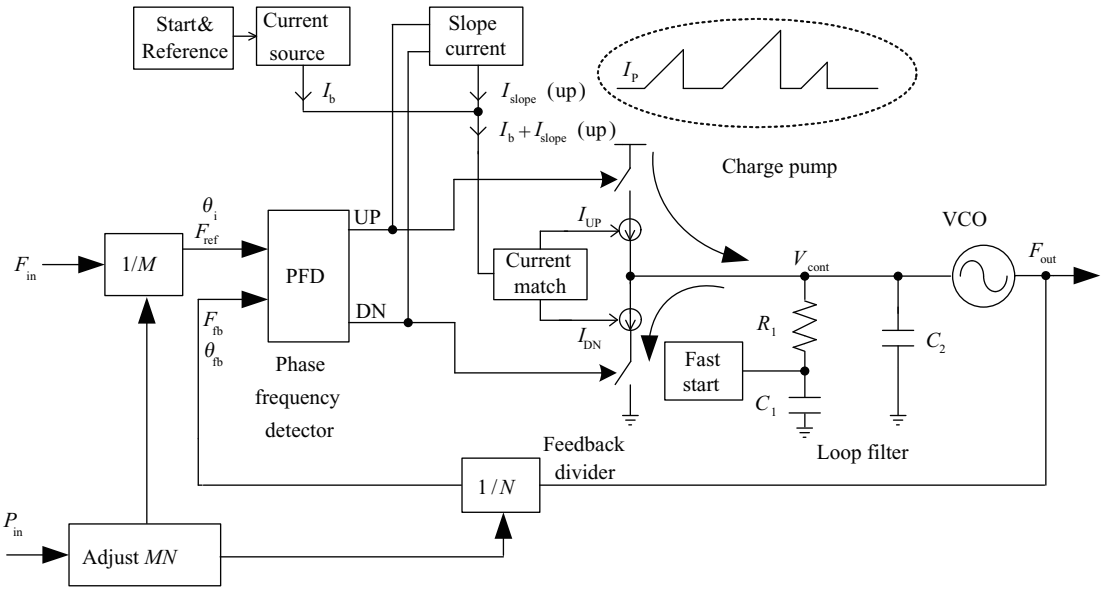


Fig. 2. Diagram of the proposed PLL.

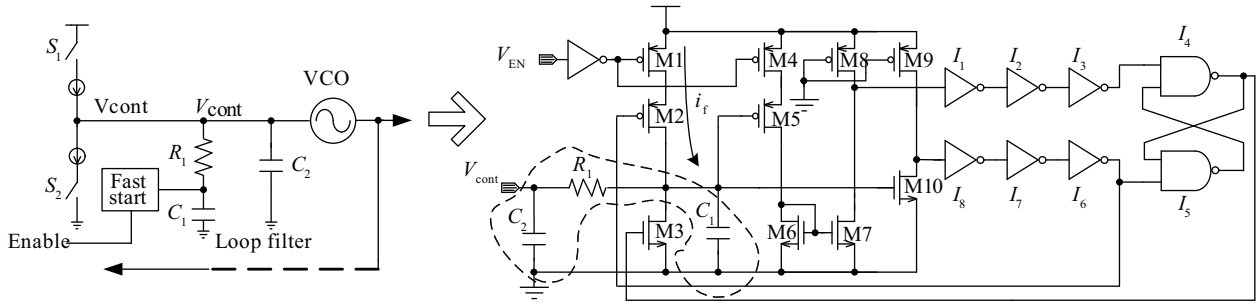


Fig. 3. Schematic of the fast start-up circuit.

set to a lower value. It will be disenabled by setting V_{EN} to a higher value. When the fast start-up is enabled, the transistors M1 and M4 are turned on. Because of the initial low voltage across the capacitor C_1, the transistor M5 is turned on to set the low level at the input of I1. The transistor M10 is turned off to set the high level at the input of I8. Through the inverter I6 and I7, M2 is conducted to charge the capacitor C_1 by the current i_f. Depending on this technology, the voltage V_{cont} can be started quickly. With the voltage across the capacitor C_1 increasing, by the point the voltage V_{cont} equals the power supply subtracted by an over driving voltage and a threshold, the transistors M5 and M3 are turned on to clamp the high level of the voltage V_{cont}. The simulation results of the fast start-up circuit are shown in Fig. 4. It can be seen that the start-up of the voltage V_{cont} is only about 15 ns at a temperature of –55 ℃/25 ℃/125 ℃. Also, the verification of the fast start-up circuit in the loop is presented in Fig. 10. It is obvious that V_{cont} rises quickly in the capture process.

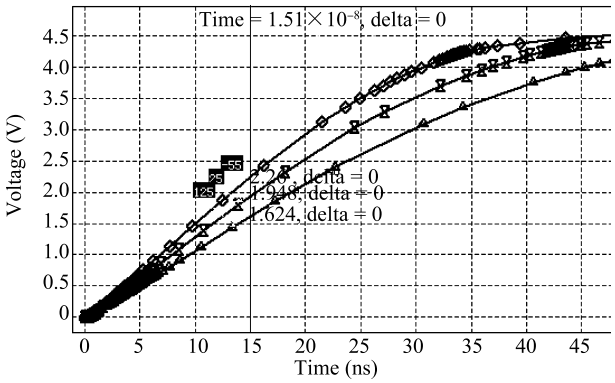


Fig. 4. Waveform of the fast start-up at different temperatures.

3.3. Slope charge pump circuit design

Figure 5 shows the schematic of the proposed slope charge pump circuit which includes the blocks of the start and current reference generator, the phase frequency detector, the minimum pulse indictor, the slope current control and the charge pump.

This phase frequency detector circuit has a monotonic phase error transfer characteristic over the range of input phase error up to ±1 cycle (360°), which is also insensitive to the duty cycle and to generate UP, UPB, DN and DNN pulses that have a certain minimum width, even when the phase difference is zero. Additionally, the PLL is allowed to track small changes in the reference signal while the loop is in lock. Any dead-zone will result in additional input tracking jitter. In order to maintain equal and short duration pulses for the UP and DN

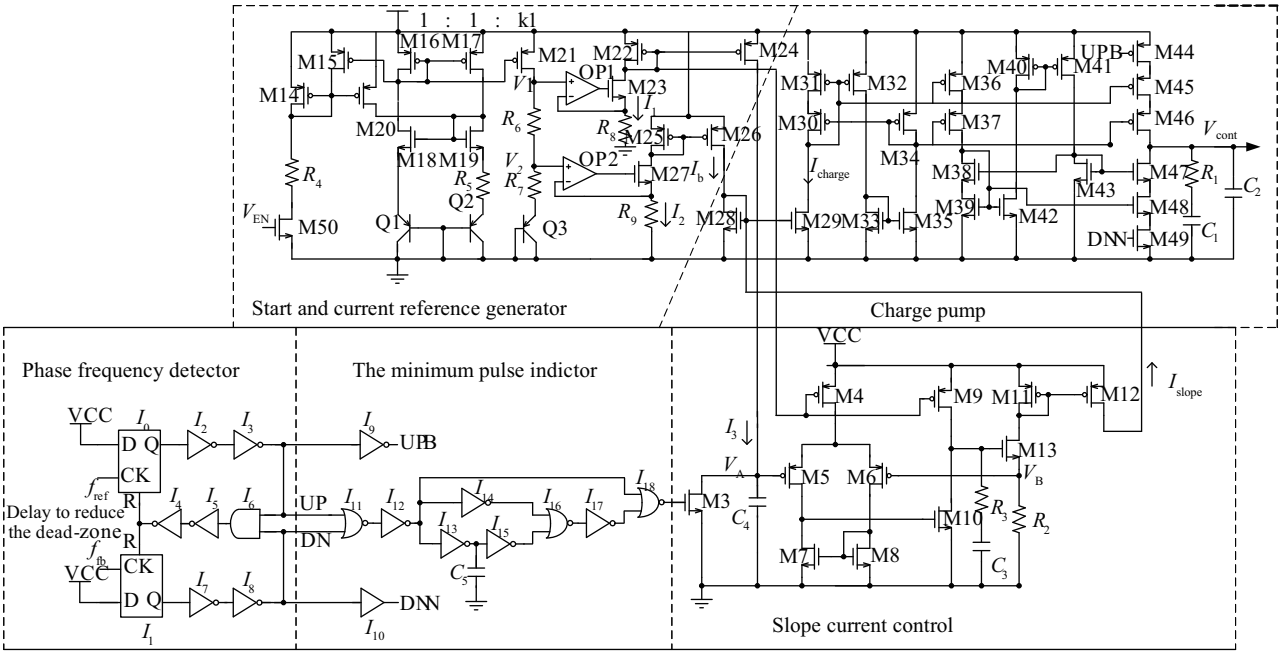


Fig. 5. Circuit of the slope charge pump current.

output signals, some delay is introduced in the reset path using additional inverters and a buffer, as shown in Fig. 5.

Because the temperature variation of the charge pump current can influence the damping factor, loop gain and phase margin, also the impact of temperature variation is getting worse with technology scaling. For the PLL design, the loop performances, such as the locking time and phase noise, will be changed with temperature variations significantly. So, in this paper, the zero coefficient of temperature current is designed to the current of the charge pump. As shown in Fig. 5, the start and current reference generator circuit provide the functions of start and the zero coefficient of temperature current. When $V_{\rm EN}$ is high, this block is enabled by the transistors M50, M14, M20 and the resistor R_4. Then the positive coefficient of temperature current is generated by the circuit composed of M16–M19, Q1–Q2 and R_5. Through R_6, R_7 and Q3, the zero coefficient of temperature voltage V_1 and negative coefficient of temperature voltage V_2 are obtained. We assume the proportion of M16 and M21 is k_1, as shown in Fig. 5. Then

$$\frac{\Delta V_{\rm be1-2}}{R_5}k_1(R_6+R_7)+V_{\rm be3}=V_1, \tag{12}$$

$$\frac{\Delta V_{\rm be1-2}}{R_5}k_1R_7+V_{\rm be3}=V_2. \tag{13}$$

Depending on the cancellation of the temperature coefficient of V_2 and R_9, the voltage following by the OP2 and M27, the current I_2 can be adjusted to a zero coefficient of temperature. At the same time, the current I_2 can be adjusted to a positive coefficient of temperature by the OP1, M23 and R_8. So, the zero coefficient of temperature current I_2 will lead to a fixed effect on the loop parameters. The power consumption of the start and reference block is only 10 μA, which does not affect the whole chip efficiency severely. Although the current I_1 is the positive coefficient of temperature, the slope current can be adjusted to a zero coefficient of temperature, which is deduced in the block of the slope current control:

$$\left(\frac{\Delta V_{\rm be1-2}}{R_5}k_1R_7+V_{\rm be3}\right)\Big/R_9=I_2, \tag{14}$$

$$\left(\frac{\Delta V_{\rm be1-2}}{R_5}k_1\left(R_6+R_7\right)+V_{\rm be3}\right)\Big/R_8=I_1. \tag{15}$$

In order to reduce the phase noise spurs, the minimum pulse indictor is designed to realize the minimum pulse indicator, which cuts off the slope current when the width of the charge pulse is less than the minimum pulse. Through the capacitor C_5, we can adjust the minimum pulse. The delay of the series inverter can also be used in most of the applications to obtain a short delay.

The slope current control block is designed to generate the slope charge pump current dependent on the output of the PFD. As shown in Fig. 5, firstly, once the slope current following the minimum pulse is enabled, the transistor M3 stops discharging, and the transistor M24 begins to charge the capacitor C_4. At the same time, a followed buffer makes the voltage across the resistor R_2 equal the voltage across the capacitor C_4. Then the current through the resistor R_2 can be controlled by the capacitor C_4 and the constant charging current. It can be expressed by Eqs. (16)–(19):

$$V_{\rm A}=\frac{I_3\Delta t}{C_4}, \tag{16}$$

$$V_{\rm A}=V_{\rm B}, \tag{17}$$

$$I_{\rm slope}=\frac{V_{\rm B}}{R_2}, \tag{18}$$

$$I_{\rm charge}=I_{\rm slope}+I_{\rm b}, \tag{19}$$

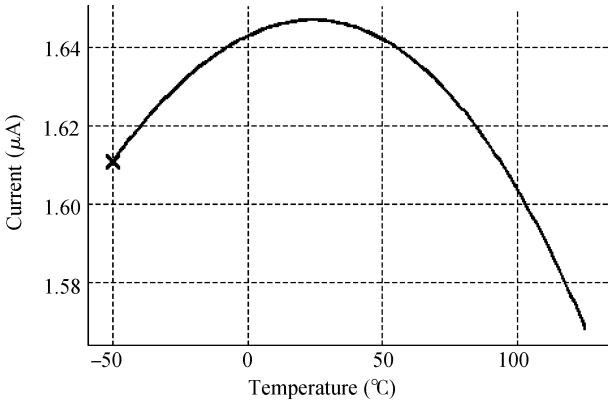


Fig. 6. Waveform of the zero coefficient of temperature current.

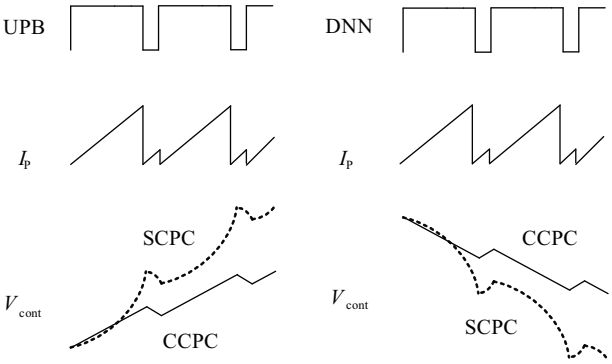


Fig. 7. Response comparison of SCPC and CCPC.

where V_A is the voltage across the capacitor C_4, I_3 is the charging current to the capacitor C_4, Δt is the time of the charging pulse width or the pulse width of UPB, V_B is the voltage across the resistor R_2, I_b is the basic charging current, and I_{slope} is the current generated from the resistor R_2. With the linearly increased charge pump current, the CPPLL successfully operates at the optimum bandwidth and the minimum phase noise at the different frequency output. There is an important note that the bandwidth of the buffer must be higher than the reference frequency to ensure the slope current can follow the input of the buffer.

The charge pump block deals with the combination of the basic charge pump current and slope current by M28 and M29. Furthermore, the charge and discharge structure adopts the cascade current mirror, improving the accuracy and the swing, which can provide a matched terminal to the charge pump current. In order to prevent the spark voltage on the V_{cont}, the transistor switches M44 and M49 are placed at the source of the current transistor. Finally, Figure 6 shows the simulation results of the zero coefficient of temperature current, which show that the current is nearly constant in the temperature range of –55 to 125 ℃, and the charge current is equal to the discharge current with high accuracy. Figure 7 shows a comparison of the traditional constant charge pump current (CCPC) and the proposed slope charge pump current (SCPC). It can be seen that the voltage V_{cont} has the faster response in the proposed circuit, because the slope of the voltage V_{cont} increases with the pulse width of UPB and DNN, respectively.

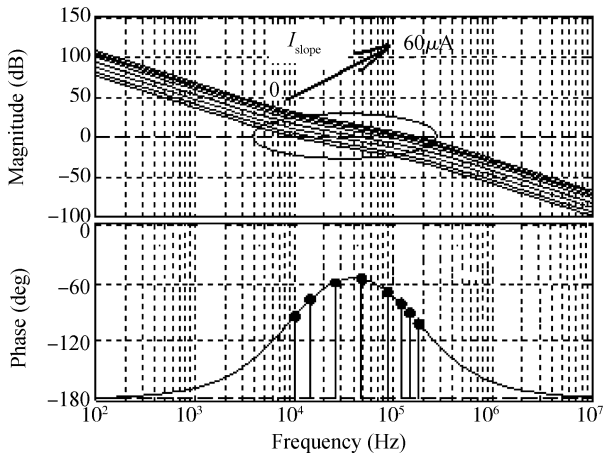


Fig. 8. Loop bandwidth and phase margin.

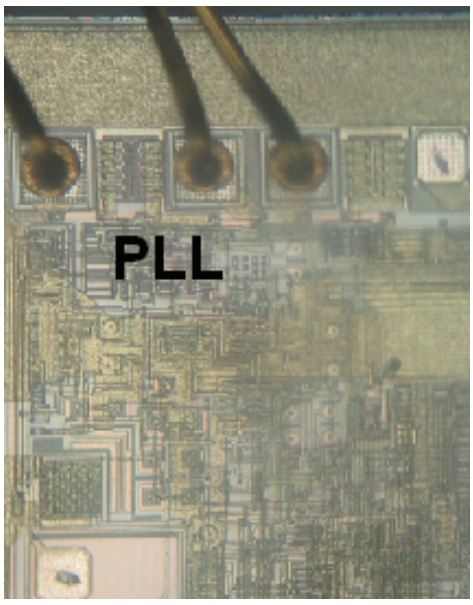


Fig. 9. Micrograph of the proposed PLL.

4. Experimental result analysis

Adopting the slope charge pump current technology, the behavior of the adaptive PLL is estimated and compared to the different charge pump currents. Figure 8 shows the loop stability under the slope charge pump current depending on the design of Eqs. (4)–(8). The design of the slope charge pump current part is from 0 to 60 μA. From Fig. 8 we can see that the loop bandwidth can be adjusted by the slope charge pump current with good stability. The phase margin is well controlled in the stable range (60°–120°) under the different output frequencies and slope charge pump current. Therefore, the locking time is optimized with the slope charge pump current. Finally, the proposed PLL has been fabricated in a kind of DSP chip based on a 0.35 μm CMOS process, as shown in Fig. 9. The proposed PLL part occupies a die size of approximately 500 $\times$ 400 μm^2. Comparing the area with the slope charge pump current and other dynamic loop bandwidth circuits reveals that the area overhead is much smaller.

The test diagram of the proposed PLL embedded in a DSP

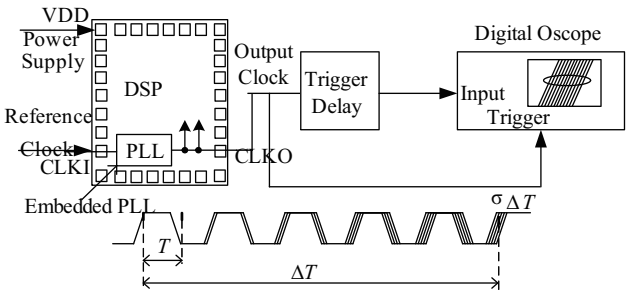
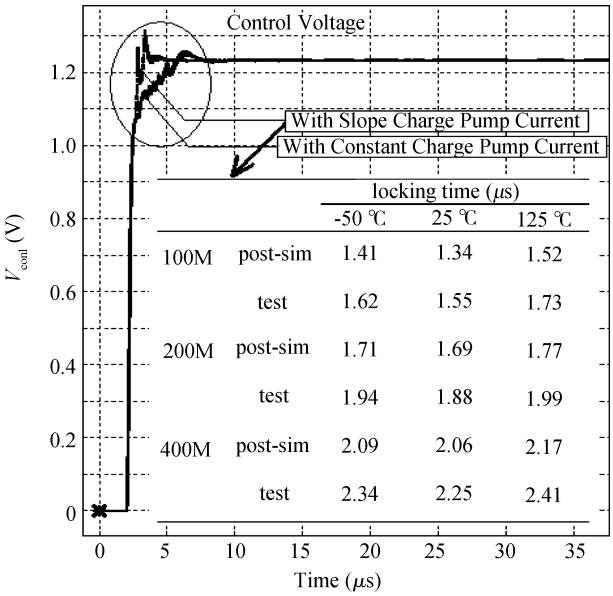


Fig. 10. Test diagram of the proposed PLL embedded in a DSP chip.



		locking time (μs)		
		-50 ℃	25 ℃	125 ℃
100M	post-sim	1.41	1.34	1.52
	test	1.62	1.55	1.73
200M	post-sim	1.71	1.69	1.77
	test	1.94	1.88	1.99
400M	post-sim	2.09	2.06	2.17
	test	2.34	2.25	2.41

Fig. 11. Comparison of the locking time between the post-simulation and test.

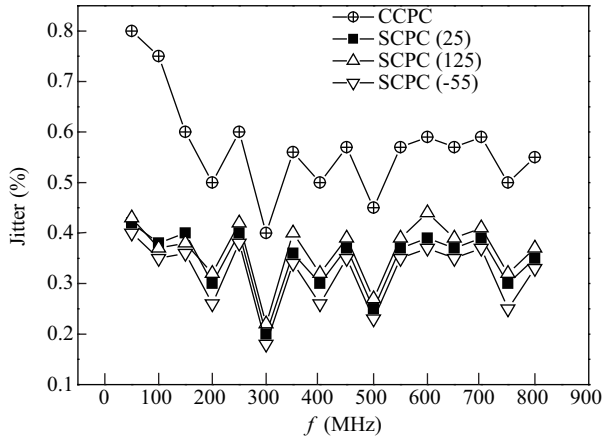


Fig. 12. Measured frequency peak-to-peak jitter versus output frequency.

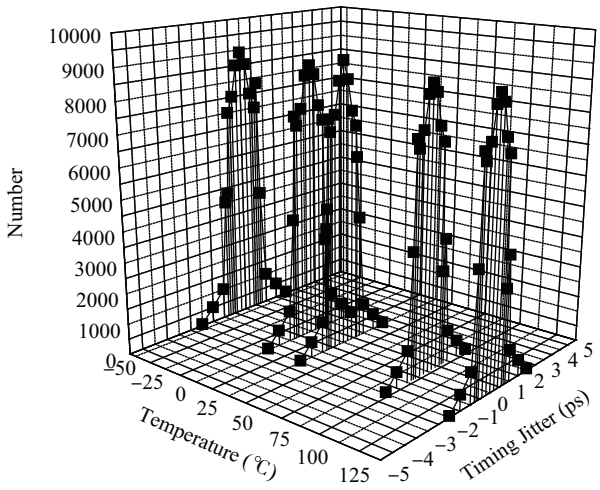


Fig. 13. Measured cycle−cycle clock jitter.

chip using the pin multi-using technology is shown in Fig. 10. The CLKI and CLKO pins are used to test the input and output of the proposed PLL, respectively. The reference clock is the crystal oscillator connected to the CLKI pin. The delay connected to the CLKO pin, as the output of the proposed PLL in the test mode, plays an important role to compensate for the trigger delay of the oscilloscope. The locking time and peak-to-peak jitter measurement results of the proposed PLL are shown in Figs. 11 and 12. In this verification, a large deviation in the frequency is detected. Then the charge pump current becomes very large to achieve fast locking. The loop gain follows the same tendency as the deviation. Smaller deviations bring back the loop gain value to the weak gain to complete the fine tuning adjustments. In Fig. 11, the fast one is the PLL which adopts the slope current control and the fast start-up circuit. Both circuits include identical building blocks, but a fast start-up and slope current control is added to the first PLL. The classical PLL locks after 8 μs while the variable controlled slope charge pump current PLL locks after less than 2 μs under the same conditions. Also, Figure 11 gives the locking time table between the post-simulation and the test results, which shows that the experimental results compare favourably with the post-simulation. Also, Figure 12 gives a comparison of the peak-to-peak jitter of the PLL, with the slope charge pump current (SCPC) and the constant charge pump current (CCPC) versus the output frequency. Jitter is the percentage of the absolute jitter/output clock period, which shows that the jitter of SCPC structure, is obviously lower than that of the CCPC structure[10]. The frequency in common use in the DSP is 100 MHz, shown in Fig. 10. So, a large number of cycles are measured to verify the accuracy of the output frequency in the practical application, as shown in Fig. 13. At the temperatures –55/0/25/85/125 ℃, the majority of the cycles converge at the certain point 0 ps. All of these measurements give the conclusion that the presented structure produces a unique combination of fast convergence, high accuracy, stability and circuit robustness. Finally, the performances are summarized and compared to other relative references in Table 1.

5. Conclusions

The PLL structure investigated in this paper achieves a short locking time and low jitter with the adaptive bandwidth control, which resolve the problem of the tradeoff between the locking time and the phase noise or reference spurs that exist in the traditional structure. With the simple and feasible circuit, without adopting the extra digital port, the charge pump

Table 1. Performance summary and comparison.

Parameter	Ref. [3]	Ref. [7]	Ref. [9]	This work
Fast settling method	Dynamic loop bandwidth	Wide-bandwidth fractional-*N*	Frequency presetting with calibration	Novel, simple and every cycle adaptive loop bandwidth control
Process	0.6 μm CMOS	0.18 μm CMOS	0.18 μm CMOS	0.35 μm CMOS
Supply voltage (V)	3	1.8	3.3/1.8	1.8–3.3
Frequency range (GHz)	0.08–0.25	2.4–2.5	0.99–1.45	0.001–0.8
Loop bandwidth (kHz)	—	> 730	< 100	Dynamic (10–200) with zero-temp coefficient
Lock-in time (μs)	30 cycles (dependent on frequency step)	35 (dependent on frequency step)	3 (dependent on frequency step)	Less than 2 (dependent on frequency phase detector)
Phase noise (ps)	2.544 (RMS)	—	—	2.005 (RMS)

current can be increased linearly depending on the PFD. At the same time, with the help of the fast start-up control, an adaptive optimization of bandwidth is obtained to increase the locking speed and reduce the jitter. Meanwhile, by temperature compensation, the improved characteristics can be kept in a wide operating temperature. The proposed PLL has been fabricated in a kind of DSP chip based on a 0.35 μm CMOS process. Comparing the characteristics with the classical PLL and the proposed PLL shows that the latter has a short locking time and low jitter. This technology can be used both in clock recovery and in clock synthesis, which require a short locking time and low jitter characteristics.

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