Design of an analog front-end for ambulatory biopotential measurement systems*

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Abstract: A continuously tunable gain and bandwidth analog front-end for ambulatory biopotential measurement systems is presented. The front-end circuit is capable of amplifying and conditioning different biosignals. To optimize the power consumption and simplify the system architecture, the front-end only adopts two-stage amplifiers. In addition, careful design eliminates the need for chopping circuits. The input-referred noise of the system is only 1.19 μVrms (0.48–2000 Hz). The chip is fabricated via a SMIC 0.18 μm CMOS process. Although the power consumption is only 32.1 μW under a 3 V voltage supply, test results show that the chip can successfully extract biopotential signals.

Key words: analog front-end; biopotential measurement system; low-power; low-noise
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1. Introduction

According to Refs. [1, 2], the cost of healthcare delivery is on a sharp upward trend. In the US alone, for example, the total national healthcare spend in 2009 increased by 6.9%. It is anticipated that the total expense will double in dollars by the end of 2019, consuming around 21% of the national GDP. A typical instance can be the diagnosis of heart disease. The patient is required to stay in bed for continuous monitoring by electrocardiogram (ECG), thus removing the patient from his routine work. Meanwhile, monitoring should always take place under the supervision of medical personnel, which is also an expensive endeavor.

With the development of microelectronics technology, a possible solution to this problem may be the ambulatory biopotential measurement system[2]. This kind of system not only frees the patient but also requires less human input in the whole process of measuring. Therefore, the potential medical cost is reduced.

However, the realization of such a system puts a lot of challenges on the system design, especially for the analog front-end circuits. To successfully extract the biopotential signals, the circuit has to cope with various demands which are closely related to the characteristics of these biosignals[3]. (1) For low frequency (lower than 1 Hz) and μV-amplitude signals, the flicker and thermal noise play an important role in the frequency of interest. Noise optimization should be taken into consideration. (2) The 50 Hz coupling from the mains appears as a common-mode signal in the input of the front-end circuits, which requires a high CMRR (greater than 90 dB). (3) The mismatch of electrodes generates a DC offset voltage. The system must be able to can implement the high-pass function to eliminate this DC electrode offset. (4) The front-end circuits should be low power to meet the requirements of ambulatory applications and have variable bandwidth and gain to be compliable with different biopotential signals, such as ECGs, electroencephalograms (EEGs) and electrooculograms (EOGs).

In recent years, a few attempts have been made to tackle these challenges. Reference [4] reports a biopotential signal readout front-end under a 90 nm CMOS process, and Reference [5] implements an 8-channel EEG front-end ASIC. Both designs require a chopping technique, but the introduction of a chopping technique makes the systems suffer from the spikes that are generated from the switches of the chopper. Reference [6] describes a current-balancing amplifier with switched-capacitor filters to condition the biosignals. However, the use of a switched capacitor not only consumes excessive power but also complicates the circuit topology. In Ref. [7], a low-noise neuropotential amplifier with an ADC embedded is presented, but the CMRR of the system is only 76 dB, which makes it sensitive to mains interference.

This paper proposes a single 3 V voltage supply analog front-end. The front-end is pure analog without interference from digital parts, like chopping and switch capacitor circuits. The noise performance is maintained by careful design of critical transistors. The system adopts only two stage amplifier architecture. The continuous gain and bandwidth achieved make the system more compatible with a variety of biopotential signals.

2. System architecture

A typical analog front-end for a biopotential measurement system always implements two main functions: amplifying and conditioning. It is common practice to embed the band-pass filter within such a low noise and low power amplifier.

Figure 1 shows the proposed system architecture of the analog front-end circuits. The front-end mainly consists of two stages. The first stage is a high-pass current feedback amplifier (HPCFA). The weak biosignals fed into the system are amplified and AC-coupled in this stage. So the DC offset voltage can effectively be eliminated. The second stage is a variable bandwidth and gain amplifier (VBGA), which offers enough gain and conditions the signal with low-pass filtering. Variable gain and bandwidth make the system suitable for different biopo-

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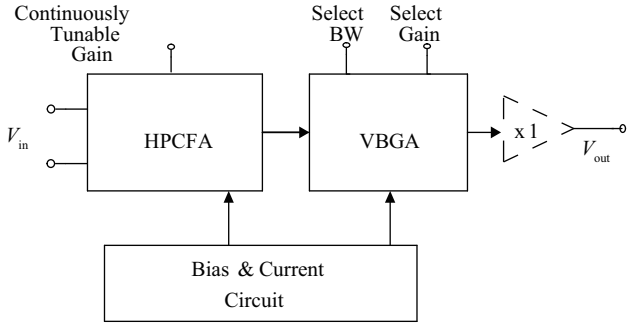

Fig. 1. System architecture of analog front-end.

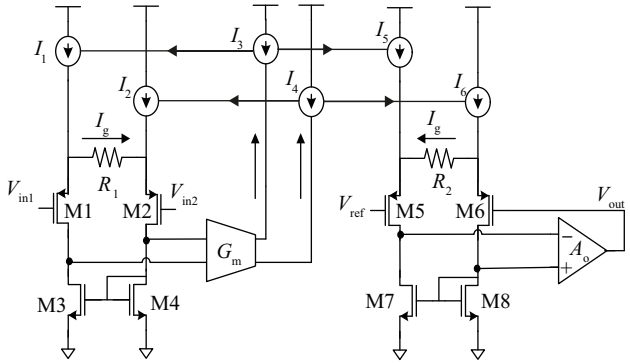

Fig. 2. Concept of current feedback amplifier.

tential signals. If necessary, a buffer can be inserted to drive the sampling capacitors of the following ADC for further digital processing. Bias and current circuits are also included in the system to offer all the DC operating points and current sources needed.

3. Circuit implementation

3.1. High-pass current feedback amplifier (HPCFA)

The basic concept of a current feedback amplifier[8] is shown in Fig. 2. With no signal applied, the circuit is balanced and all currents are equal, $V_{out} = V_{ref}$. When a differential signal is applied, the output current of the transconductance stage G_m becomes unbalanced in order to keep the currents of M1 and M2 equal. In this situation, the V_{gs} of M1 and M2 are also approximately equal and

$$I_g = (V_{in2} - V_{in1})/R_1. \tag{1}$$

This current difference is mirrored to current source I_5 and I_6. The output stage (M5–M8) serves as a transresistance stage and creates the output voltage according to

$$I_g = (V_{out} - V_{ref})/R_2. \tag{2}$$

Combining Eqs. (1) and (2), Equation (3) can be easily derived:

$$V_{out} = V_{ref} + (V_{in2} - V_{in1})R_2/R_1. \tag{3}$$

The voltage gain is decided by the ratio of the two resistors. The resistors no longer need laser trimming as those in three-opamp architecture[9]. In fact, the current feedback topology is a very good choice for the implementation of analog front-end circuits.

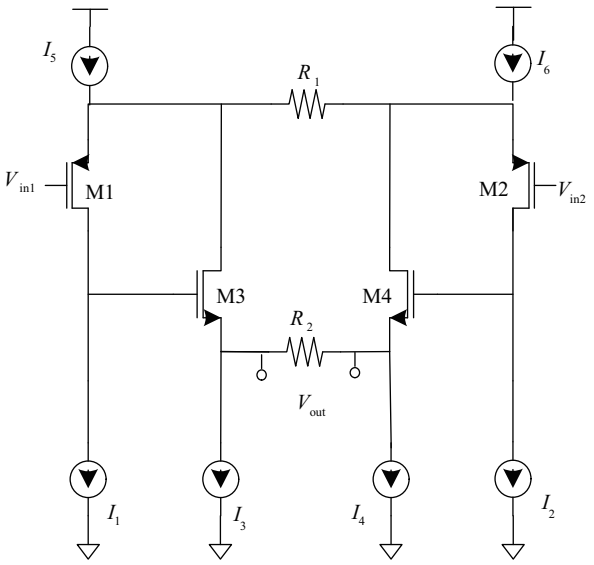

Fig. 3. Architecture of differential current feedback amplifier.

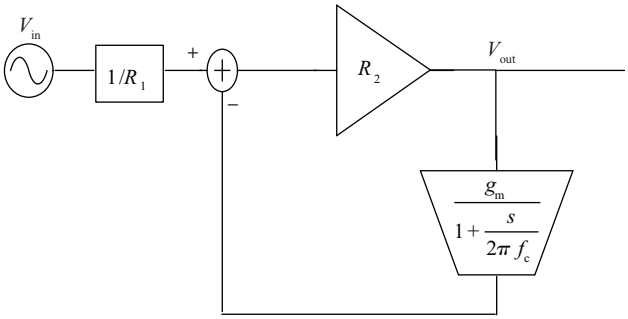

Fig. 4. Equivalent diagram of the HPCFA.

We implement a fully differential current feedback amplifier (CFA) based on the concepts of current feedback, as shown in Fig. 3. The theory behind the circuits can be understood in an intuitive way. When differential signals are applied, small current signals can only pass through resistor R_1 for the existence of current source I_1 and I_2. For the same reason, current sources I_3 and I_4 lead the small current flowing through R_2. The small signal current circling between R_1 and R_2 make the gain of the circuits still defined by the ratio of R_1 and R_2. Transistors M3 and M4 serve not only as a G_m stage, but also as the current mirrors and transresistance stage to recreate the output voltage. Totally differential architecture not only improves the CMRR of the system but also simplifies the circuits by reducing the parallel current pairs.

Considering the high-pass characteristic of the system, we do not design additional high-pass filters. Instead, G_m–C filter is introduced to the feedback circuits. Figure 4 shows the equivalent diagram of the HPCFA. The transfer function of Fig. 4 can be calculated as

$$\frac{V_{out}}{V_{in}} = \frac{s + 2\pi f_c}{s + 2\pi f_c(1 + g_m R_2)} \frac{R_2}{R_1}, \tag{4}$$

where f_c is the low pass cut-off frequency of the G_m–C filter.

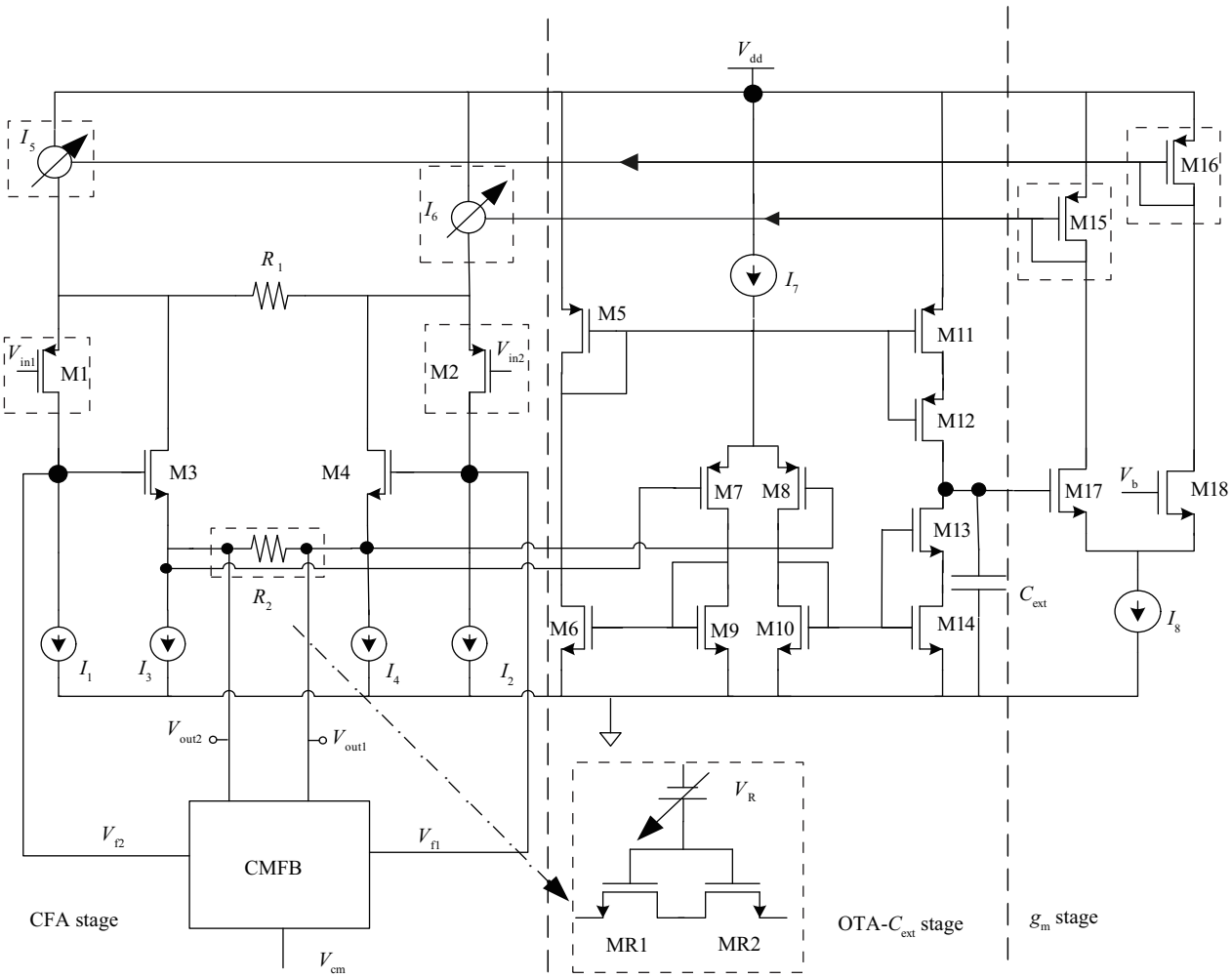

Fig. 5. Circuit implementation of HPCFA.

If $g_m R_2$ is much greater than 1, Equation (4) is a typical high-pass-filter function with a cut-off frequency of $g_m R_2 f_c$.

Figure 5 gives the circuit implementation of the HPCFA. The G_m–C filter actually consists of an OTA-C_{ext} stage (M5–M11) and a g_m stage (M15–M18). The combination of these two stages ensures that $g_m R_2$ in Eq. (4) is much greater than 1. Therefore, the cut-off frequency of the first stage can be rewritten as:

$$f_h = \frac{g_{M17} R_2 g_{m,OTA}}{2\pi C_{ext}}, \tag{5}$$

where g_{M17} and $g_{m,OTA}$ are the transconductance of transistor M17 and OTA separately. Transistor pairs M11, M12 and M13, M14 are connected in series. Since $g_m \propto L^{-1/2}$, an increase in equivalent L will minimize $g_{m,OTA}$. As for C_{ext}, it is defined around 1 μF. This capacitor consumes too much room in the chip, so it is implemented externally.

To save space, R_2 is implemented by two NMOS transistors (MR1 and MR2, shown in Fig. 5) work in linear region. Altering the V_R can vary the equivalent resistance, thus a continuously tunable gain is achieved.

The HPCFA has a fully differential architecture, so a common mode feedback (CMFB) circuit is needed, as shown in Fig. 6.

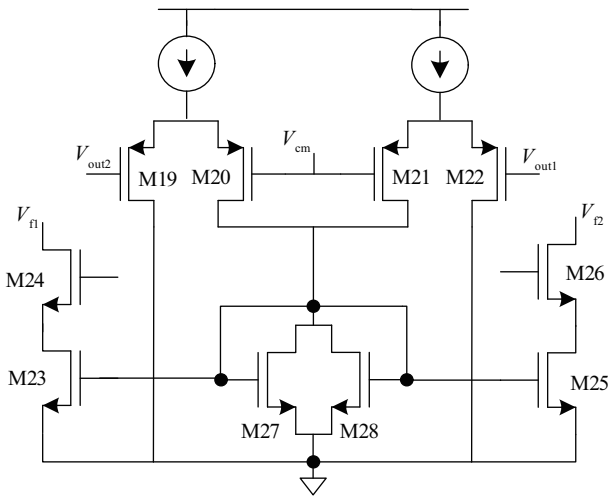

Fig. 6. CMFB circuits for HPCFA.

3.2. Discussion of CMRR and noise of HPCFA

The CMRR of the whole analog front-end circuits is mainly defined by the first stage, i.e. the HPCFA stage. For current feedback topology, factors that affect the CMRR performance can be written as[10]

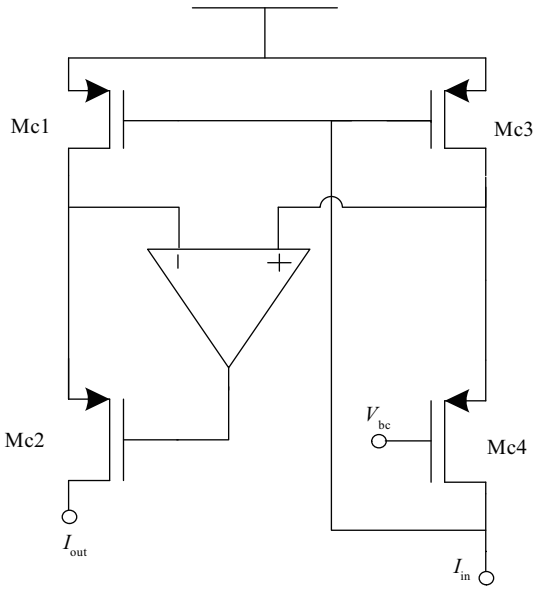

Fig. 7. Active current source.

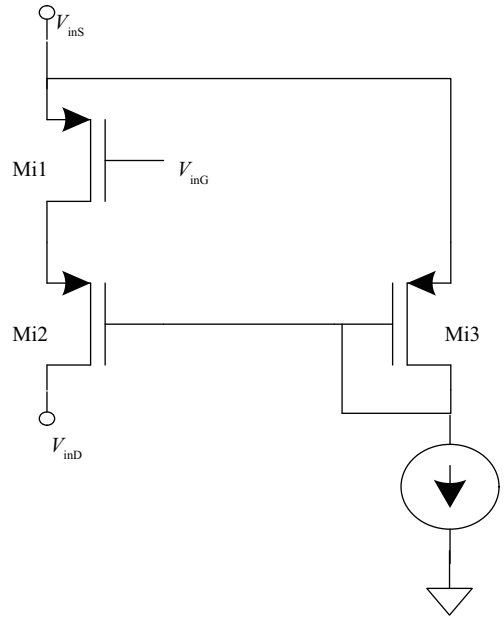

Fig. 8. Dedicated input stage.

$$\frac{1}{\mathrm{CMRR_{all}}} = \frac{1}{\mathrm{CMRR_{struct}}} + \frac{1}{\mathrm{CMRR_{iout}}} + \frac{1}{\mathrm{CMRR_{in}}}, \quad (6)$$

where $\mathrm{CMRR_{all}}$ is the total equivalent CMRR, $\mathrm{CMRR_{struct}}$ is the CMRR defined by the system topology, $\mathrm{CMRR_{iout}}$ is the CMRR restricted by the limited output resistance of current sources I_5 (or I_6) and $\mathrm{CMRR_{in}}$ is the CMRR with the V_{ds} mismatch of input transistors (M1 and M2).

The topology in Fig. 5 is fully differential, so $\mathrm{CMRR_{struct}}$ is infinity in theory and the first item in Eq. (6) can be ignored. For the second item, we increase the output resistance of the current source to optimize $\mathrm{CMRR_{iout}}$. An active current source is adopted to achieve even greater output resistance than the cascade current source. Replacing M15, M16 and current sources I_5, I_6 with the active current source (shown in Fig. 7) gives an output resistance:

$$R_{\mathrm{out}} = (r_{\mathrm{o,Mc1}} g_{\mathrm{Mc2}} r_{\mathrm{o,Mc2}}) A, \quad (7)$$

which is A times greater than that of the cascade current source (A is the gain of the amplifier). Greater output resistance means greater $\mathrm{CMRR_{iout}}$.

For the third item in Eq. (6), a dedicated input stage[11] is introduced to overcome the V_{ds} difference between M1 and M2, shown in Fig. 8. Assuming Mi1, Mi2 and Mi3 all work in the saturation region with fixed current, the V_{gs} of these three transistors are constant. Obviously, V_{ds} of Mi1 is the V_{gs} difference between the other two transistors, i.e. $V_{gs,\mathrm{Mi2}} - V_{gs,\mathrm{Mi3}}$. V_{ds} of Mi1 does not vary with input voltage at the gate of Mi1. Therefore, the introduction of input stages ensures that V_{ds} of input transistors is no longer affected by the DC offset, which dramatically increases $\mathrm{CMRR_{in}}$.

Figure 9 shows the simulated CMRR of the HPCFA stage. The CMRR is as high as 137 dB, which is much greater than the 90 dB demanded by clinical use[3].

The input-referred noise of the system is another important issue. The same as CMRR, the noise performance of the front-end is dominated by the HPCFA stage. The HPCFA stage can

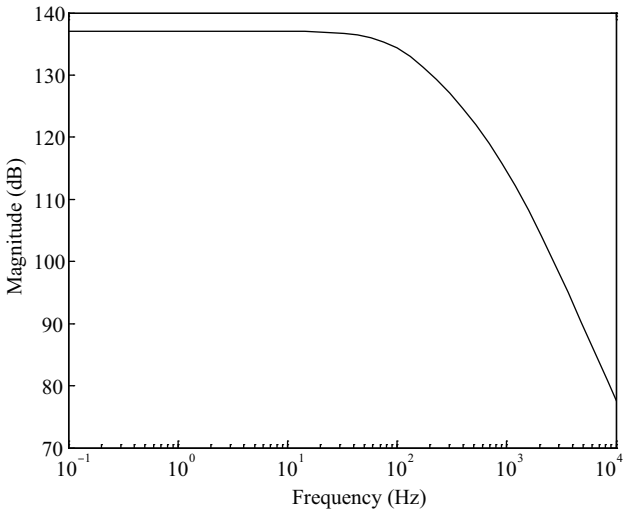

Fig. 9. Simulated CMRR of HPCFA.

be divided into two parts: the CFA stage and the G_m–C filter stage consisting of the OTA-C_{ext} stage and g_m stage. According to Eq. (4), the G_m–C filter offers a low-pass cut-off frequency f_c, which is much lower than the high-pass cut-off frequency $g_m R_2 f_c$. Therefore, the G_m–C stage filters its own input-referred noise. The systematic noise is directly decided by the CFA stage (shown in Fig. 3). Analysis of the small signal half-circuit noise model (shown in Fig. 10) reveals that the input referred noise of the CBA can be expressed as

$$\begin{aligned}\overline{V_{\mathrm{CFA}}^2} = {} & \overline{V_{\mathrm{M1}}^2} + \frac{1}{2}\overline{V_{R_1}^2} + \frac{R_1^2}{R_2^2}\left(\overline{V_{\mathrm{M3}}^2} + \frac{1}{2}\overline{V_{R_2}^2}\right) \\ & + g_{\mathrm{m}I_5}^2 R_1^2 \overline{V_{I_5}^2} + g_{\mathrm{m}I_3}^2 R_1^2 \overline{V_{I_3}^2} \\ & + g_{\mathrm{m}I_1}^2 \left(R_1 + \frac{1}{g_{\mathrm{mM1}}}\right)^2 \overline{V_{I_1}^2}, \end{aligned} \quad (8)$$

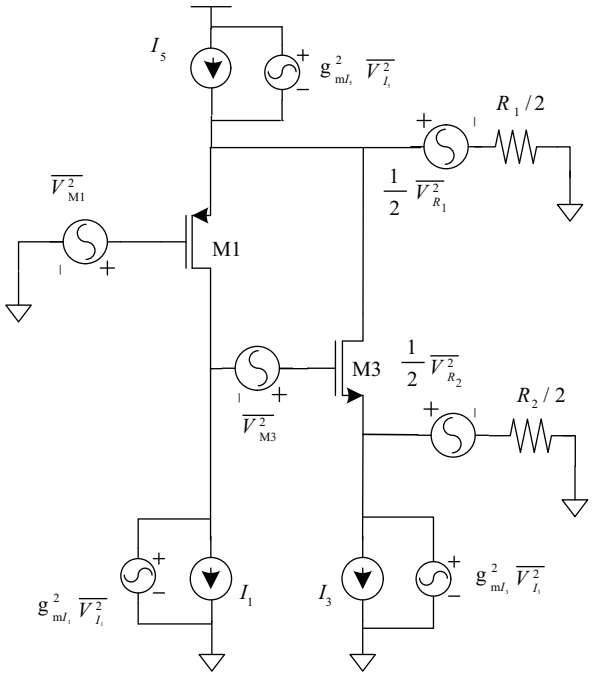

Fig. 10. Small signal half-circuit noise model.

where $g_{mI_1}, g_{mI_3}, g_{mI_5}$ are the transconductance of current sources I_1, I_3 and I_5.

Considering thermal noise can be expressed as $8kT/3g_m$ and $R_1/R_2 \ll 1$, Equation (8) can be rewritten as

$$\overline{V_{CFA}^2} = \frac{8KT}{3}\left[\frac{1}{g_{mM1}} + \frac{3}{4}R_1 + R_1^2 g_{mI_5} + R_1^2 g_{mI_3} + g_{mI_1}\left(R_1 + \frac{1}{g_{mM1}}\right)^2\right]. \quad (9)$$

The current sources I_1, I_3 and I_5 work in the saturation region and can ensure transconductance g_{mI_1}, g_{mI_3} and g_{mI_5} a relatively low value. Additional means to optimize the noise can be an increase in g_{mM1} or a decrease in R_1. Transconductance g_{mM1} can be maximized when transistor M1 works in the sub-threshold region. However, the resistor R_1 cannot be reduced arbitrarily. Decreasing R_1 will lead current caused by an input DC offset to increase. If current in the G_m stage does not increase proportionally, the DC offset the system can overcome is reduced. Raising the current can overcome this problem but sacrifice the consumption. So a trade-off between DC offset and consumption should be taken into during the design.

As for the flicker noise, we do not use chopping circuits and digital clocks to process this noise as is normal. Instead, careful design is used to optimize the dimensions of the transistors. Since the $1/f$ noise is in inverse proportion to the gate area, large dimension transistors are adopted, especially for the input. Large W/L ratio input PMOS transistors not only guarantee a big gate area but also greater g_{mM1}, since the input transistors work in the sub-threshold region. In some ways, the methods to optimize the thermal noise and flicker noise are the same.

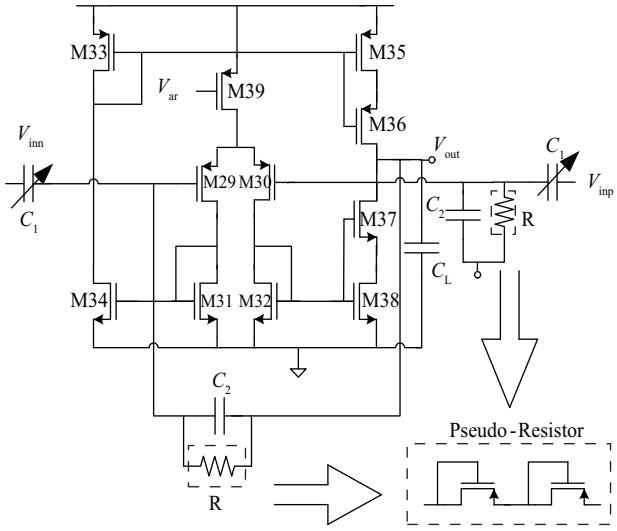

Fig. 11. Circuit implementation of the VBGA stage.

3.3. Variable bandwidth and gain amplifier (VBGA)

The voltage gain of the first stage is not big enough for a weak biopotential signal. A second stage amplifier circuit is introduced. The amplifier is implemented as a variable gain and bandwidth amplifier, which is suitable for different amplitude and frequency biosignals, like ECG, EMG, EEG and EOG signals. The VBGA composed of transistor M29–M39 is shown in Fig. 11.

Capacitors C_1 and C_2 form negative feedback circuits and resistor R sets the DC operating point. When $C_1, C_L \gg C_2$, the gain of the circuit is decided by the ratio of C_1 to C_2. The high and low cut-off frequencies are

$$f_h = 1/2\pi C_2 R, \quad (10)$$

$$f_l = g_m C_2/2\pi C_1 C_L, \quad (11)$$

where g_m is the transconductance of the amplifier. For ECG signals, the high cut-off frequency is as low as 0.5 Hz. If C_2 is set as 1 pF, the resistor R should be higher than 10^{11} Ω. It is almost impossible to implement this resistor in the chip. A pseudo-resistor made from two MOS-bipolar[12] devices can be a substitution for this kind of resistor. With negative V_{gs}, each device functions as a diode-connected pMOS transistor. With positive V_{gs}, the parasitic source–well–drain p–n–p bipolar junction transistor (BJT) is activated and the device acts as a diode-connected BJT. So whenever V_{gs} is positive or negative, for a small voltage across the pseudo-resistor, the current passing this device is ultra-low and its equivalent resistance is always higher than 10^{12} Ω.

C_1 is designed as the combination of capacitors internally and externally. To save space, we implement this capacitor with 10 pF in the chip and 10 to 80 pF off-the-chip. An external capacitor is connected in parallel with the internal capacitor and can be adjusted by switches. Thus, variable gain is achieved.

A high cut-off frequency relies on the C_L and transconductance of the OTA. A biopotential signal extracted from the human body is always in the magnitude of several hundred

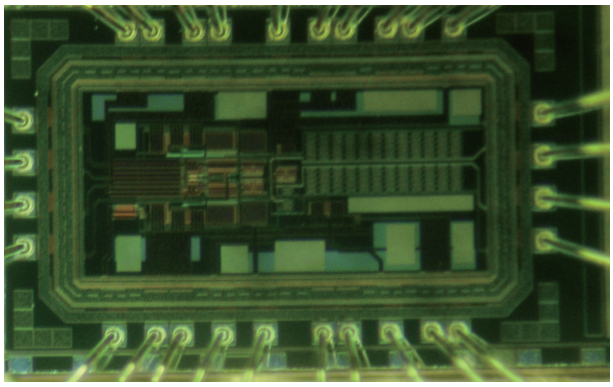

Fig. 12. Die micrograph of the chip.

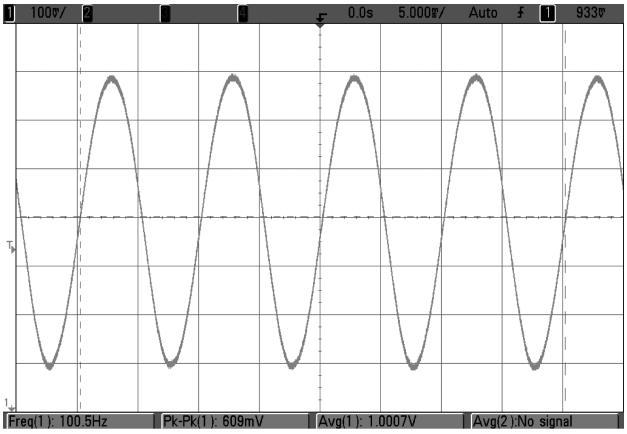

Fig. 13. Transient response of a sinusoidal signal.

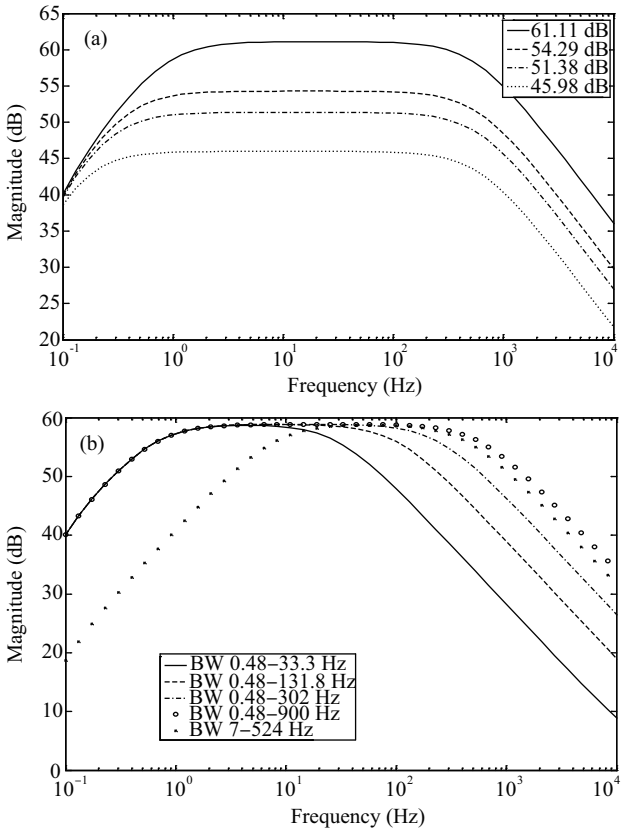

Fig. 14. (a) Measured variable gain of the front-end. (b) Measured variable bandwidth of the front-end.

Hz; increasing C_L alone to lower the frequency is not a cost-effective choice. Instead, varying the gate voltage of transistor M39 leads to the alternation of the OTA bias current, thus affecting transconductance g_m. Since gm is in direct proportion to the current in transistor M39, reducing g_m makes the transconductance qualified for the amplifier bandwidth. In addition, the power dissipation is saved.

4. Experimental results

The analog front-end has been realized in a SMIC 0.18 μm process. The die micrograph of the chip takes up an area of 1630×974 μm^2, as shown in Fig. 12.

Figure 13 shows the transient response of the front-end with the gain set to 300 (49.5 dB). A 100 Hz 2 mV Vpp input signal is generated by AP2700.

Figure 14(a) shows four different gains, 45.55 dB, 51.38 dB, 54.29 dB and 61.11 dB that are measured. Additional gain could be achieved by continuously changing the V_R of the HPCFA stage and external capacitor of the VBGA stage. Figure 14(b) shows the AC response of the front-end. Four different bandwidths are measured. The measured results clearly show that the bandwidth of the front-end includes the spectra of ECG, EEG, EMG and EOG signals.

Figure 15 shows the amplification of an ECG signal generated by an ECG stimulator. The stimulator creates a 1 mV Vpp ECG signal with artificial interference. When the gain is set to 52.6 dB, the measured result shows that the ECG signal

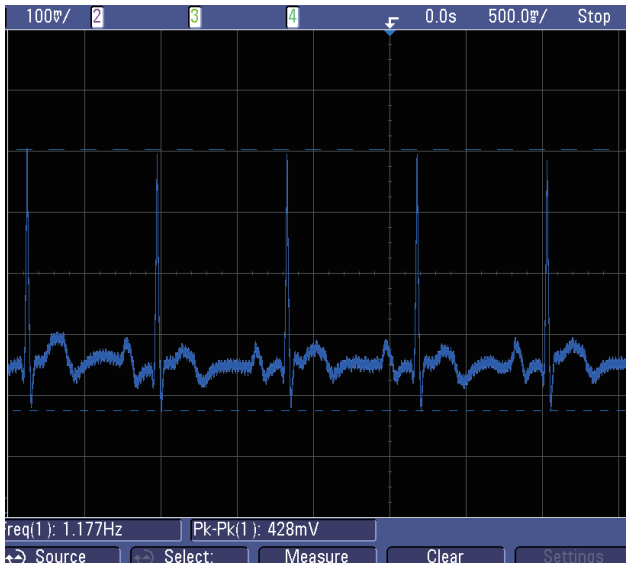

Fig. 15. Measured ECG signals from the analog front-end.

can be clearly extracted. The 50 Hz interference is effectively reduced. All the P, Q, R, S and T complexes are evident on the waveform.

The NEF (noise efficiency factor)[12] is always introduced to evaluate a different low-noise low-power amplifier.

Table 1. Performance summary of this work.

Parameter	Value	Parameter	Value
Process	SMIC 0.18 μm	High cut-off frequency (changed by C_{ext})	> 0.48 Hz
Supply voltage	3 V	Low cut-off frequency (continuously tunable)	< 2000 Hz
Power consumption	32.1 μW	Gain (continuously tunable)	40–63 dB
Input referred noise	1.19 μV_{rms} (0.48–2000 Hz)	NEF	2.97
CMRR	137 dB		

Table 2. Performance comparison with recently published papers.

Reference, Year	Ref. [13], 2007	Ref. [6], 2008	Ref. [7], 2009	This work
Voltage supply (V)	$\pm$1.7	$\pm$1.5	+3.3	+3
Power (μW)	27.2	142.8	40.26	32.1
Input referred noise (μVrms)	3.6 (20– 10000 Hz)	2.417 (0.3– 150 Hz)	1.65 (0.5– 5000 Hz)	1.19 (0.48– 2000 Hz)
NEF	4.9	N/A	3.2	2.97
CMRR (dB)	N/A	155	> 76	137
Application area	ECG/ENAP	ECG/ECG/EMG	EEG/EcoG	ECG/EEG/EMG

$$\text{NEF} = V_{\text{in, rms}} \sqrt{\frac{2I_{\text{tot}}}{\pi V_{\text{t}} 4kTB_{\text{w}}}}, \tag{12}$$

where $V_{\text{in, rms}}$ is the input referred noise, I_{tot} is the total current consumption and B_{w} is the amplifier bandwidth. After calculating, the NEF of this work is 2.97.

Table 1 shows the performance summary of the whole analog front-end. For the constraints of testing equipment, the input referred noise and CMRR are just simulated here.

Table 2 compares this work with other recently published works. It can be seen that our work achieves the lowest NEF among the biopotential acquisition chips, which means better power and noise trade-off.

5. Conclusion

This paper presents an analog front-end for ambulatory biopotential measurement systems. The front-end achieves a continuous gain and bandwidth function with low-power and low-noise characteristics. The system has been successfully realized under a 0.18 μm CMOS process. The measurement results show that the system works well and can be used in different clinical practices.

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