# A low power dual-band multi-mode RF front-end for GNSS applications*

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**Abstract:** A CMOS dual-band multi-mode RF front-end for the global navigation satellite system receivers of all GPS, Bei-Dou, Galileo and Glonass systems is presented. It consists of a reconfigurable low noise amplifier (LNA), a broadband active balun, a high linearity mixer and a bandgap reference (BGR) circuit. The effect of the input parasitic capacitance on the input impedance of the inductively degenerated common source LNA is analyzed in detail. By using two different LC networks at the input port and the switched capacitor at the output port, the LNA can work at two different frequency bands (1.2 GHz and 1.5 GHz) under low power consumption. The active balun uses a hybrid-connection structure to achieve high bandwidth. The mixer uses the multiple gated transistors technique to acquire a high linearity under low power consumption but does not deteriorate other performances. The measurement results of the proposed front-end achieve a noise figure of 2.1/2.0 dB, a gain of 33.9/33.8 dB and an input 1-dB compression point of 0/1 dBm at 1227.6/1575.42 MHz. The power consumption is about 16 mW under a 1.8 V power supply.

**Key words:** dual-band; multi-mode; electrostatic discharge; low-noise amplifier; active balun; high linearity
**DOI:** 10.1088/1674-4926/31/11/115008 **EEACC:** 2570

## 1. Introduction

In recent years, GPS based applications for commercial use have grown dramatically. The manufacturers of cellular telephones, portable computers, vehicles and other mobile devices are looking for ways to embed GPS into their products. Although GPS is the only fully operational, available global navigation satellite system (GNSS), in the near future, GPS radios and the other three navigation systems, i.e. Bei-Dou, Galileo and Glonass, will be broadly utilized in cell phones, PDAs, cars and so on. The four navigation systems ranging signal broadcasting from the satellites mainly use two frequency bands: 1.2 GHz band and 1.5 GHz band. Most existing navigation receivers are one band one mode[1, 2], one band dual-mode[3] or dual-band one mode[4, 5]. Thus, there is strong motivation to provide highly integrated, low-cost, low-power, dual-band navigation receivers for the positioning services. This paper presents a dual-band multi-mode navigation receiver front-end targeted for low-cost, low power consumption and high linearity.

## 2. Receiver architecture and considerations

Usually, there are three typical architectures in the common wireless receiver design: super-heterodyne, low-IF and zero-IF. The super-heterodyne has been the most widely used architecture in the last few years, since it can provide high and stable performance. However, this architecture needs many more off-chip components, which thus increases the design complexity and the system cost. In addition, this architecture needs significant power to drive the off-chip surface acoustic wave (SAW) filters. Undoubtedly, this architecture is not suitable for low-power and low-cost applications. In contrast, zero-IF architecture is very low cost due to its very high integration. In this architecture, the image rejection is not very important at the RF front-end. However, it has some disadvantages, such as high flicker noise, DC-offset, LO leakage, even-order distortion and IQ mismatch. Furthermore, a significant amount of energy of the GPS signal is contained at the center frequency, so zero-IF implementation is unpractical.

In order to avoid the drawbacks of the two architectures described above, the navigation receiver described in this paper uses a low-IF architecture, as shown in Fig. 1. The low-IF receiver features a similar integratability as the zero-IF one. Compared with the zero-IF receiver, the low-IF receiver is less sensitive to $1/f$ noise and DC-offset at the expense of a higher image-rejection requirement. In this design, the RF SAW filter and the IF complex band pass filter (BPF) were used to improve the image rejection.

In Fig. 1, the RF signal is received by the antenna and is filtered with a RF SAW filter to remove the out-of-band signals, including the image signal. The dual-band low noise amplifier provides enough high gain (HG) to suppress the noise of the subsequent blocks. In order to connect the single-end LNA and the double balance mixer, the active balun was added be-

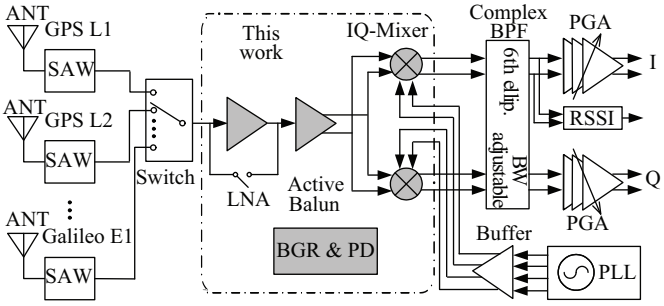


Fig. 1. Block diagram of the multi-mode selectable dual-band GPS receiver.

* Project supported by the National High Technology Research and Development Program of China (No. 2007AA01Z2A7).
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Received 15 April 2010, revised manuscript received 28 June 2010 

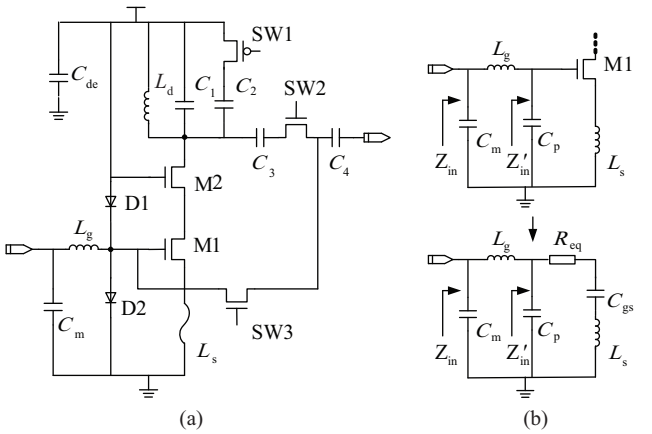


Fig. 2. Proposed dual-band LNA. (a) Schematic of the LNA. (b) Equivalent circuits of the input port.

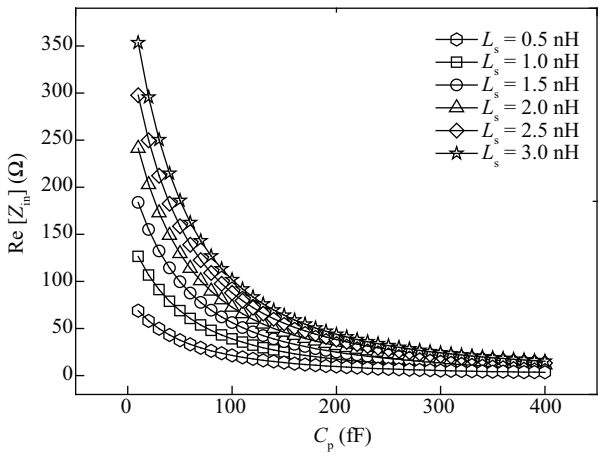


Fig. 3. Effect of $C_p$ on the real part of the input impedance ($W/L$ = 60/0.18, $V_{GS}$ = 0.65 V, $f$ = 1.5 GHz).

tween them. Then the broadband mixer converts the RF signal to an IF signal of 46 MHz. The active complex BPF acts as the channel selected filter and suppresses the image signal further. Last, the programmable gain amplifier (PGA) ensures that the receiver can satisfy the required dynamic range of the GPS receiver. In addition, in order to control the gain of the PGA, the received signal strength indicator (RSSI) circuit was added in front of the PGA.

This paper presents a dual-band RF front-end for multi-mode GNSS applications, including a dual-band single-end LNA, broadband active balun, high linear mixer and BGR. The BGR provides the precise bias voltage for the LNA, active balun and mixer. In addition, every block has the power down (PD) mode to save the product's power when the GNSS receiver does not need to work. The front-end topology shown in Fig. 1 was chosen based on the following reasons:

(1) Compared with the differential topology, a single-end LNA can save a lot of power consumption and chip area.

(2) The balun behind the LNA can achieve a lower noise figure than in front of the LNA, because an external balun will cause gain loss and therefore deteriorate the noise figure.

(3) The active balun can provide more positive voltage gain and save greater chip area than an on-chip passive balun.

(4) A 46-MHz IF can achieve very high image-rejection from the RF SAW filter.

## 3. Circuit design

### 3.1. Dual-band input impedance matching

The schematic of the proposed dual-band low-power LNA is shown in Fig. 2(a). The input ESD protection circuit comprises dual diodes D1 and D2. Figure 2(b) shows the equivalent circuits of the input port. $C_p$ is the parasitic capacitance of the input port, including the ESD protection circuit, bonding pad and SW3. Through a series of parallel-series and series-parallel conversions, the real part of $Z'_{in}$ can be expressed by

$$\mathrm{Re}\left(Z'_{in}\right) = R_{in} = \left(\frac{C_1}{C_1 + C_p}\right)^2 R_{eq}, \qquad (1)$$

where

$$\frac{1}{C_1} = \frac{1}{C_{gs}} - \omega^2 L_s, \quad R_{eq} = \omega_T L_s. \qquad (2)$$

From Eq. (1), it can be seen that the parallel parasitic capacitance $C_p$ transforms downwards the real part of the input impedance. Figure 3 shows the real part of the input impedance $Z_{in}$ versus the parasitic capacitance $C_p$ at different $L_s$ values. When $C_p$ increases, the real part of $Z_{in}$ decreased greatly. With $C_p$ > 200 fF (usually $C_p$ is greater than 200 fF[6]), the real part of $Z_{in}$ is below 30 Ω. From Eq. (1), it can be seen that larger $C_{gs}$, $L_s$ and $\omega_T$ can increase the Re[$Z'_{in}$], but a larger $L_s$ will reduce the gain and increase the noise figure. In addition, a larger $C_{gs}$ means a larger width, and a larger $\omega_T$ means a larger overdriving voltage, which increases the power consumption. That is to say, under the influence of the input parasitic capacitance, a single inductor $L_g$ cannot match the input impedance of the low-power LNA to 50 Ω. So, the external LC network ($L_g$, $C_m$) was used to match the input impedance, as shown in Fig. 2.

Figure 4 shows the dual-band input impedance matching using the different LC networks. From Fig. 4, it can be seen that the input impedance can be achieved to 50 Ω easily by using appropriate $C_m$ and $L_g$. By using two different LC networks, the input port of the LNA can be matched to 50 Ω easily.

### 3.2. LNA

The proposed dual-band LNA has two gain modes: HG mode and bypass mode. When the input power is small or using the passive antenna, SW2 is on, SW3 is off and the LNA works at the HG mode. Otherwise, when the input power is very large or using the active antenna, SW2 is off, SW3 is on and the LNA works at the bypass mode to avoid the saturation of the next block. SW1 is the output band selected switch.

From the analysis above in Section 3.1, it can be seen that, if $C_p$ is very large, the Re[$Z'_{in}$] is very small (far less than 10 Ω), then, the input matching is very difficult. So, the value of $C_p$ must be reduced as far as possible. In order to have 2-kV ESD protection, the parasitic capacitor of the ESD circuit is about 200 fF[6]. So, there are only two ways to reduce the $C_p$ value. One is to use a low-capacitance PAD. In this paper, the octagonal-shaped pad with only the top metal was used at the

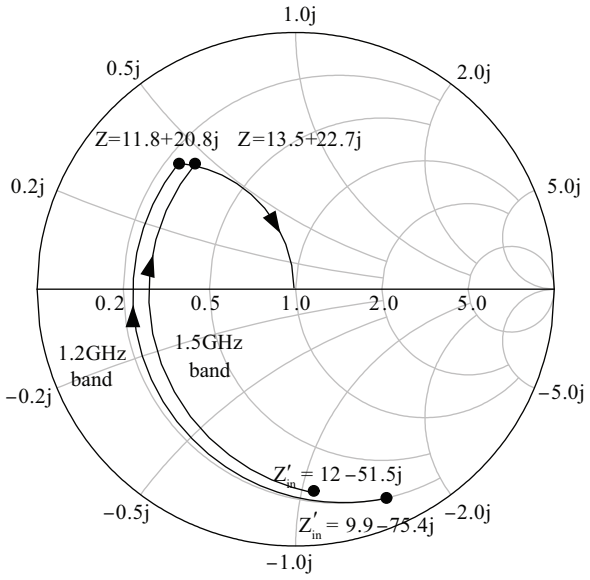


Fig. 4. Dual-band input impedance matching (assume $Q$ of the inductor is 50).

input port. The other was to reduce the capacitance of SW3. Reducing the size of SW3 can achieve low capacitance. In contrast, a small width means a small on-resistance, which may cause a large signal attenuation at the low gain (LG) mode. Therefore, the size of SW3 must be a trade off. Compared with SW3, the size of SW2 can be selected easily. It can be selected large enough to acquire small on-resistance, because its parasitic capacitance can be considered in the output matching network.

A single-end topology can save half power, compared to the differential topology. In addition, the on-chip inductor occupies a large chip area, the differential topology usually needs four on-chip inductors, but the single-end topology only needs one on-chip inductor. The source degenerated inductor can be realized by the bond wire, so the chip area of the single-end LNA is only about a quarter of the differential LNA.

The noise figure of the LNA can be expressed by[7]

$$F = 1 + \left(\frac{C_{\rm p}+C_1}{C_1}\right)^2 \frac{R_{\rm Lg}+R_{\rm cm}}{R_{\rm eq}} + \frac{r_{\rm g}}{R_{\rm eq}} + \frac{\gamma}{\alpha} g_{\rm m} R_{\rm eq} \left(\frac{\omega_0}{\omega_{\rm T}}\right)^2 \Upsilon + \eta^2 g_{\rm m}^2 R_{\rm sub} R_{\rm eq} \left(\frac{\omega_0}{\omega_{\rm T}}\right)^2 + \frac{\delta\alpha}{5 g_{\rm m} R_{\rm eq}} + \frac{4R_{\rm eq}}{R_{\rm d}} \left(\frac{\omega_0}{\omega_{\rm T}}\right)^2, \quad (3)$$

$$\Upsilon = 1 + 2c\sqrt{\frac{\delta}{5\gamma}}\alpha + \frac{\delta\alpha^2}{5\gamma}, \quad (4)$$

where $R_{\rm Lg}$ and $R_{\rm cm}$ are the series parasitic resistance of $L_{\rm g}$ and $C_{\rm m}$, respectively. $R_{\rm sub}$ is the substrate resistance, $R_{\rm d}$ is the equivalent load parallel resistor, $\omega_0$ is the operation frequency, $\alpha = g_{\rm m}/g_{\rm d0}$, $g_{\rm m}$ is the transconductance of M1, $g_{\rm d0}$ is the zero bias drain conductance, $\gamma$ is the channel current noise factor, $\delta$ is the gate induced current noise factor, $\eta$ is the bias-dependent constant and $c$ is the correlation coefficient between the gate and drain noise[9]. From Eq. (3), it can be seen that reducing $C_{\rm p}$, $R_{\rm Lg}$ and $R_{\rm cm}$ and adopting large $\omega_{\rm T}$ can result in a low noise figure.

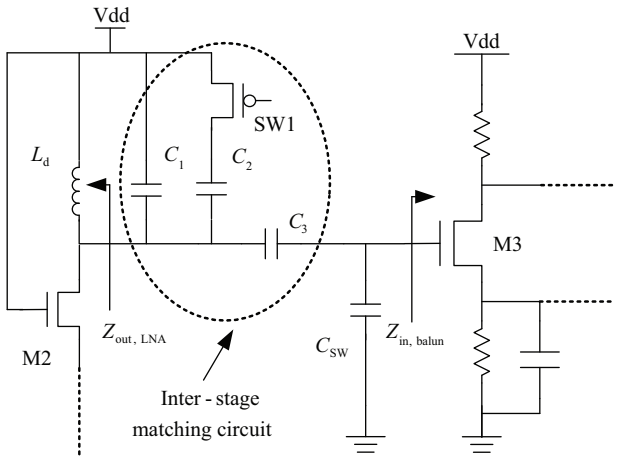


Fig. 5. Inter-stage matching of LNA and balun.

### 3.3. Inter-stage connection

In the fully integrated transceiver, the connection between two blocks is very important, especially at the RF frequency band. In this work, the connection between the LNA and the balun shown in Fig. 5 is analyzed. Since the output impedance of the LNA ($Z_{\rm out,\ LNA}$) is inductive while the input impedance of the balun ($Z_{\rm in,\ balun}$) is capacitive, the capacitors $C_1$, $C_2$, $C_3$ and $C_{\rm SW}$ (parasitic capacitance of SW2 and SW3) are used to realize the inter-stage connection. In order to acquire a high voltage gain, the load impedance of the LNA was adopted in a parallel resonance circuit that is made up by the MIM capacitors $C_1$, $C_2$, the drain capacitor of M2, the gate capacitance of M3, the parasitic capacitance $C_{\rm SW}$ and the load inductor $L_{\rm d}$. $C_3$ is the coupling capacitor. If the width of SW2 is large enough, the on-resistor can be ignored. Compared with the inter-stage LC-matching network, this connection structure needs less area.

The choice of inductor $L_{\rm d}$ must be a tradeoff. A larger $L_{\rm d}$ can achieve a higher gain of the LNA. But, if $L_{\rm d}$ is increased, the capacitance must be decreased in order to not change the resonant frequency. In order to meet the needs of the two bands, the switch capacitance, which is composed of SW1 and $C_2$, is used to change the resonant frequency.

### 3.4. Active balun

In order to connect the single-end LNA and the double balanced mixer, the active balun was added between them. Figure 6 shows the schematic of the active balun, which has three basic cells. The basic cell of the active balun uses the common-source amplifier with source degeneration to produce the differential output. This kind of topology has an advantage over the pseudo-differential pair converter. Since it has the source degeneration resistor, it can achieve higher linearity with low biasing current[8]. From the viewpoint of out+, the circuit is a source follower (SF) with a drain resistor. On the other hand, from the viewpoint of out–, the circuit is a common source (CS) amplifier with source degeneration. A capacitor $C_{\rm s}$ is added to compensate for the effect of the drain capacitance

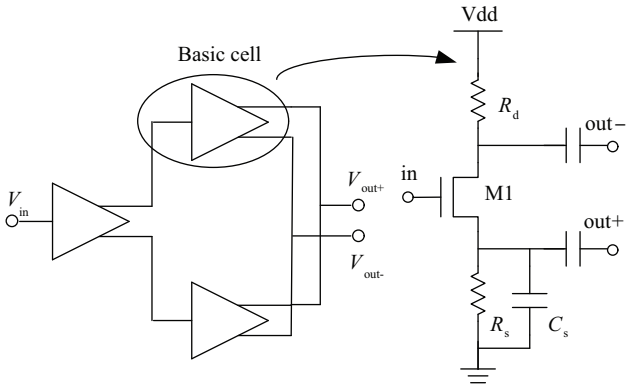


Fig. 6. Schematic of the broadband active balun and its basic cell.

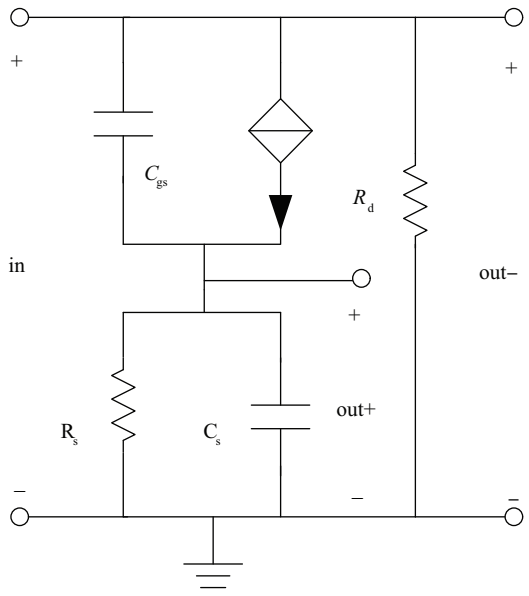


Fig. 7. Small-signal equivalent circuit of the basic cell.

of Ml on the phase of the differential output. From its small-signal equivalent circuit, shown in Fig. 7, the transfer functions of the two outputs can be derived as

$$H(s)_{\mathrm{SF}} = \frac{\left(sC_{\mathrm{gs}} + g_{\mathrm{m}}\right)\left(R_{\mathrm{s}} \parallel \dfrac{1}{sC_{\mathrm{s}}}\right)}{1 + \left(sC_{\mathrm{gs}} + g_{\mathrm{m}}\right)\left(R_{\mathrm{s}} \parallel \dfrac{1}{sC_{\mathrm{s}}}\right)} = \frac{R_{\mathrm{s}}\left[\left(g_{\mathrm{m}} + R_{\mathrm{s}}C_{\mathrm{gs}}C_{\mathrm{s}}\right) + sC_{\mathrm{gs}}\left(1 - g_{\mathrm{m}}R_{\mathrm{s}}\right)\right]}{\left(1 + R_{\mathrm{s}}^2C_{\mathrm{s}}^2\right)\left[1 + \left(sC_{\mathrm{gs}} + g_{\mathrm{m}}\right)\left(R_{\mathrm{s}} \parallel \dfrac{1}{sC_{\mathrm{s}}}\right)\right]}, \tag{5}$$

$$H(s)_{\mathrm{CS}} = \frac{-g_{\mathrm{m}}R_{\mathrm{d}}}{1 + \left(sC_{\mathrm{gs}} + g_{\mathrm{m}}\right)\left(R_{\mathrm{s}} \parallel \dfrac{1}{sC_{\mathrm{s}}}\right)}. \tag{6}$$

From Eqs. (5) and (6), it can be seen that, when

$$\frac{R_{\mathrm{s}}(g_{\mathrm{m}} + R_{\mathrm{s}}C_{\mathrm{gs}}C_{\mathrm{s}})}{1 + R_{\mathrm{s}}^2C_{\mathrm{s}}^2} = g_{\mathrm{m}}R_{\mathrm{d}}, \tag{7}$$

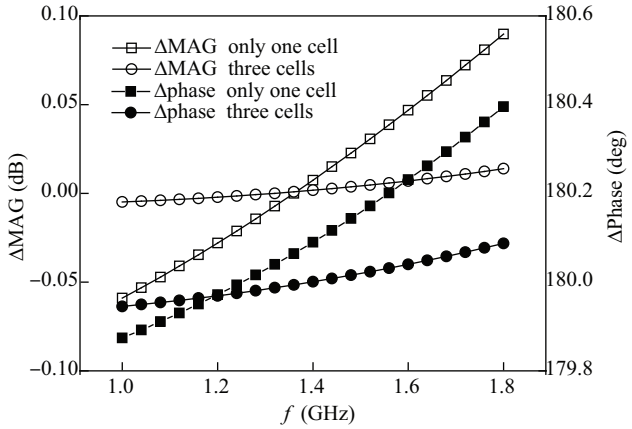


Fig. 8. Simulation results of the active balun.

$$g_{\mathrm{m}}R_{\mathrm{s}} - 1 = 0, \tag{8}$$

the two voltage gains have opposite sign. By adjusting the values of $R_{\mathrm{d}}$, $R_{\mathrm{s}}$ and $C_{\mathrm{s}}$, two outputs have the same voltage gains with a 180° phase shift. But the impedance of the compensation capacitor $C_{\mathrm{s}}$ is frequency dependant and does not suit broadband applications. In addition, the output impedances of the two ports are different. So, we use three cells hybrid connected, as shown in Fig. 6. The fully symmetrical topology of the active balun can acquire high bandwidth and the same output impedance. Figure 8 shows the differential characteristics of one cell and three cells. From Fig. 8, it can be seen that the magnitude and phase can be matched very well at one frequency using only one cell. However, the cascade topology can be matched very well during a large frequency range. The drawback of the cascade topology is that its power consumption is three times that of only one cell. Fortunately, the power consumption at this stage is very small.

### 3.5. IQ-mixer

As the last stage of the RF frontend, the mixer's linearity plays an important role in the whole system[9]. In the conventional Gilbert mixers, the linearity is mainly limited by the transconductor stage[10]. There are many methods to improve the transconductor stage's linearity. For example, the multi-tanh linearization technique is used to improve the linearity of the mixer by using a multiple paralleled transconductance stage[11]. In this method, the additional paralleled transconductance stages will increase the noise figure and the power consumption. The other one is a source degeneration technique. The main drawback of this method is that the negative feedback will decrease the voltage gain of the mixer. Furthermore, the resistive degeneration will increase the noise figure and reduce the voltage headroom. The inductive degeneration will occupy large chip areas. So, in this paper, the transconductor stage uses the multiple gated transistor (MGTR) technique[12], as shown in Fig. 9, to improve the linearity. The mixer is a modified double balanced Gilbert-cell. The tail current source is removed to acquire more voltage headroom, thus improving the linearity. Mp1 and Mp2 are the current bleeding devices to reduce the noise figure. In addition, the current bleeding technology can reduce the current flowing though the load resistors,

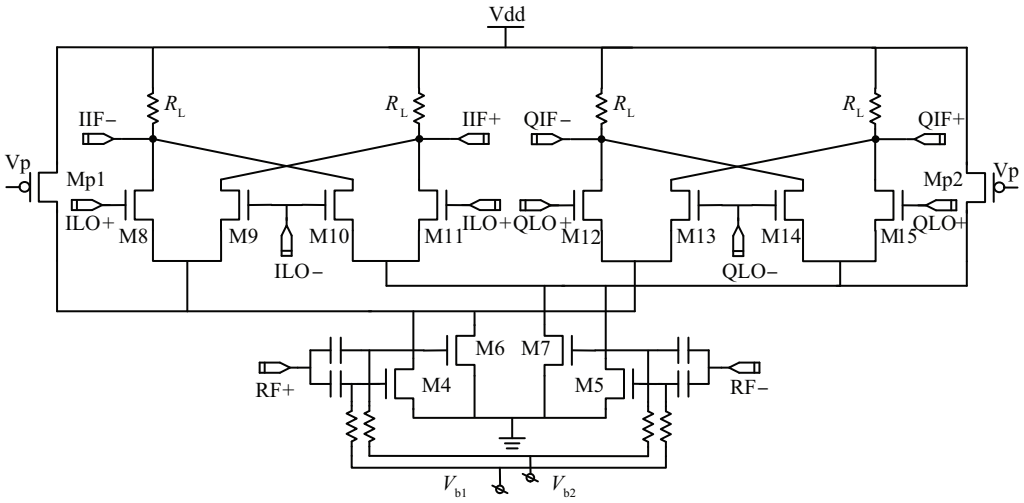


Fig. 9. Schematic of the high linear mixer.

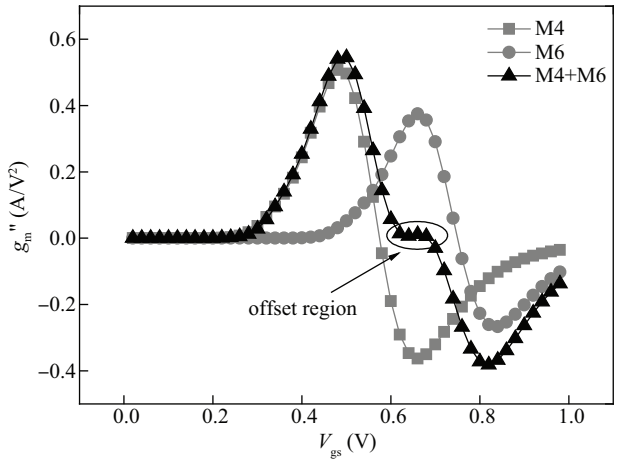


Fig. 10. Third-order nonlinear currents of the main FET and the auxiliary FET, and their summation.

thus allowing the use of large load resistors, which can increase the conversion gain. The load uses the poly resistor to achieve a high bandwidth and linearity. Besides this, the poly-Si resistors are free from flicker noise.

The MOSFETs of the MGTR topology work in two different regions. The main FETs (M4 and M5) operate in the saturation region and the auxiliary FETs (M6 and M7) operate in the sub-threshold region. The $g_m''$ of the main FETs can be off-set by the $g_m''$ of auxiliary FETs when the bias voltages and sizes are chosen carefully. Figure 10 shows the $g_m''$ offset mechanism. Because the auxiliary FET works in the sub-threshold region, its drain current is near zero, that is to say, this technique can improve the IIP3 of the mixer but does not consume additional power.

### 3.6. Bias circuits

The variations in the supply voltage and the temperature will affect the current in the circuit and the $S$-parameter of the devices. To solve those problems, the BGR bias circuit was adopted for the frontend to stabilize the gain and input impedance over the temperature and supply voltage variations. Figure 11 shows a schematic of the bias circuits.

The BGR voltage circuit produces a precise reference voltage ($V_{ref}$), which is independent of the temperature and supply voltage. The operational amplifier (OPA) makes the voltage on R_offchip equal to $V_{ref}$. That is to say, the current through R_offchip ($I_{ref}$) is independent of the temperature and the supply voltage too. The self bias circuits convert the currents which copy from the $I_{ref}$ to voltages for the LNA, the balun and the mixer. Between the bias circuits and the LNA, there is a power down circuit. When the PD is high, M1 is on, M2 is off and the bias voltage is added on the LNA. In contrast, when the PD is low, M1 is off, M2 is on, and M1 cuts off the connection of the bias circuit and the LNA. The bias of the LNA was connected to ground though M2. $C_{pass}$ is the bypass capacitor which uses the MOSFET capacitor to save the chip area.

## 4. Measurement and discussion

The RF front-end was fabricated in the TSMC 0.18-$\mu$m RF CMOS process. The micrograph of the front-end chip is shown in Fig. 12. The chip area including all bonding pads is $1327 \times 836\ \mu m^2$. The major test equipment includes an Agilent network analyzer E5071B, a spectrum analyzer E4440A, a RF signal generator E4438C and SMP04, a noise figure analyzer N8975A and a digital oscillograph 6102.

In this frontend, the input matching is very important. Before the chip test, the off-chip input matching network of the LNA, shown in Fig. 1, must be prepared. In this design, $L_s$ is realized by bond wire, and $L_g$ is composed of the input bond wire ($L_b$) and an off-chip SMD component ($L_m$). As the length of the bond wire ($L_s$ of LNA) is difficult to control very precisely, $Z'_{in}$ may have some difference with the post-simulation result. In addition, $L_b$ is difficult to control too. The length of input bond wire will affect the value of $L_m$. So, the matching method used in Ref. [13] is not suitable for this work and the values of $L_m$ and $C_m$ must be determined through testing. The matching procedure of bonding the LNA with an L-type network is as follows. First, port expansion. Extend the calibration plane from A to B, as shown in Fig. 13. Now, the influence of the transmission line $T_{in}$ is calibrated off. Second, bond the chip

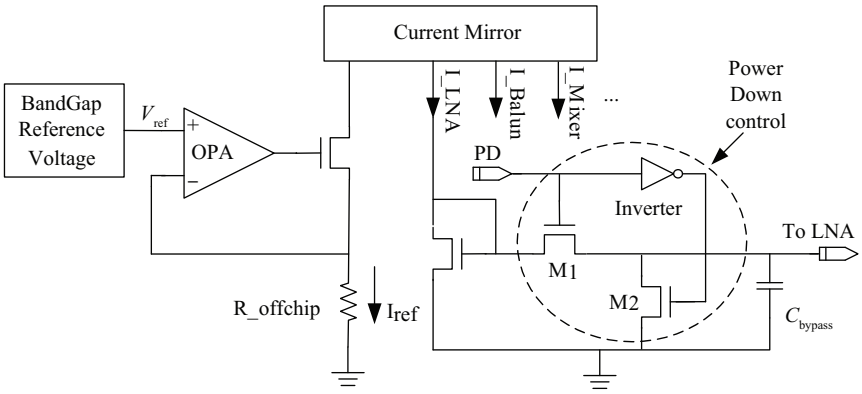


Fig. 11. Schematic of the bias circuit.

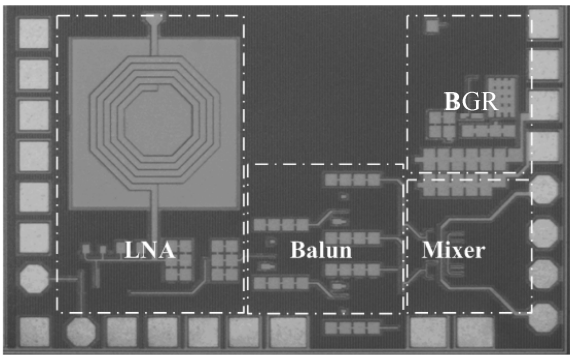


Fig. 12. Micrograph of the front-end.

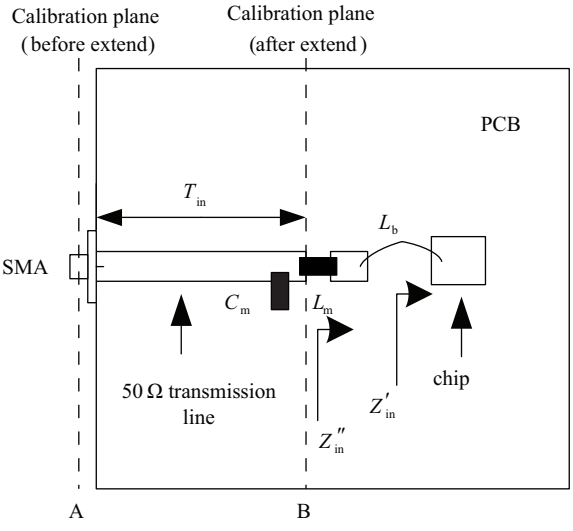


Fig. 13. Top view of the test board (not to scale).

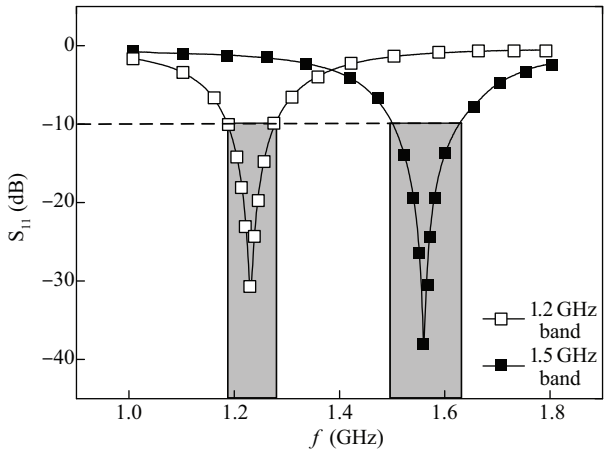


Fig. 14. Measured $S_{11}$ of the front-end in HG mode.

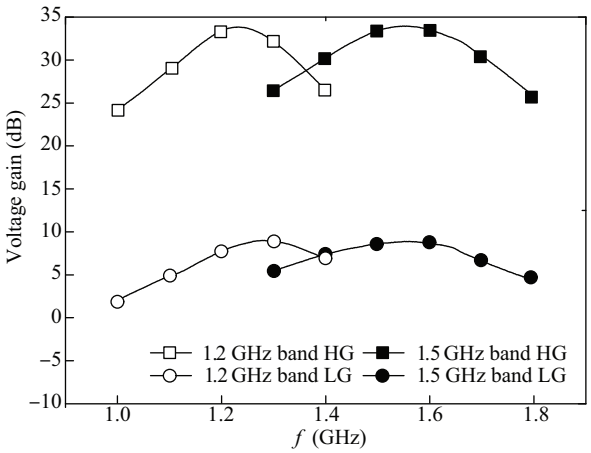


Fig. 15. Measured voltage gain in HG and LG modes.

on the PCB board and solder the zero-ohm resistor at the position of $L_m$. Then, test the input impedance $Z''_{in}$. Last, according to the test result of $Z''_{in}$, determine the value of $L_m$ and $C_m$, as shown in Fig. 4. In order to avoid the deterioration of NF due to the parasitic resistance of $L_m$ and $C_m$, high $Q$ components can be used. In this work, the ATC inductor was used. (The $Q$ of a 12 nH inductor is about 62 at 1.2 GHz and the $Q$ of a 7.4 nH inductor is about 79 at 1.575 GHz.)

Figure 14 shows the measured results of the input matching performance in the range of 1–1.8 GHz. By using the matching method described above, $S_{11}$ is about –28 dB at 1227.6 MHz and –23 dB at 1575.42 MHz. Figure 15 shows the measured conversion gain of the front-end at two bands. The conversion gain is about 33.8 dB at 1227.6 MHz and 33.9 dB at 1575.42 MHz. Figures 16 and 17 show the measured results of the linearity performance. Under the bypass mode, the 1-dB compression point is 0 dBm at 1227.6 MHz and

Table 1. Performance comparisons between recently published frontends.

| Parameter | This work | This work | Ref. [14] | Ref. [15]** | Ref. [16] | Ref. [17] |
|---|---|---|---|---|---|---|
| Freq (MHz) | 1227.6 | 1575.42 | 1575.42 | 1575.42 | 1575.42 | 1575.42 |
| Gain (dB) | 33.9/8.8* | 33.8/8.4* | 36 | 35 | 38 | 11.4 |
| $S_{11}$ (dB) | –28 | –23 | –20 | –17.7 | Na | –24.5 |
| $P_{1dB}$ (dBm) | –25.5/0* | –24/1* | –31 | –38 | –31.6 | –6.2 |
| IIP3 (dBm) | –10/5* | –10.5/5.5* | –19 | Na | –20.2 | 6.1 |
| NF (dB) | 2.1 | 2.0 | 4.8 | 3.3 | 1.8 | 5.87 |
| ΔMag (dB) | < 0.05 | < 0.08 | Na | Na | Na | Na |
| Δphase (deg) | < 0.8 | < 0.6 | Na | Na | Na | Na |
| Process (nm) | 180 | 180 | 130 | 180 | 90 | 350 |
| Topology*** | sed-LNA+balun +diff-mixer | sed-LNA+balun +diff-mixer | Full-sed | Balun-LNA +diff-mixer | Balun-LNA +diff-mixer | Full-diff |
| Power (mW) | 16 | 16 | 5.4 | 10 | 36 | 40.9 |

* Correspond to the HG and the LG mode, respectively. **Simulation results. ***sed and diff mean single-ended and differential topology, respectively.

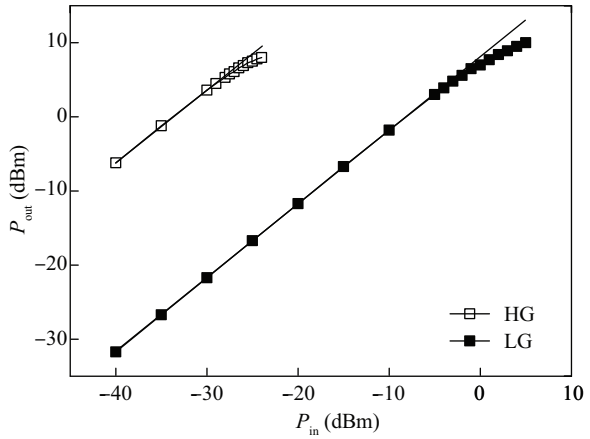


Fig. 16. Measured input 1 dB compression point at 1.2 GHz band.

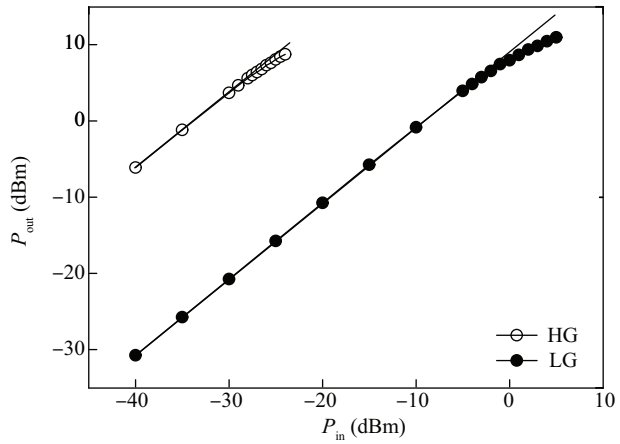


Fig. 17. Measured input 1 dB compression point at 1.5 GHz band.

1 dBm at 1575.42 MHz. Table 1 gives the measured results of the proposed frontend compared to recently published works. The NF of 1575.42 MHz is lower than 1227.6 MHz, which is due to the higher $Q$ factor of $L_m$. From Table 1, it can be seen that the proposed frontend achieves a low noise figure and high linearity under low power consumption.

## 5. Conclusions

A dual-band multi-mode RF front-end for a navigation receiver in a 0.18-$\mu$m RF CMOS process is presented. In order to work at two frequency bands, a reconfigurable LNA and broad band active balun were used. The LC input matching network makes the LNA work under low power consumption. To increase the linearity of the frontend, MGTR technology was employed. The measured results show that the frontend can be used for the four navigation systems.

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