Reset noise reduction through column-level feedback reset in CMOS image sensors*

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Abstract: A low reset noise CMOS image sensor (CIS) based on column-level feedback reset is proposed. A feedback loop was formed through an amplifier and a switch. A prototype CMOS image sensor was developed with a 0.18 μm CIS process. Through matching the noise bandwidth and the bandwidth of the amplifier, with the falling time period of the reset impulse 6 μs, experimental results show the reset noise level can experience up to 25 dB reduction. The proposed CMOS image sensor meets the demand of applications in high speed security surveillance systems, especially in low illumination.

Key words: CMOS image sensor; reset noise; feedback reset; five-transistor pixel; global shutter
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1. Introduction

Nowadays, high speed security systems are widely used, and the global shutter CMOS image sensor (CIS) is preferred because a rolling shutter causes motion blur as each line of pixels is integrating light at a slightly different moment in time[1]. However, in global shutter CIS with a pixel transistor count of less than 6, correlated double sampling (CDS) cannot be used[1], which makes reset noise relatively higher in five transistor global shutter CIS. In order to suppress the reset noise as much as possible, active reset noise reduction[2] and capacitive control[3] have been reported, but these methods employ an added transistor per pixel to control the gate of the reset transistor. In this paper, a reset noise reduction technique through column-level feedback reset is proposed. With the feedback reset, the reset noise is suppressed without extra transistors in the pixel.

Figure 1 is the five-transistor pixel structure diagram[4]. The five-transistor active pixel employs the pinned photodiode (PPD). M1 is the reset transistor with the control signal RST at its gate terminal. M2 is the transfer gate with the control signal TCK at its gate terminal. M3 is the source follower. M4 is the row selection transistor with the control signal SEL at its gate terminal. M5 is the global reset transistor with the pixel reset signal PR at its gate terminal.

The working principle of the five-transistor pixel in this paper is shown in Fig. 2. At first, the PR sets all of the sensing nodes at a high voltage level. When the PR shifts to a low level, integration begins. When the TCK shifts to a high level, integration ends and the signal voltage is transferred from the sensing node to the storage node. In this mechanism, the signal voltage is stored in the storage node until it is read out. Therefore, the correlated double sampling (CDS), which aims to reduce temporal noise by sampling the reset and signal voltage of one frame and by subtracting the latter from the former, cannot be used in a five-transistor pixel structure. Temporal noise sets the fundamental limit on image sensor performance, especially under low illumination[5].

2. Reset noise reduction

2.1. Reset noise

During the reset operation, the reset transistor M1 can be represented by a resistor R whose cross voltage drop is represented by a series voltage v_{R}, as shown in Fig. 3. The thermal noise spectral density of a resistor with a value R is give by

$$S_{\mathrm{R}}(f) = 4kTR, \quad f \geqslant 0. \tag{1}$$

Here T is the absolute temperature and k is Boltzmann's constant. The resistor R and the FD node capacitor C_{FD} constitute a low-pass filter, so that the noise spectral density at node FD

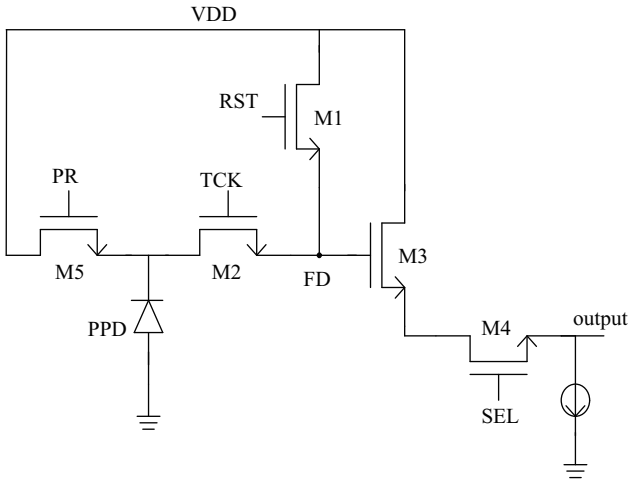

Fig. 1. Pixel structure diagram.

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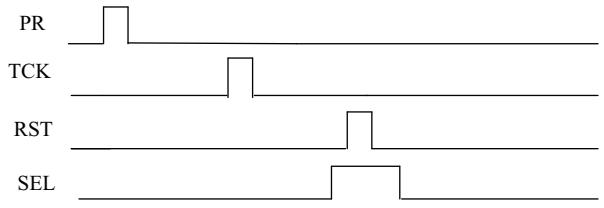

Fig. 2. Timing diagram.

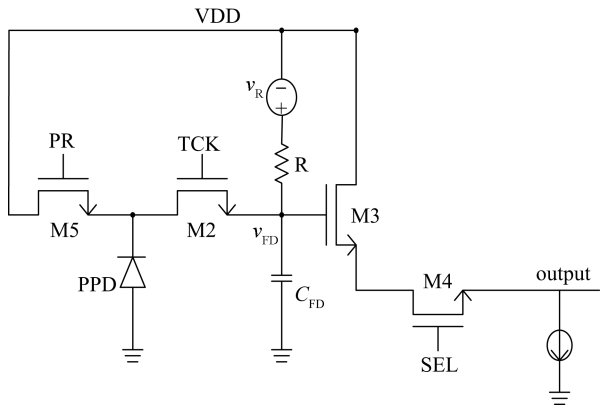

Fig. 3. Equivalent circuit of five-transistor pixel.

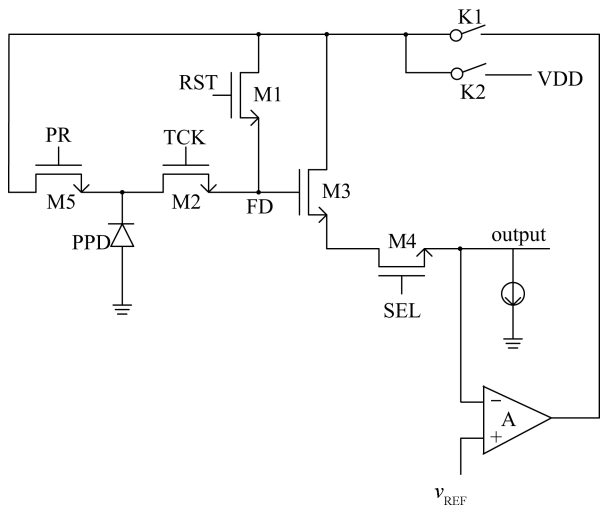

Fig. 4. Proposed feedback reset schematic.

is

$$S_{FD}(f) = \frac{4kTR}{1 + (2\pi fRC_{FD})^2}. \tag{2}$$

The mean square noise at node FD is

$$v_{FD}^2 = \int_0^\infty S_{FD}(f)\mathrm{d}f = 4kTR\int_0^\infty \frac{1}{1 + (2\pi fRC_{FD})^2}\mathrm{d}f$$
$$= 4kTR\frac{1}{4RC_{FD}} = \frac{kT}{C_{FD}}. \tag{3}$$

So reset noise is often called kT/C noise as well. Equation (3) indicates that the reset noise is independent of its resistance.

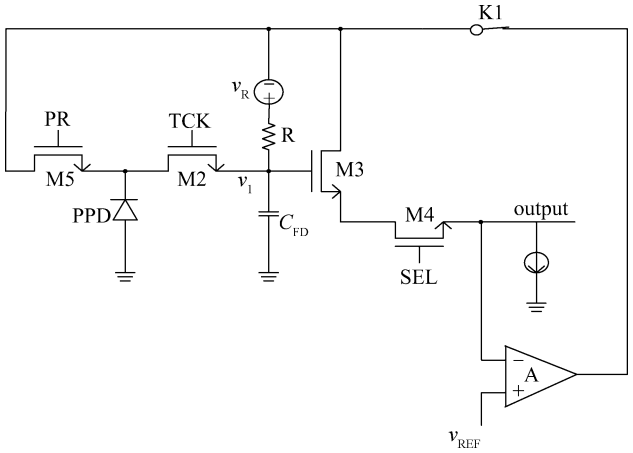

Fig. 5. Equivalent circuit of proposed feedback reset.

2.2. Principle of reset noise reduction

Figure 4 shows the principle of the proposed reset noise reduction through column-level feedback reset operation. Amplifier A and switches K1 and K2 are employed. The amplifier is used to fix the reset voltage of the reset transistor and connect the output of the amplifier with the power supply, which builds the circuit relevance of the reset transistor to reduce its reset noise. The noise stored on the node FD is reduced because the feedback loop acts to minimize the difference between the voltage on the node FD and a fixed reference voltage V_{REF}. The mathematical analysis is given as follows.

The circuit operates in two modes: the first is when the photodiode is being readout and the second is when the photodiode is being reset. In the signal readout mode, K1 is off and K2 is on, and the feedback loop is off. In the reset mode, K1 is on and K2 is off. The feedback loop, which includes M1, M3, M4, amplifier A and K1, is formed. Figure 5 shows the model of the feedback loop, where A is the gain of the amplifier. For simplicity of analysis, we assume that M3 and M4 behave as an ideal transistor with no noise. The voltage at node FD v_1 is calculated as

$$(0 - v_1)A = v_1 - v_R, \tag{4}$$

$$v_1 = \frac{v_R}{1 + A}. \tag{5}$$

The noise spectral density of v_1 is

$$S_1(f) = \frac{4kTR}{(1 + A)^2}\frac{1}{1 + (2\pi fRC_{FD})^2}. \tag{6}$$

Since M1 is in sub-threshold region, its drain-to-source resistance R is very large. The dominant pole in the feedback loop is determined by R and C_{FD}. To keep the stability of the loop, the amplifier A preferably has a much wider bandwidth than the dominant pole frequency.

When the amplifier's bandwidth is wider than the dominant pole frequency, the mean square value of the noise voltage

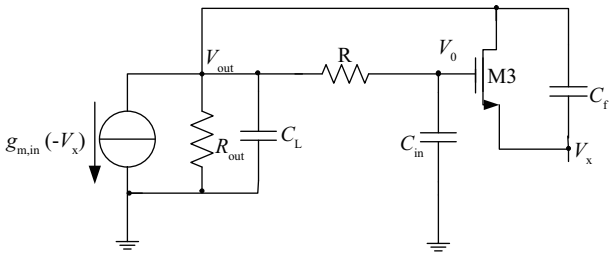

Fig. 6. Equivalent circuit.

at node FD is

$$v_1^2 = \int_0^\infty S_1(f)\mathrm{d}f = \frac{4kTR}{(1+A)^2}\int_0^\infty \frac{1}{1+(2\pi f R C_{\mathrm{FD}})^2}\mathrm{d}f = \frac{4kTR}{(1+A)^2}\frac{1}{4RC_{\mathrm{FD}}} = \frac{1}{(1+A)^2}\frac{kT}{C_{\mathrm{FD}}}. \tag{7}$$

Compared with the standard reset noise, the mean square noise is reduced by a factor of $(1+A)^2$, and the effective capacitance at node FD is $(1+A)^2 C_{\mathrm{FD}}$.

When the dominant pole frequency is wider than the amplifier's bandwidth, the mean square value of noise voltage at node FD includes two parts: in the amplifier's bandwidth and beyond the amplifier's bandwidth. In the amplifier's bandwidth, the amplifier has enough response time in the negative feedback loop, and the noise spectral density is $S_1(f)$. Beyond the amplifier's bandwidth, the feedback loop cannot work, and the noise spectral density is $S_{\mathrm{FD}}(f)$.

$$\begin{aligned} v_1^2 &= \int_0^{\frac{w_0}{2\pi}} S_1(f)\mathrm{d}f + \int_{\frac{w_0}{2\pi}}^\infty S_{\mathrm{FD}}(f)\mathrm{d}f \\ &= \frac{4kTR}{(1+A)^2}\int_0^{\frac{w_0}{2\pi}} \frac{1}{1+(2\pi f R C_{\mathrm{FD}})^2}\mathrm{d}f \\ &\quad + 4kTR\int_{\frac{w_0}{2\pi}}^\infty \frac{1}{1+(2\pi f R C_{\mathrm{FD}})^2}\mathrm{d}f \\ &= \frac{2kT\arctan RC_{\mathrm{FD}}w_0}{\pi C_{\mathrm{FD}}(1+A)^2} + \frac{2kT}{\pi C_{\mathrm{FD}}}\left(\frac{\pi}{2} - \arctan RC_{\mathrm{FD}}w_0\right) \\ &\approx \frac{2kT}{\pi C_{\mathrm{FD}}}\left(\frac{\pi}{2} - \arctan RC_{\mathrm{FD}}w_0\right), \end{aligned} \tag{8}$$

w_0 is the amplifier's bandwidth, which can be calculated in the equivalent circuit of the feedback loop, as shown in Fig. 6. V_{x} is the input voltage. V_{out} is the output voltage. g_{m} is the input transconductance of the amplifier. g_{msf} is the transconductance of the M3. R_{out} is the output resistance of the amplifier. C_{in} is the input capacitance of the amplifier. C_{f} is the feedback capacitance. C_{L} is the load capacitance of the amplifier. V_0 is the voltage in FD. Equation (9) is the equation according to Kirchhoff's current law. Applying Eq. (9) to Eq. (10), it is found that the transfer function of the feedback amplifier is Eq. (11). The feedback amplifier loop bandwidth w_0 approximately equals its pole position, as shown in Eqs. (12) and (13),

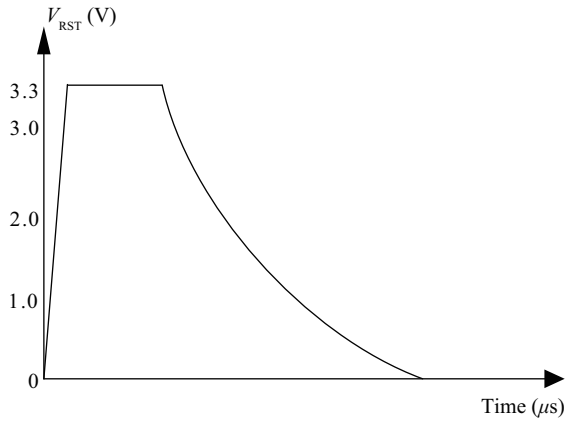

Fig. 7. Reset signal pulse.

$$g_{\mathrm{m}}(-V_{\mathrm{x}}) + V_{\mathrm{out}}\left(\frac{1}{R_{\mathrm{out}}} + sC_{\mathrm{L}}\right) + \frac{V_{\mathrm{out}}}{R + \dfrac{1}{sC_{\mathrm{in}}}} + g_{\mathrm{msf}}(V_0 - V_{\mathrm{x}}) + sC_{\mathrm{f}}(V_{\mathrm{out}} - V_{\mathrm{x}}) = 0, \tag{9}$$

$$V_0 = V_{\mathrm{out}}\frac{1}{sC_{\mathrm{in}}}\Big/\left(\frac{1}{sC_{\mathrm{in}}} + R\right), \tag{10}$$

$$\frac{V_{\mathrm{out}}}{V_{\mathrm{x}}} = \frac{g_{\mathrm{m}} + g_{\mathrm{msf}} + sC_{\mathrm{f}}}{\dfrac{1}{R_{\mathrm{out}}} + sC_{\mathrm{L}} + sC_{\mathrm{f}} + \dfrac{sC_{\mathrm{in}}}{sC_{\mathrm{in}}R+1} + \dfrac{g_{\mathrm{msf}}}{sC_{\mathrm{in}}R+1}}, \tag{11}$$

$$\begin{aligned} w_0 \approx \Big(&RC_{\mathrm{in}} + R_{\mathrm{out}}C_{\mathrm{in}} + R_{\mathrm{out}}(C_{\mathrm{f}} + C_{\mathrm{L}}) \\ &- \left\{[RC_{\mathrm{in}} + R_{\mathrm{out}}C_{\mathrm{in}} + R_{\mathrm{out}}(C_f + C_{\mathrm{L}})]^2\right. \\ &\left. - 4RR_{\mathrm{out}}C_{\mathrm{in}}(C_{\mathrm{f}} + C_{\mathrm{L}})(g_{\mathrm{m,SF}}R_{\mathrm{out}} + 1)\right\}^{1/2}\Big) \\ &\times [2RR_{\mathrm{out}}C_{\mathrm{in}}(C_{\mathrm{f}} + C_{\mathrm{L}})]^{-1}, \end{aligned} \tag{12}$$

$$f(R) = RC_{\mathrm{FD}}w_0. \tag{13}$$

Equation (14) is the derivative of $f(R)$, and it is always larger than zero. Therefore, $RC_{\mathrm{FD}}w_0$ is a monotonic increasing function of R, and v_1^2 in Eq. (8) is a monotonic decreasing function of R. That is, as R increases, the mean square reset noise voltage decreases, which could also be explained as follows. As R increases, both of the reset noise and amplifier loop bandwidth decrease, yet the former decreases faster, which makes the reset noise diminish as a result.

As shown in Fig. 7, the method to increase R can be realized by slowly shutting down the reset transistor M1, which extends the high impedance period of the reset transistor to allow the feedback amplifier enough response time in the feedback loop.

However, the drain-to-source resistance R is

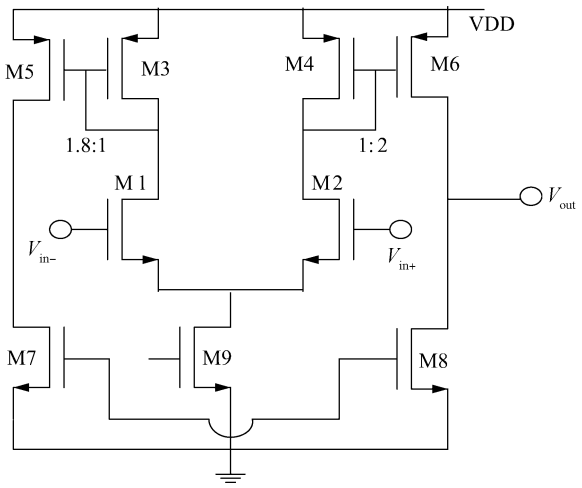

Fig. 8. Structure of the amplifier.

Table 1. Amplifier sizes.

Transistor	$W/L(\mu m/\mu m)$
M3 ($m = 5$), M4 ($m = 5$), M5 ($m = 9$), M6 ($m = 10$)	4/0.85
M1, M2	5/0.5
M7, M8	5/0.8
M9	10/0.5

$$f'(R) = \frac{C}{2R_{\text{out}}C_{\text{in}}(C_{\text{f}}+C_{\text{L}})}\Big\{C_{\text{in}} - \frac{1}{2}\big\{2C_{\text{in}}[RC_{\text{in}} + R_{\text{out}}C_{\text{in}} + R_{\text{out}}(C_{\text{f}}+C_{\text{L}})] - 4R_{\text{out}}C_{\text{in}}(C_{\text{f}}+C_{\text{L}})(g_{\text{m,SF}}R_{\text{out}}+1)\big\} \times \big\{[RC_{\text{in}} + R_{\text{out}}C_{\text{in}} + R_{\text{out}}(C_{\text{f}}+C_{\text{L}})]^2 - 4RR_{\text{out}}C_{\text{in}}(C_{\text{f}}+C_{\text{L}})(g_{\text{m,SF}}R_{\text{out}}+1)\big\}^{-1/2}\Big\}, \tag{14}$$

also the amplifier's load resistance. The amplifier's bandwidth is reduced due to the high impedance period of the reset transistor. So the falling edge time of reset transistor should be optimized.

3. Circuit implementation and measurement results

Figure 8 shows a schematic of the amplifier which is employed in the loop. Table 1 shows the size of the amplifier. The open-loop DC gain is found to be 33 dB, unity gain-bandwidth to be 41 MHz and phase margin 76°. As mentioned in the previous section, the reset-noise-reduction effect is intended to be observed through slowly shuttering down the reset transistor to magnify its resistance. Six different fall time periods of the reset impulse are set as 1, 2, 3, 4, 6, and 10 μs, which are basically realized by a 3–8 decoder to choose the reset signal's falling edge time period. The proposed reset noise reduction through column-level feedback reset has been employed in a prototype CMOS image sensor. This sensor was fabricated based on a 0.18 μm CIS process. In the dark condition (0 lux), the output pixel root mean square (RMS) noise is measured with and without feedback reset. With the proposed feedback reset, the falling time periods of reset impulse were set as 1 , 2, 3, 4, 6, and 10 μs. Figure 9 shows photographs of the CMOS image sensor chip and the evaluation board. The random noise is reduced by about 90%, as shown in Fig. 10, while it is reduced by 75% in Ref. [2].

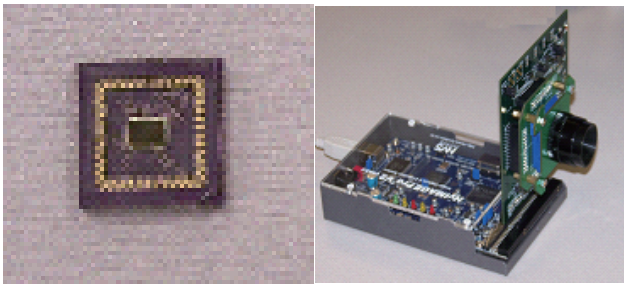

Fig. 9. Photographs of the chip and evaluation board.

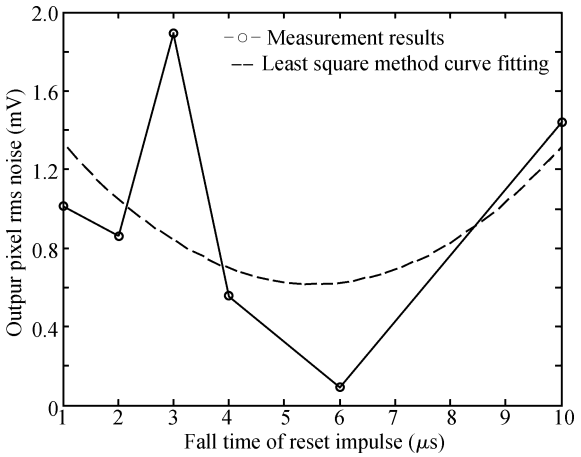

Fig. 10. Measurement result.

Table 2. Measured output noise.

Parameter	Value
Without the feedback reset	1.754759 mV
With the feedback reset	0.091556 mV
Improvement in noise	25 dB

The round curve is the measurement result and the dashed curve is the least square method curve fitting. This indicates that the optimized falling time period is 6 μs. The optimized value is not 10 μs because the falling-edge time extends longer than the readout signal and the reset transistor doesn't shut down completely, which reduces its resistance. That is also the reason why different falling-edge times are employed in this paper to choose an optimized falling-edge time. Table 2 shows the measurement result of the reset noise.

4. Conclusion

A reset noise reduction technique through a column-level feedback reset in a CMOS image sensor is proposed. It is de-

signed with six different falling-edge time periods of the input impulse of the reset transistor to choose one with an optimized reset-noise-reduction effect. It is found that the reset noise level can have up to 25 dB reduction when the optimal noise performance when the falling-edge time period of the input pulse of the reset transistor is set to 6 μs.

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