Selective wet etch of a TaN metal gate with an amorphous-silicon hard mask*

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Abstract: The appropriate wet etch process for the selective removal of TaN on the HfSiON dielectric with an amorphous-silicon (a-Si) hardmask is presented. SC1 ($NH_4OH : H_2O_2 : H_2O$), which can achieve reasonable etch rates for metal gates and very high selectivity to high-*k* dielectrics and hardmask materials, is chosen as the TaN etchant. Compared with the photoresist mask and the tetraethyl orthosilicate (TEOS) hardmask, the a-Si hardmask is a better choice to achieve selective removal of TaN on the HfSiON dielectric because it is impervious to the SC1 etchant and can be readily etched with NH_4OH solution without attacking the TaN and the HfSiON film. In addition, the surface of the HfSiON dielectric is smooth after the wet etching of the TaN metal gate and a-Si hardmask removal, which could prevent device performance degradation. Therefore, the wet etching of TaN with the a-Si hardmask can be applied to dual metal gate integration for the selective removal of the first TaN metal gate deposition.

Key words: TaN; wet etching; metal gate; high *k* dielectric; hardmask; integration
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1. Introduction

As MOSFET dimensions scale down to 45 nm nodes and beyond, there is an urgent need to introduce metal gate electrodes and high-*k* gate dielectrics into complementary metal–oxide–semiconductor (CMOS) technologies[1]. Replacing poly gate electrodes with dual metal gates with work functions near the band-edges of Si can eliminate poly depletion, boron penetration and Fermi level pinning[2−4]. Replacing SiO_2 or SiON gate dielectrics with high-*k* gate dielectrics can reduce the gate direct tunneling leakage current and power consumption[2, 4]. A versatile method of integrating dual metal gate CMOS is to employ a metal wet etch process to selectively remove the first metal from either the NMOS or PMOS region before depositing the second metal, because the wet etch could reduce possible plasma damage to the high-*k* dielectric from energetically charged particles compared with the dry etch[5]. However, this method presents a critical challenge in that the high-*k* dielectric in the second-metal area is exposed during selective removal of the first metal and hardmask, so the high-*k* dielectric in this area can be damaged significantly if the material is susceptible to the wet etch chemical[6]. Therefore, development of a reliable wet etch module is an integral part of the overall high-*k*/dual metal gate integration.

In this article, we will introduce an appropriate selective wet etch process of a TaN metal gate for the HfSiON/TaN gate stacks with the a-Si hardmask. The wet chemical etchant of the TaN metal gate and proper selection of the hardmask are discussed. The key process of selective removal of TaN on the HfSiON dielectric with an a-Si hardmask, such as a plasma etch of the a-Si hardmask, selective wet etch of the TaN metal gate and the removal of the remaining hardmask, are also demonstrated. The use of SC1 to etch the TaN metal gate with the a-Si hardmask may be a potential solution for dual metal gate CMOS device integration.

2. Experimental

After a standard cleaning process, the HfSiON (30 Å) film was deposited onto the SiO_2 interface layer by co-sputtering of Hf and Si targets in an Ar/N_2 ambience. A TaN metal gate was deposited on the HfSiON that annealed by rapid thermal annealing (RTA) at 900 ℃ for 30 s through reactive sputtering of the Ta target in Ar/N_2 ambient. Then the a-Si hardmask was deposited by LPCVD at 550 ℃ and etched with a Cl_2/HBr gas mixture in a LAM Rainbow 4420, which is a plasma etching system with 4 inch wafers. Wet etches were performed in a beaker set-up by immersing the sample into the etch solution. After etching, samples were rinsed in deionized water ten times and dried by N_2 flow. TaN and a-Si etch rates were obtained by means of step height measuring with a VEECO/Dektak 150 surface profilometer and a nanospectrometer/AFT film thickness measurement system, respectively. The surface morphology was measured using AFM in tapping mode on an area of 1×1 μm with a tip radius of less than 10 nm. The cross section of the samples was taken using a Hitachi S-4800 cold field emission scanning electron microscope.

3. Results and discussion

3.1. Wet etch etchant of the TaN metal gate

The choice of the first metal removal etchant is a crucial factor in dual metal gate CMOS integration as the first metal needs to be removed completely as well as not losing or roughening the underneath dielectric layer. Since the wet etch process for the deposition-etch-deposition integration method depends on the metal gate, hardmask and high-*k* dielectric wet etch rate for a given process, the etchant of the TaN metal gate should have a high etch rate for the TaN material and a very low

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Table 1. Etch rates of TaN, HfSiON, a-Si and TEOS by SC1.

SC1 (volume ratio)	Temperature (℃)	TaN (Å/min)	HfSiON (Å/min)	a-Si (Å/min)	TEOS (Å/min)
$NH_4OH : H_2O_2 : H_2O = 1 : 1.1 : 10$	60	16	0.11	0.42	3.52
$NH_4OH : H_2O_2 : H_2O = 1 : 1.1 : 5$	60	26.3	0.13	0.52	3.92
$NH_4OH : H_2O_2 = 1 : 2$	60	167	1.2	1.03	7.28

etch rate for the gate dielectric and hardmask materials. The common acids and alkalis, such as HF, HCl, HNO_3, H_3PO_4, H_2SO_4, aqua-regia and NH_4OH, either could not etch TaN or the etch rates of TaN were below several Å/min[7], but it was found that SC1 offers fast removal rates for TaN and high selectivity to high-*k* dielectric and hardmask. So, SC1 was the effective chemistry for the TaN metal gate wet-etch. Additional efforts were made to optimize the different concentrations of SC1 at various temperature conditions. Etch rates of TaN, HfSiON, a-Si and TEOS hardmasks by SC1 with different concentrations at 60 ℃ are shown in Table 1. SC1 with a volume ratio of 1 : 1.1 : 5 ($NH_4OH : H_2O_2 : H_2O = 1 : 1.1 : 5$) at 60 ℃ was optimized as an ideal etchant for the selective etch process of TaN since this etchant not only had a reasonable and controllable TaN etch rate (26.3 Å/min) but also had high selectivity to HfSiON (202 : 1), a-Si (51 : 1) and TEOS (7 : 1).

3.2. Choice of the etch mask

Mask material of the first TaN metal gate must be chosen carefully, since the mask material should be kept stable during the TaN wet etch by SC1 solution and the remaining mask removal step should not attack the exposed gate dielectric and the TaN metal gate. The process window of the TaN wet etch by SC1 with a photoresist mask is very small and a suitable hardmask is a better choice because the photoresist mask could only remain stable in the SC1 for a short time, and the standard PR descum process gives rise to serious surface oxidation of the TaN inhibiting SC1 solution etching at the first etching stage[8]. In addition, since SC1 solution has a high enough selectivity to the TEOS hardmask (as shown in Table 1), selective removal of the TaN metal gate on the HfSiON dielectric with the TEOS hardmask could be achieved, but the removal of the remaining hardmask by dilute HF solution results in a vigorous attack on the HfSiON gate dielectric[9]. Therefore, the TEOS hardmask is not compatible with the HfSiON gate dielectric and we decided to use a-Si as the hardmask because this is impervious to the SC1 etchant of TaN and can be easily removed by NH_4OH solution without damaging the TaN and the exposed HfSiON.

It was found that the a-Si hardmask deposited by LPCVD at 550 ℃ almost could not be etched within one minute with various concentrations of NH_4OH solutions at 60 ℃ because native oxide is easily grown on a-Si after brief exposure to the environment. Pretreating the a-Si hardmask with dilute HF is a conventional way to eliminate the native oxide, but it is also not compatible with HfSiON. Hence, we have to directly use NH_4OH solution to etch an a-Si hardmask, although the etch rate is very slow at the beginning. For example, the 65 nm a-Si hardmask could be removed clearly by NH_4OH solution ($NH_4OH : H_2O = 1 : 10$) at 60 ℃ with an average etch rate of 93 Å/min. In addition, NH_4OH solution ($NH_4OH : H_2O = 1 : 10$) at 60 ℃ almost did not etch the HfSiON and TaN materials, indicating that a-Si hardmask removal is compatible with the HfSiON dielectric and the TaN metal gate. So, an a-Si hardmask is a suitable choice for the HfSiON/TaN gate stacks.

3.3. TaN wet etch with an a-Si hardmask

A wet etch process for the selective removal of TaN on the HfSiON dielectric with an a-Si hardmask has been developed for dual metal gate integration, since SC1 has very high selectivity to high-*k* dielectrics and hardmask materials and a-Si hardmask removal is compatible with the HfSiON gate dielectric. Figure 1 sequentially presents the SEM images at each step of the formation process of 150 Å TaN selective removal on the HfSiON dielectric with a 650 Å a-Si hardmask. First, a dry etch developed from a poly etch recipe was used to remove the a-Si hardmask to open the underneath of the TaN metal gate after lithography on the HfSiON/TaN/ a-Si gate stack. To avoid oxidation of the metal layer affecting the SC1 solution etching, oxygen is omitted from the a-Si plasma etch process. This process etched out the exposed a-Si hardmask and stopped on the TaN metal gate, as shown in Fig. 1(a). After the dry etch for an a-Si hardmask and photoresist removal, an SC1 wet etch plus a 30% over etch with a volume ratio of 1 : 1.1 : 5 at 60 ℃ was used to remove the exposed TaN metal gate without affecting the underlying HfSiON film and the remaining a-Si hardmask, as shown in Fig. 1(b). Although a less than 15 nm undercut of TaN metal gate appeared, we proposed that there should be plenty of margin between the actual gate area to be defined by the gate-stack dry etch and the edge of the first metal gate defined by the metal wet etch because the current 45 nm design rule requires about 100 nm of isolation space and another 100 nm between the gate and the isolation space[10]. Also, the complete removal of TaN by SC1 was confirmed by the energy dispersive spectrometer (EDS, not shown here), which showed no Ta element remaining on the HfSiON high-*k* dielectrics. Finally, the remaining a-Si hardmask was removed from the TaN metal gate using NH_4OH (1 : 10) solution at 60 ℃, as shown in Figs. 1(c) and 1(d). The a-Si hardmask was completely removed without affecting the underlying TaN metal gate and the already exposed HfSiON dielectric film.

In order to prevent device degradation, the HfSiON dielectric surface should be smooth after the wet etch of the TaN metal gate and the a-Si hardmask. So, HfSiON film surfaces were carefully studied using AFM after every wet etch step. Figure 2(a) shows the HfSiON surface topography after selective removal of the TaN with an a-Si hardmask. It was smooth with R_{rms} = 1.76 Å, which is comparable to that as deposited HfSiON film (R_{rms} = 1.59 Å, not shown here). A little increase in HfSiON film likely resulted from the TaN deposition process by the PVD and TaN wet etch. Figure 2(b) presents AFM images of the HfSiON surface after the TaN etch and the final a-Si removal. The HfSiON film surface was also relatively smooth (R_{rms} = 1.82 Å) after the a-Si hard mask was removed, indicating that the a-Si hardmask removal step did not significantly increase surface roughness of the exposed high-*k*. Therefore, the HfSiON dielectric film processed through the representative

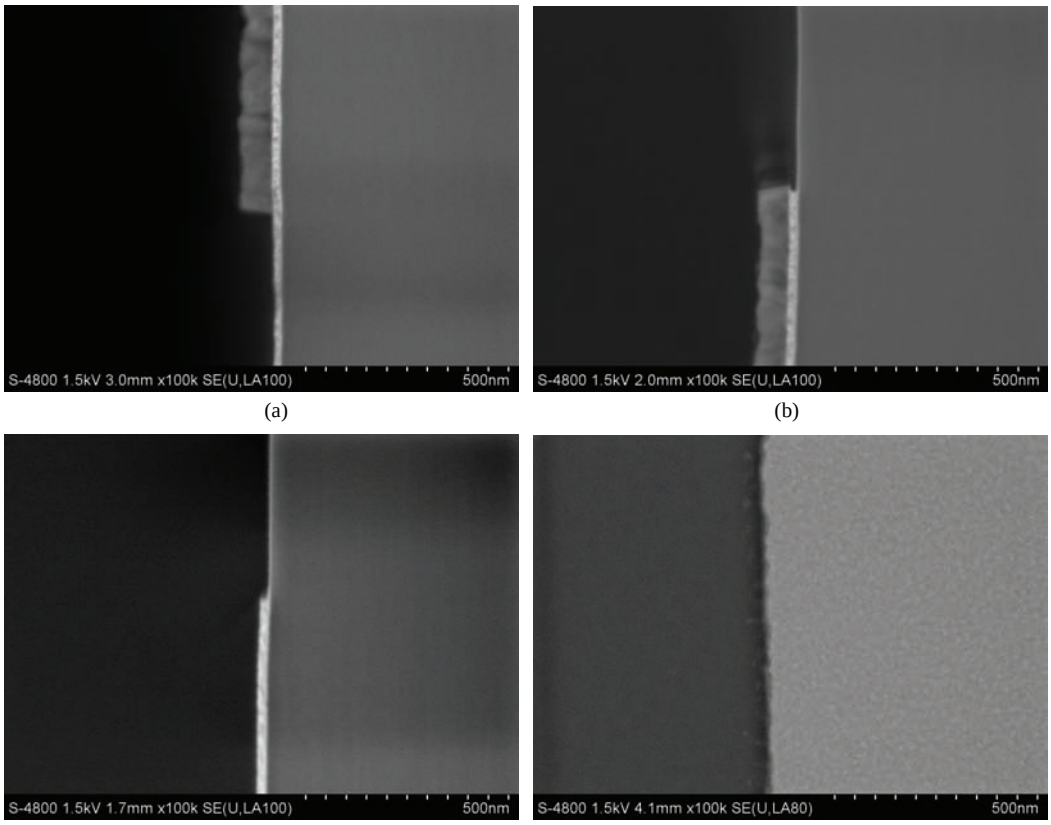

Fig. 1. SEM images of TaN selective removal on HfSiON with an a-Si hardmask process. (a) After dry etch of the a-Si hardmask. (b) After the TaN wet etch. (c) After the a-Si hardmask removal. (d) The surface of TaN and HfSiON after a-Si hardmask removal.

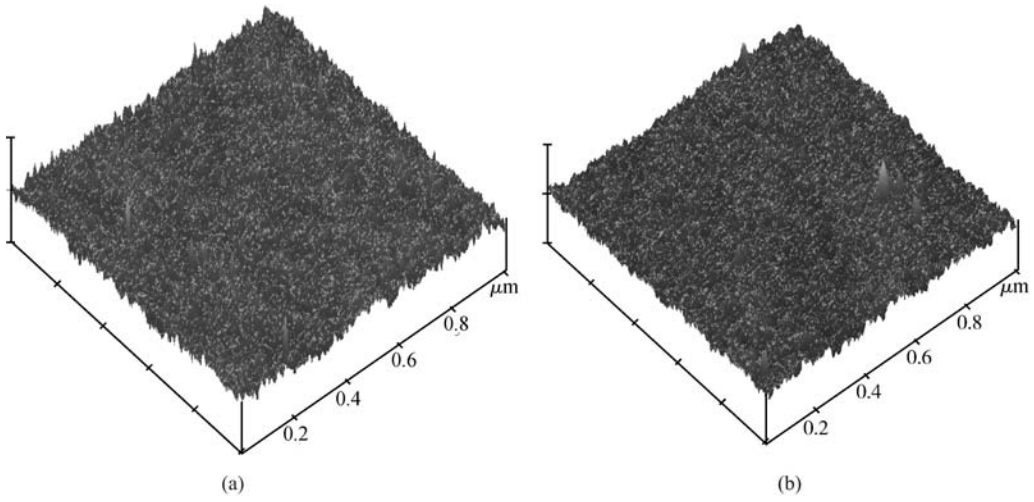

Fig. 2. AFM topography of the HfSiON surface. (a) After TaN wet etch. (b) After final a-Si hardmask removal.

TaN and a-Si hardmask removal processes still has a relatively smooth surface, which ensures excellent device performance.

4. Conclusion

The selective etch of the TaN on the HfSiON dielectric with an a-Si hardmask for dual metal gate integration has been presented. SC1 is an ideal etchant for the TaN metal gate selective etch and the a-Si hardmask removal is compatible with the HfSiON dielectric. More importantly, the HfSiON dielectric has a smooth surface after the wet etch of the TaN metal gate and the a-Si hardmask removal. Therefore, the scheme of selective etch TaN by SC1 with an a-Si hardmask provides a potential solution to realize high-k/dual metal gate CMOS device integration.

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