Dummy fill effect on CMP planarity*

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Abstract: With the use of a chemical-mechanical polishing (CMP) simulator verified by testing data from a foundry, the effect of dummy fill characteristics, such as fill size, fill density and fill shape, on CMP planarity is analyzed. The results indicate that dummy density has a significant impact on oxide erosion, and copper dishing is in proportion to dummy size. We also demonstrate that cross shape dummy fill can have the best dishing performance at the same density.

Key words: chemical mechanical polishing; dummy fill; dishing; erosion; planarity
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1. Introduction

Chemical-mechanical polishing (CMP) is a widely used technology to attain high levels of planarization[1]. It is influenced by geometric characteristics, such as line width and pattern density, as well as slurry chemistry, pad type, polishing pressure and rotational speed[2]. However, as the number of layers increases and line widths shrink, the process is not perfect in achieving planarization. The two common problems that often occur at different densities and metal widths are dishing and erosion, as shown in Fig. 1. Metal dishing is defined as the difference between the height of the oxide in the spaces and that of the metal in the trenches. Oxide erosion is defined as the difference between the oxide thickness before and after CMP[3]. These two phenomena have negative impacts on the performance of circuits, since variations in interlayer dielectric (ILD) thickness profile and interconnect height lead to variations in interconnect capacitance and resistance. This variation will increase the timing uncertainty of the circuit. Hence, it is crucial to minimize dishing and erosion[4].

In order to decrease interconnect thickness variations in metal and interlayer dielectric (ILD), dummy fill was introduced to low density regions[5]. Dummy fill is a non-functional feature that does not directly contribute to the logic implementation and can either be ground or left floating. However, the additional fill metal can increase wire capacitance and degrade interconnect performance[6, 7].

The capacitive impact and algorithm of dummy fill has been a subject of great interest over the last few years. Kurokawa[8] claims that the propagation delay can be increased by more than 20% by dummy fill. Stine[6] proposed rule-based filling methods and provided general guidelines based on the study of the impact of dummy fill on interconnect capacitance. Jia[9] proposed a performance aware dummy fill insertion algorithm which can reduce the delay of net by 15% on average compared with the traditional algorithm. There are also many papers focused on the modeling of CMP and the effects of pattern characteristics on copper CMP planarity. Several reports[10, 11] have been published characterizing dishing and erosion as functions of line width, pattern density, over-polish time, pad force and consumables. Nanz and Camilletti[12] provide an early review of these models. A more recent review is presented by Boning and Ouma[13]. Ruan[14] analyzed the copper CMP process and studied the influence of pattern characteristics on dishing, erosion and topography variation. However, there have been few reports dealing with the impacts of dummy fill characteristics on CMP planarization. Nowadays, dummy fill is inserted in the foundry during the process of manufacturing, which means that the effects of dummy fill on capacitance are not emphasized in the real design. Different dummy fill characteristics can have different influences on copper CMP thickness uniformity. In this work, several test structures were designed to analyze the effect of dummy fill characteristics, such as fill density, fill size and fill shape, on erosion and dishing.

2. Experiment

In this experiment, the impact of dummy fill characteristics on dishing and erosion was studied. The CMP simulation software used was developed by the EDA Center of Chinese Academy of Sciences. It was built on the density-step-height model and the contact mechanics model[14], and has been mod-

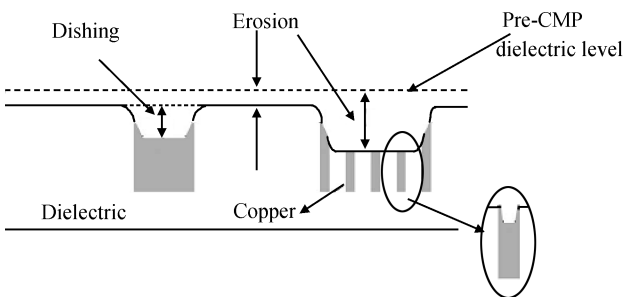

Fig. 1. Dishing and erosion[3].

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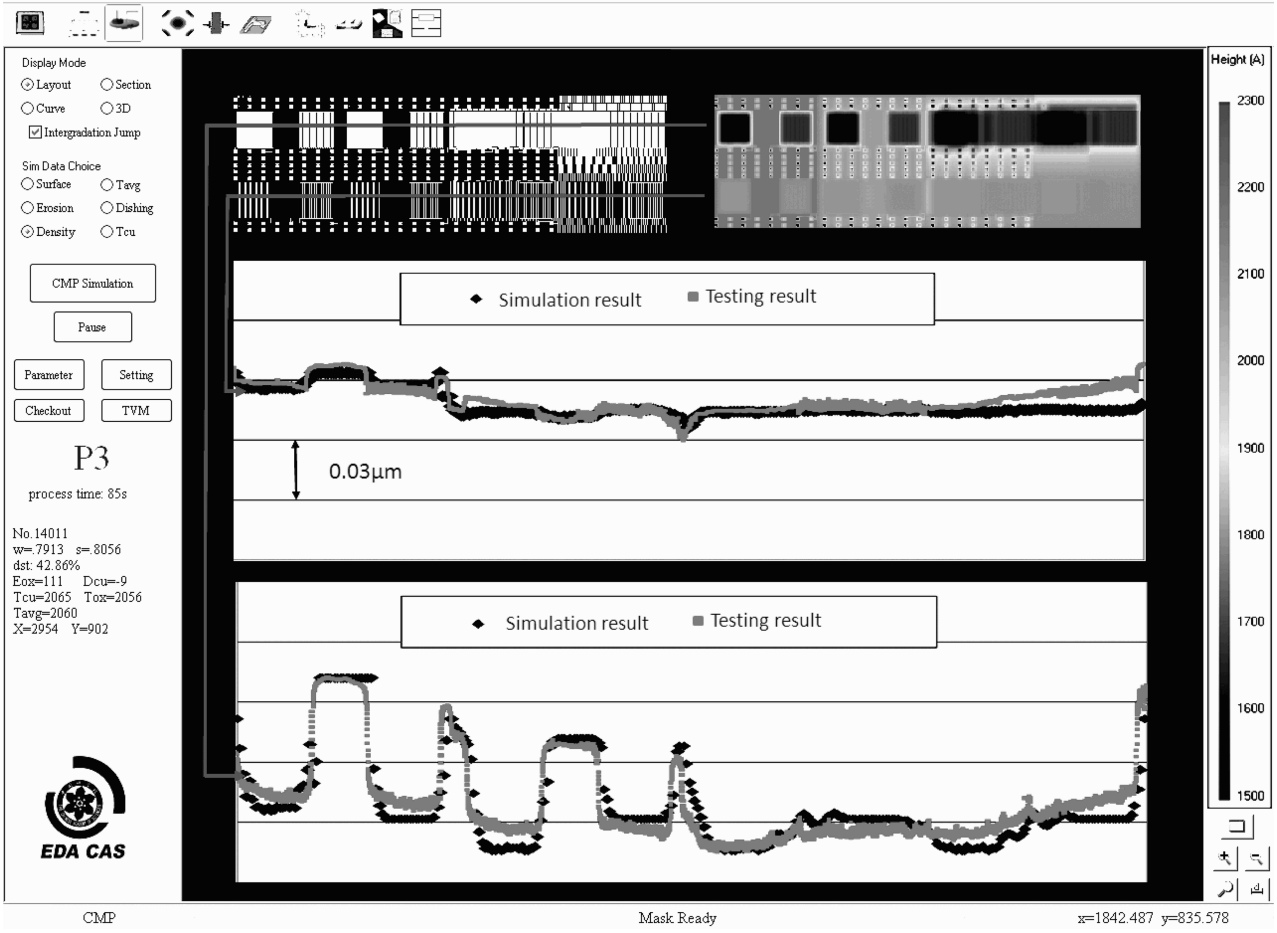

Fig. 2. CMP simulation results versus testing results.

ified and validated by several tape-out data in 65 nm technology under certain processes and equipment. The simulator, which has been adopted by an internationally famous foundry, will enable the user to input layout files and process information, and predict the surface topography during the process of manufacturing. Figure 2 shows the surface variation comparison between CMP simulation results and the testing results from the foundry with 65 nm process technology. The CMP polishing tool was an AMAT reflection. The atomic force microscope was used to measure surface dishing and erosion. As can be seen in the graph, the testing results show good agreement with those obtained by our CMP simulator.

Three groups of test structures used in this work are illustrated in Fig. 3. Every instance contains a parallel signal line with different dummy fills. The size of each instance is 300 × 300 μm^2, and the space is 100 μm to make sure that the result is not interfered with by neighboring ones.

The first group was inserted with square dummy fills, with a pattern density range from 20% to 60% and a fill size between 0.5 and 1 μm.

The second group was also inserted with square dummy fills, with a dummy size range from 1× line width to 5× line width under the constant pattern density of 50% and signal line widths between 1 and 3 μm.

The third group was inserted with different dummy shapes under the constant pattern density of 50% with the same dummy width: (a) cross, (b) square, (c) parallel line and (d) orthogonal dummy.

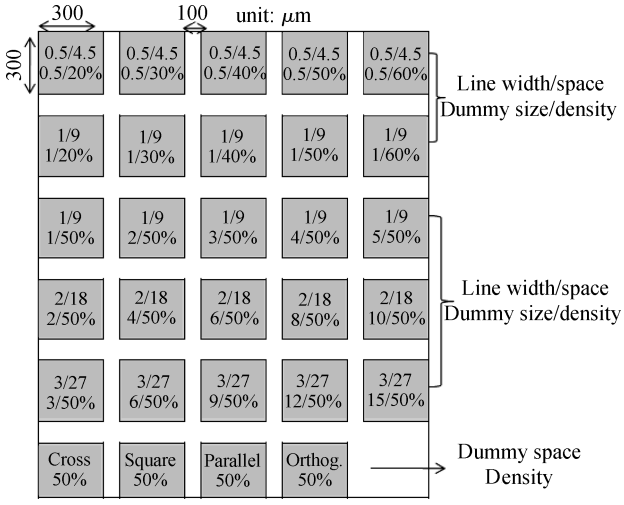

Fig. 3. Floor plan and layout of test pattern.

3. Results and discussion

We now present our analyses of the impact of dummy fill on CMP planarity.

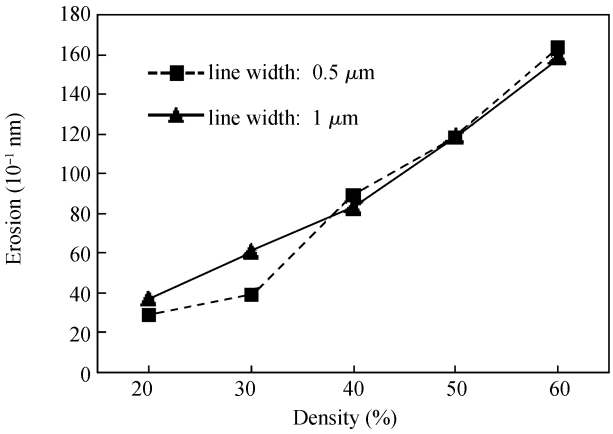

Fig. 4. Oxide erosion versus pattern density.

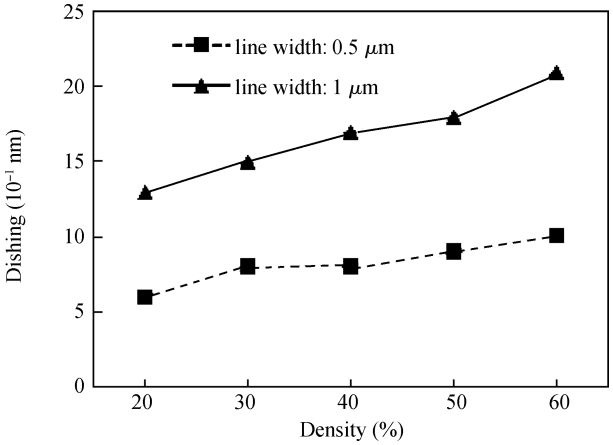

Fig. 5. Copper dishing versus pattern density.

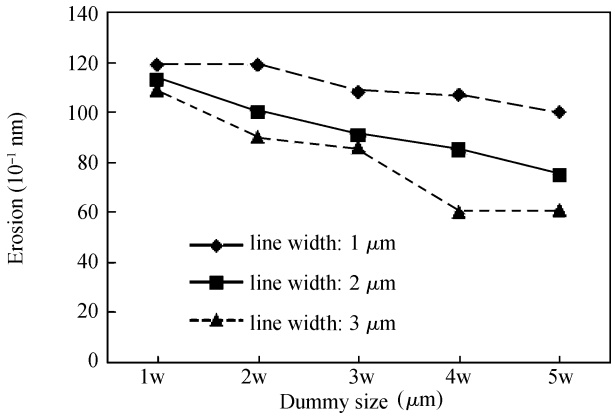

Fig. 6. Oxide erosion versus line width for 50% pattern density.

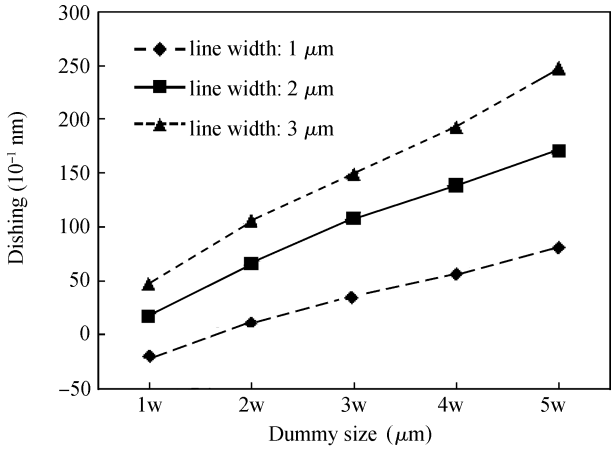

Fig. 7. Copper dishing versus line width for 50% pattern density.

3.1. Fill density

The erosions of oxide have been examined with various densities with line width between 0.5 and 1 μm. The densities are the major factors governing the effect of CMP planarity. In Fig. 4, erosion increases considerably as the density of pattern increases, regardless of the line width. This is because, for a given dummy size, as the dimension of the dielectric decreases with increasing pattern density, the pressure on the dielectric increases, which enhances the aggressiveness of the slurry towards the dielectric, and assists in mechanical abrasion. These combined effects account for the dramatic increase in erosion with increasing pattern density[15]. In our simulator, erosion in the blank area is defined as zero. As a result, it is the difference in erosion but not the erosion itself that reflects the situation of planarity. In order to decrease the erosion variation, the pattern density after dummy fill should be kept uniform within the chip. We can observe from Fig. 5 that copper dishing increases more slowly with the line width of 0.5 μm than that of 1 μm with increasing pattern density.

3.2. Fill size and line width

For a given line width and pattern density, increasing dummy size has a more dramatic effect on metal dishing than oxide erosion. Figures 6 and 7 show the effect of dummy size on oxide erosion and metal dishing. Erosion decreases slightly with an increase in dummy size when the line width is 1 μm, but markedly when the line width is 2 or 3 μm. The reason is that for a given pattern density, decreasing dummy fill size reflects decreasing dimension of the dielectric separating lines, which are more easily removed during the process of polishing. As dummy size increases, copper dishing increases dramatically, regardless of line width. This phenomenon can be explained as follows. Because the pad surface is distorted during the CMP process, as line width increases, the pad asperity easily touches the copper in the trench and scoops out soft copper between the harder dielectric.

3.3. Fill shape

Figure 9 presents the oxide dishing for different dummy shapes, which are shown in Fig. 8. Their pattern density and dummy width are the same. The area of cross shape is 55% of the square fill. However, copper dishing of the cross shape is minus, which can be taken as zero. The result indicates that a cross dummy fill can have a better effect on metal dishing, compared to the other three dummy fill shapes. The orthogonal dummy structure has the worst impact on copper dishing. The best performance of the cross dummy fill can be explained in two ways. One reason is because the smaller area of the cross dummy brings a smaller area of trench, which makes the pad surface less distorted and causes less copper loss during the

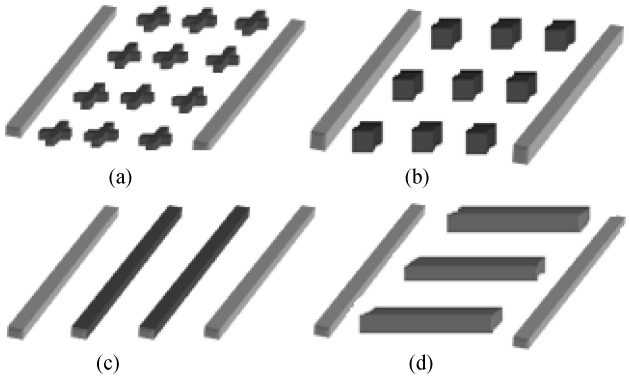

Fig. 8. Possible dummy shapes. (a) Cross. (b) Square. (c) Parallel line. (d) Orthogonal.

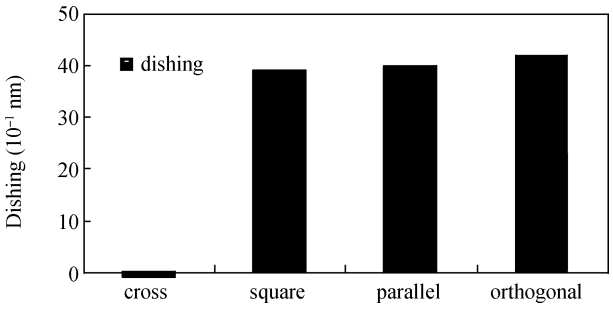

Fig. 9. Copper dishing with different dummy shapes.

polishing process. The other reason is because it can achieve more uniform distribution compared to the other three shapes at the same density, which makes the wafer endure mechanical force more evenly. Therefore, in order to reduce dishing in real design, the cross shape dummy fill is preferred over the other three shapes.

4. Conclusions and future work

In this paper, we analyze the effect of dummy fill characteristics, such as fill density, fill size, and fill shape, on copper CMP. A CMP simulator and three test structures were introduced to test the influence of dummy fill characteristics on dishing and erosion. Our study shows that fill density is an important factor for erosion, while dishing increases with the increasing dummy fill size. Compared with other dummy shapes, a cross dummy fill has a better dishing performance because of its smaller area.

In future work, we will study the effect of dummy fill characteristics on both planarization and interconnect capacitance. Then we can propose a more comprehensive dummy fill guideline to achieve better uniformity and less impact on interconnect capacitance.

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