A novel 2.2 Gbps LVDS driver circuit design based on 0.35 μm CMOS

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Abstract: This paper presents a novel high-speed low voltage differential signaling (LVDS) driver design for point-to-point communication. The switching noise of the driver was greatly suppressed by adding a charge/discharge circuit and the operating frequency of the circuit was also increased. A simple and effective common-mode feedback circuit was added to stabilize the output common-mode voltage. The proposed driver was implemented in a standard 0.35 μm CMOS process with a die area of 0.15 mm^2. The test result shows that the proposed driver works well at 2.2 Gbps with power consumption of only 23 mW and 21.35 ps peak-to-peak jitter under a 1.8 V power supply.

Key words: high-speed; LVDS; charge injection; common-mode feedback
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1. Introduction

In point-to-point communication, low voltage differential signaling (LVDS)[1, 2] can greatly increase data rates with decreased power consumption compared to other means of transmission. The traditional LVDS driver usually consists of two PMOS and two NMOS switches. In order to reduce input loading, the PMOS switches were replaced by NMOS switches[3–6]. As the power supply keeps falling, the limitation of overdrive voltage with certain noise margin becomes an issue, so the driver with a single current source has been brought up[7, 8]. In Fig. 1, the topology of Ref. [7], a pull-down capacitor is added to reduce the switch-off voltage for the PMOS, which reduces the transition time and brings a small amount of switching noise to the output. But the driver in Fig. 1 cannot operate so well at high frequency due to the extra charges from switches S1/S2 and the gate of P1/P2.

This paper analyzes the theory and functionality of the additional charge/discharge circuit and introduces the proposed common-mode feedback structure. Experimental results of the prototype LVDS driver are given.

2. Charge/discharge circuit

The operation theory of the driver in Fig. 1 is that if D1 goes low, N3 shuts down, and D1b goes high to have N4 conduct current. The voltage at D2b now is pulled up by C_o to V_C to shut down P2. At this moment switch S2 opens and S1 closes. P1 connects to V_{b2} to be correctly biased. Before and after D1/D1b changes its state, as the capacitance of C_o is much higher than the parasitic capacitance of S1, 2, so half of the charge injection of S1, 2 can hardly affect the voltage at the gate of P1/P2. The other half of the charge is discharged through the buffer. But when the driver operates at a very high frequency (above 1 GHz), assume P2 turns to conduct, so S2 closes to bias P2 by V_{b2}. However, in the previous state when P2 opens, the voltage at its gate V_C is higher than V_{b2}, which means some extra charge has to be discharged through the buffer quickly enough not to affect the bias of P2. But due to the limited settling behavior of the buffer, it will take a certain period to discharge completely, so V_{b2} will vary. In order to solve this problem, in this work a charge/discharge circuit between the buffer and switches S1, 2 has been added so that when S1, 2 opens or closes, there is a capacitor with no initial charge connects to these switches to pull down the voltage at the gate of P1/P2, then the LVDS output can be more smooth and stable, and the switching noise is greatly minimized.

As discussed above, in order to absorb these charges, a charge/discharge circuit is added in Fig. 2. This additional circuit consists of current comparison, control logic and a pair of switchable capacitors.

In Fig. 2, if V_{b2} varies by charge injection, the currents of the first stage of the buffer will be sampled and the current difference $I_1 - I_2 = \Delta I$ will be sent to the current comparison circuit, whose output will be captured by the sensitive latch to produce a pulse to trigger the following circuit. The following circuit converts the pulse to a complementary controlling clock signal Φ_3 and Φ_{3b} in Fig. 3, which will alternately charge or discharge C_1 and C_2. For example, at phase Φ_{3b}, C_1 connects to ground to discharge, C_2 connects to V_{b2} to be charged by the extra charges from the charge in the channel of S1 or S2 and from the gate of P1 or P2, so that during each phase (Φ_3

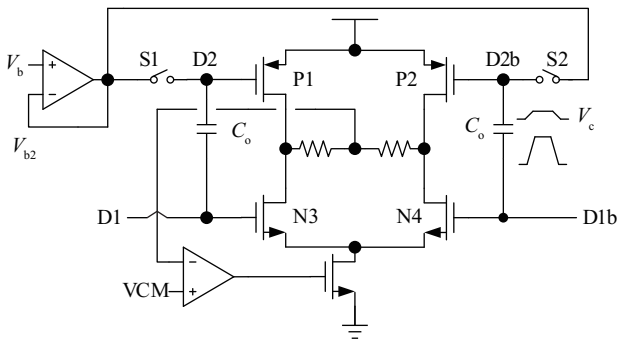

Fig. 1. Single current source LVDS driver.

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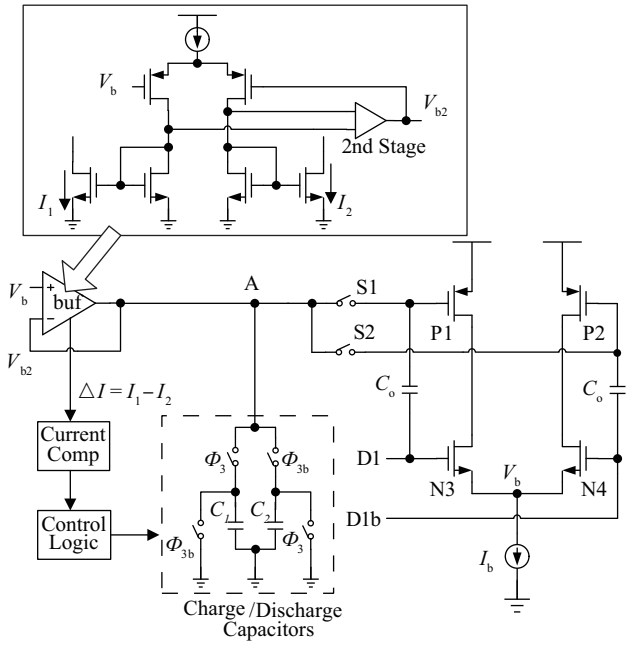

Fig. 2. Modified LVDS driver upon Fig. 3 (CMFB not shown).

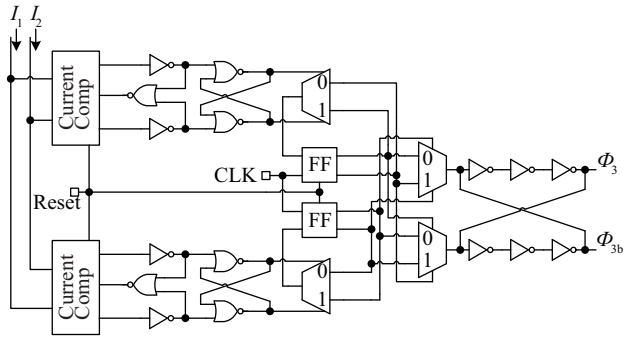

Fig. 3. Control logic of charge/discharge capacitors.

and Φ_{3b}) there is always a capacitor (C_1 or C_2) with no initial charge sharing these extra charge at this node. At very high frequency (above 1 GHz) it can be assumed that the turn-on and turn-off time of the MOS switch approaches zero, so the extra charges from driver switch S1 or S2 can be written as

$$Q_i = C_{ov}(V_{g,on} - V_{g,off}) + \frac{1}{2}C_{ox}(V_{g,on} - V_o - V_{th}) = C_{ov}V_{CC} + \frac{1}{2}C_{ox}(V_{CC} - V_{off} - V_{th}). \quad (1)$$

And the charge from the gate of P1 or P2 is

$$Q_g = (V_C - V_{b2})C_{OXP}. \quad (2)$$

C_{ov} is the overlap capacitance between the gate and drain of the MOS transistor, and C_{ox} is the gate oxide capacitance of the switch. C_{oxp} is the gate oxide capacitance of P1 or P2. When the MOS turns off, Q_g and half of the channel charge will inject to node A in Fig. 2, which can be seen in Fig. 4.

After the charge redistributes with C_1/C_2, the total charge is

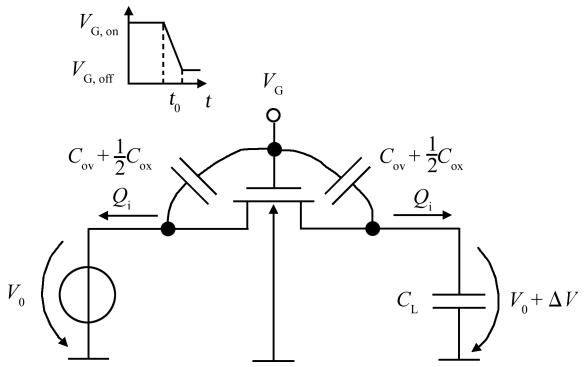

Fig. 4. Charge injection model of a MOS transistor.

$$Q_f = \Delta V_C \left(C_{1,2} + \frac{1}{2}C_{ox} + C_{ov} + C_{OXP} + C_{out} \right). \quad (3)$$

C_{out} is the output equivalent capacitance of the buffer. During these switching states, the total charge will remain the same, $Q_g + Q_i = Q_f$, so

$$\Delta V_C = [2C_{ov}V_{CC} + C_{ox}(V_{CC} - V_{off} - V_{th})] \times \left(C_{1,2} + \frac{1}{2}C_{ox} + C_{ov} + C_{OXP} + C_{out} \right)^{-1}. \quad (4)$$

ΔV_C is the amount of change on V_{b2} due to extra charge injection. In Fig. 2, if Φ_3 goes high, C_1 with no initial charge starts to share the extra charge with all equivalent capacitance at node A, so at this moment the voltage at A will be pulled down by ΔV_e, and C_1 will be charged for a short period. When Φ_{3b} goes high, C_1 will discharge to ground, and at the same time C_2 will start to share the charge and be charged by ΔV_c, as shown in Fig. 5. If Φ_3 and Φ_{3b} do not change state, $C_{1,2}$ will keep being charged from point "K" to "U" (during T_1). If Φ_3 and Φ_{3b} change state frequently, $C_{1,2}$ will alternately absorb the charge that V_{b2} gradually goes down from point "U" to "G" (during T_2). ΔV_e is larger than ΔV_c because whatever the kind of $C_{1,2}$, there is still a parasitic serial resistance which will have an ac voltage drop when $C_{1,2}$ starts to share the charge. In addition, the reference bias V_b will have a little change from time to time caused by the coupling from inside parasitic capacitances of the buffer, which can be neglected for their small variation (within 2 mV).

So if an appropriate value is chosen for $C_{1,2}$ and a right period for the control pulse, then according to the above theory, when Φ_{3b} (or Φ_3) changes its state frequently (T_2), $C_{1,2}$ starts to share the charge alternately, so V_{b2} will decrease by ΔV_e. When Φ_3 (or Φ_{3b}) stays high (T_1), C_1 or C_2 will keep being charged and V_{b2} will increase by ΔV_c. As a result, the bias voltage V_{b2} can be dynamically stabilized. Here, $C_{1,2}$ is 500 fF, and in Fig. 3 the frequency of "CLK" equals the data rate so that when S1 or S2 opens, C_1 or C_2 will be connected to node A accordingly to adjust V_{b2} in time. The period (T_1 and T_2 in Fig. 5) that Φ_3 (or Φ_{3b}) keeps changing its state or staying still depends on the sensitivity of the current comp and delay of the control logic, as shown in Fig. 3, so in order to respond quickly, a high-speed latch is used for current comparison.

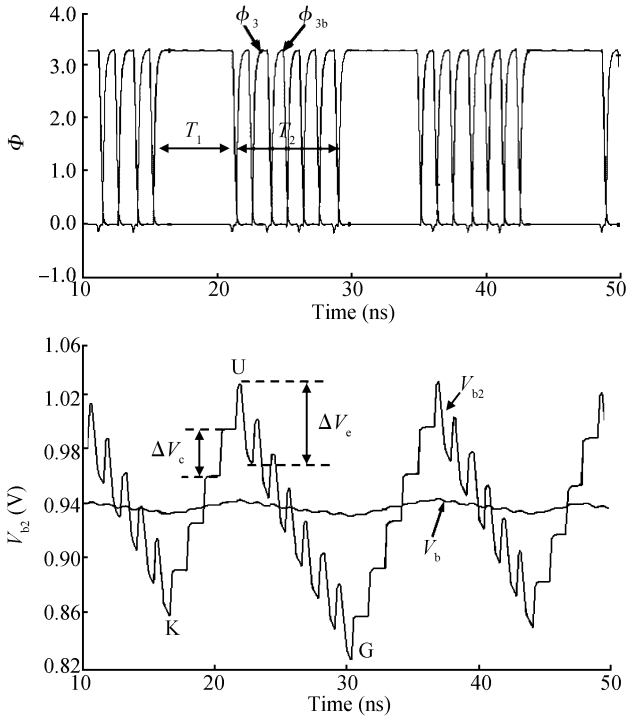

Fig. 5. V_{b2} changed as node A charge/discharge.

There are two factors that affect the sensitivity and performance of the charge/discharge circuit. One is the propagation delay of this control loop, which is determined by the number and size of the digital gates, and the size is determined by the driving requirement. The less the delay, the faster this control loop is able to operate. In this design, the current comparison circuit, the inverter chain, the 2-to-1 MUX and the RS flip-flops bring 0.9 ns, 0.2 ns, 0.2 ns and 0.3 ns delay, respectively, and due to the decision hysteresis the feedback decision circuit contributes 2.4 ns delay. So the total delay of the control loop is 4 ns. The other factor is the offset of the buffer and current comparison latch. The offset of the buffer is quite large as a result of using a MOS transistor as the input rather than a bipolar one. In this design the offset is 10 mV in the worst case. To save power and increase comparison speed, no pre-amp is used in this current comparison latch, so the latch will bring an equivalent 20 mV offset.

3. Common-mode feedback (CMFB)

The traditional way of stabilizing the LVDS output common-mode signal is to use a high-frequency op-amp to build up an internal CMFB circuit, where it is very hard to ideally fix the output common-mode signal. It is also hard to ensure stability of the CMFB loop due to the large size of the LVDS driver switches. So the op-amp should not only have high gain but high bandwidth. In this work, an extra NMOS transistor as an internal CMFB structure was introduced to the driver, as shown in Fig. 6. The additional part only contains an auxiliary Nx transistor. It can easily be found that $I_{bias} = I_{b2} + I_{Nx}$, when V_{CM} happens to go up, the current flowing through Nx increases, then V_{CM} is pulled down. Because no op-amp was used here, the loop gain was low, so in real applications the sizes of Nx should be much larger than Ns

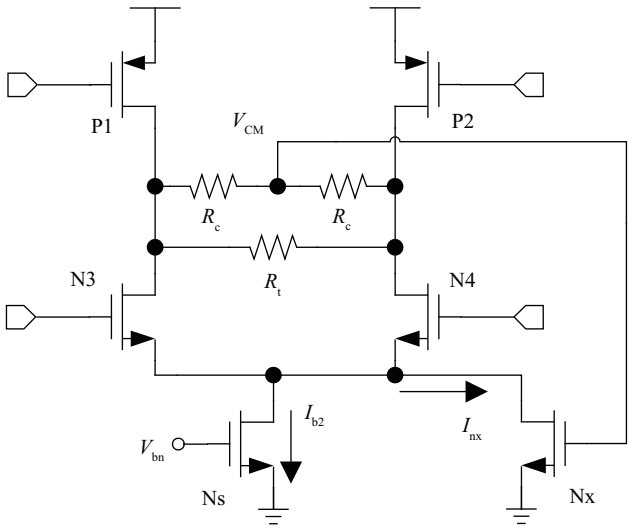

Fig. 6. LVDS driver with a simple CMFB.

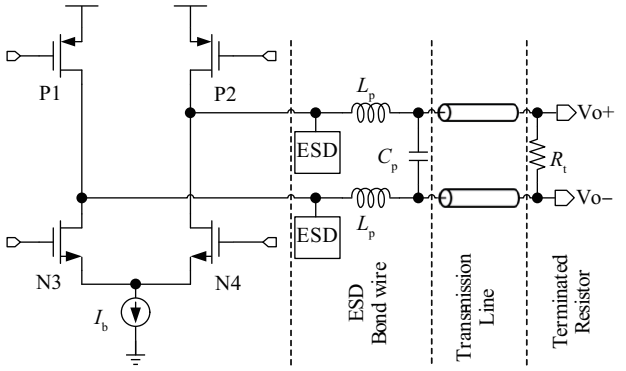

Fig. 7. Simulation circuit of LVDS driver.

to be capable of responding to the current change. In this paper, $L_{Nx} = L_{Ns}$ is chosen for matching purpose and $W_{Nx} = 9W_{Ns}$.

4. Simulation and measurement results

To simulate the circuit according to the real application, the relevant ESD, package, bond wire, transmission line and terminated resistor models have been added, as shown in Fig. 7. The effective inductance brought by the package and bond wire is L_p = 2 nH, C_p = 300 fF. Here the transmission line is the standard twisted pair with characteristic resistance of 50 Ω and distributed capacitance of 15 pF, and the terminated resistor R_t = 100 Ω. The data rate is 2.2 Gbps under a power supply of 1.8 V.

In Fig. 8(a), when the charge/discharge circuit is disabled, at the moment P1/P2 starts to switch on, its gate voltage cannot quickly transit from V_C to V_{b2} due to the limited settling behavior of the buffer, as the gate-source voltage of P1/P2 is proportional to the square root of the drain current. As a result, the peak current through the output terminal resistor produces about 80 mV switching peak at the LVDS output (wave A). When the charge/discharge circuit is enabled, according to the theory shown above, the charge/discharge capacitor quickly pulls down the gate voltage of P1/P2 to V_{b2}. If the gate voltage of P1/P2 is lower than V_{b2}, the control loop will pull it up to

Table 1. LVDS driver performance comparison.

Parameter	Ref. [4]	Ref. [7]	Ref. [9]	This paper
Process	0.35 μm CMOS	0.35 μm CMOS	0.35 μm BiCMOS	0.35 μm CMOS
Output voltage swing (mV)	412	340	300	306
Maximum data rate (Gbps)	1.2	1.2	2	2.2
Die size (mm^2)	0.17	0.14	—	0.15
Power supply (V)	3.3	1.8	1.8	1.8
Power consumption (mW)	43	12.8	10.8	23

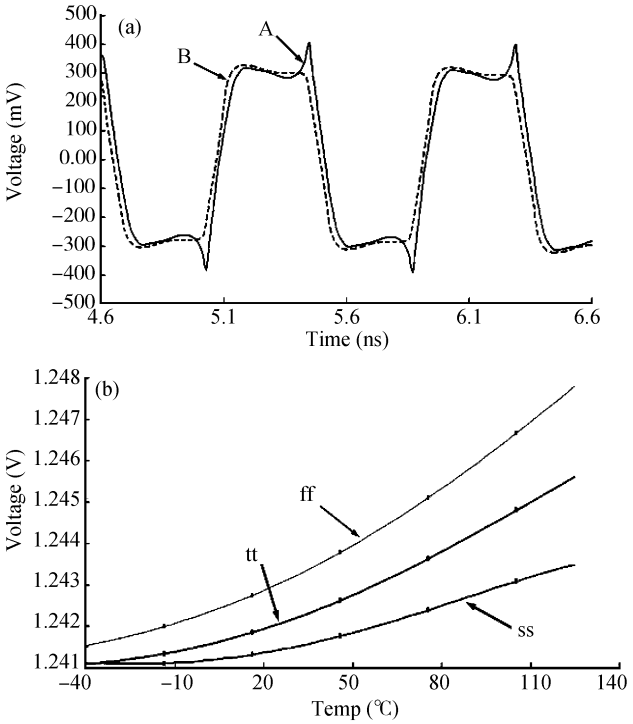

Fig. 8. Simulated output differential and common-mode signal of proposed LVDS driver. (a) Output differential voltage. (b) Output common-mode voltage.

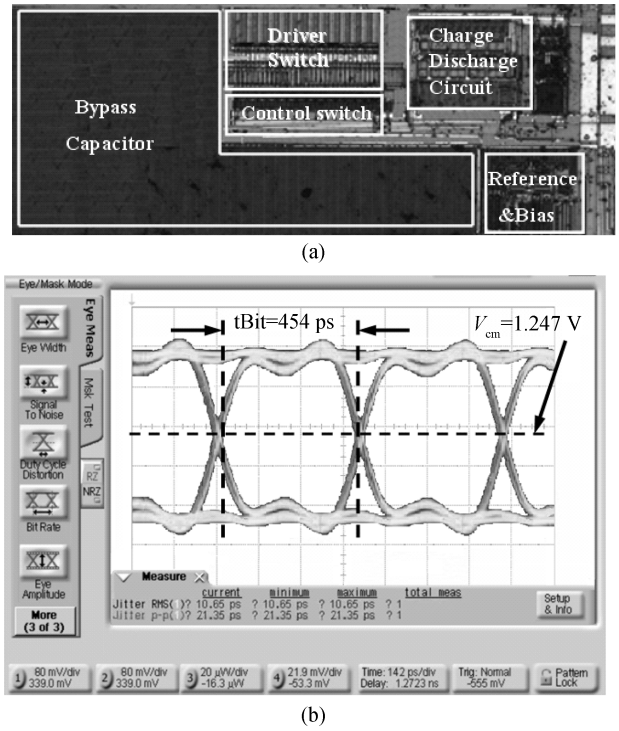

Fig. 9. (a) Chip photograph and (b) measured result.

make the bias point dynamically stable. The output is indicated by wave B that the signal peak is almost removed. Obviously, the proposed CMFB works well from –40 to 125 ℃. The maximum output common-mode voltage deviation is only 6 mV, which can be seen in Fig. 8(b).

This driver is implemented in a standard 0.35 μm CMOS process, with a power supply of 1.8 V. The overall die size is 0.15 mm^2 in the TSOP-28 package. The chip photograph is shown in Fig. 9. It can be seen that the additional charge/discharge circuit only occupies 0.02 mm^2. The measurement shows that this driver can work well at a data rate of 2.2 Gbps with 306 mV differential swing and, thanks to the charge/discharge circuit, the total output noise decreases a lot so that the measured peak-to-peak jitter is 21.35 ps. The driver consumes only 23 mW power in total at this high data rate.

5. Conclusion

In this paper, a novel high-speed LVDS driver design for point-to-point communication has been discussed. By adding an additional charge/discharge circuit and an internal simplified CMFB, the performance of the driver increases significantly. The final chip implemented in a low cost 0.35 μm CMOS process and the measured result proves that the data rate up to 2.2 Gbps application can be guaranteed with only 23 mW power consumption and 21.35 ps peak-to-peak jitter under a 1.8 V power supply. It can be easily found from Fig. 11 that the output differential and common-mode signal are within the standard[1]. Table 1 also shows that the proposed driver has better performance than the counterparts reported previously.

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