Design and optimization of an ultra-wide frequency range CMOS divide-by-two circuit*

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Abstract: A novel toggled flip-flop (TFF) divide-by-two circuit (DTC) and its optimization method based on a large-signal analysis approach are proposed. By reducing the output RC constant in tracking mode and making it large in latching mode, compressing the internal signal swing as well as compensating the current leaked in the latching mode, the operating frequency range is greatly expanded. Implemented in a SMIC 0.13 μm RF CMOS process with a 1.2 V power supply, it can work under an ultra-wide frequency band ranging from 320 MHz to 29.6 GHz. Experimental results show that two phase-locked loops (PLLs) with the proposed DTC can achieve in-band phase noise of –94 dBc/Hz @ 10 kHz under 4224 MHz operating frequency and –84 dBc/Hz @ 10 kHz under 10 GHz operating frequency, respectively. The power consumption of the proposed DTC is reduced by almost 50% compared with the conventional counterparts.

Key words: TFF; DTC; PLL; ultra-wide frequency range; optimization method; in-band phase noise
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1. Introduction

A DTC, as the foremost building block in a frequency divider, is an important module in a PLL-based frequency synthesizer which decides the maximum operating frequency and has an important effect on the in-band noise performance. There are mainly two categories of architectures for CMOS DTCs in the published literature: source-coupled logic based toggled flip-flop DTC architecture (TFF-DTC)[1] and true single phase circuit architecture (TSPC-DTC)[2]. Their differences are listed in Table 1.

The former has attracted much more research attention, both in the past and in recent years, due to the fact that it can work at such high frequencies, ranging from several GHz to some decades of GHz, that otherwise cannot be achieved by other types of DTC. Therefore, it makes feasible a wide band programmable divider, be it integral or fractional, with small steps to accurately choose different channels. Also, it outputs a quadrature phase signal from a differential input clock, which is compatible with the output of conventional voltage controlled oscillators (VCOs). The latter gradually becomes a competent alternative when low power consumption is involved as a critical requirement. Also, its rectangular-wave output property is desired as the last block of divider for conventional PLL architecture.

However, this paper only puts the research focus on the TFF-DTC, and an ultra-wide frequency range CMOS TFF-DTC circuit and its optimization method are proposed. We also introduce the design considerations where several circuit techniques are investigated and three design trends are summarized, detail the proposed DTC topology and its optimization method, discuss the application case where a practical DTC is designed and used in two different integer PLLs, and give the simulation results of the DTC and experimental results of the in-band noise performance for both PLLs.

2. Design considerations

2.1. TFF-DTC fundamental

As the most obvious characteristic of a TFF-DTC, two high-speed D-type latches are connected as a master-slave pattern in a negative feedback with a regenerative gate-coupled circuit in each D latch, which works only at half of the clock cycle alternately. Given an input clock CK with differential phases, the TFF-DTC can generate two output signals, namely in-phase OI and quadrature OQ, or I/Q respectively, whose frequencies are half of the input frequency. The block diagram and timing scheme are shown in Fig. 1.

In the tracking mode when CK is high, the master D latch amplifies the input signal, which is held by the slave D latch, and the signal path from master to slave is cut off. While in the latching mode when CK is low, the master D latch holds the amplified signal and transfers it to and is amplified by the slave D latch, at this time, the signal path from slave to master is cut off. Through the so called "master-slave TFF" operating principle as simply described above, the divide-by-two function can be achieved.

2.2. Previous wisdom

A variety of circuit techniques have been introduced in the public literature to improve the performance of DTCs for specific applications, which can be sorted into the following three aspects.

2.2.1. Fast speed technique

A key problem limiting the speed of the conventional TFF-DTC is the dilemma of load resistance[3]. Most of the previous TFF-DTCs use constant load, be it a single resistor[4] or an active load[5]. However, the requirements for the load resistance

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Table 1. Comparison of TFF-DTC and TSPC-DTC.

Architecture	Operating frequency range		IO pattern		Power
	Lower limited (MHz)	Upper limited (GHz)	I	O	
TFF-DTC	< 500	> 15	Diff. Sine.	Quad. Diff.	Large
TSPC-DTC	< 50	> 4	Single. Rec.	Single	Small

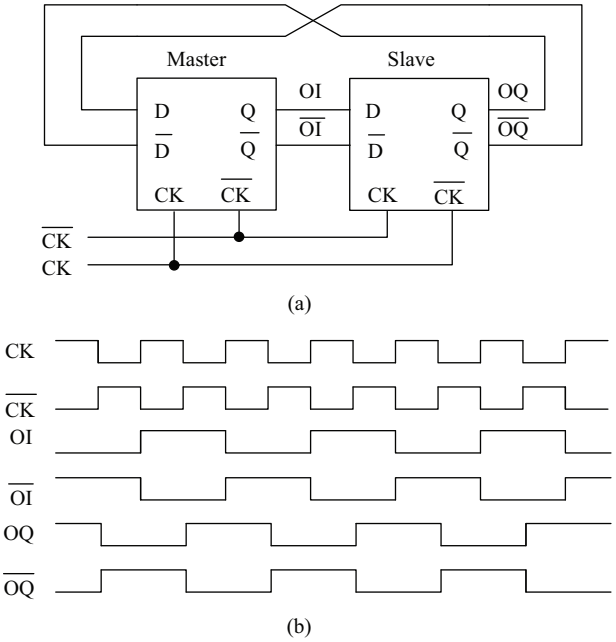

Fig. 1. Principle of the TFF-DTC. (a) Block diagram. (b) Timing scheme.

in the two operating modes are quite different. On one hand, the load resistance is required to be small to guarantee fast tracking of the input signal in the tracking mode, while, on the other hand, it needs to be large to make sure the signal is held in the latching mode. This is one of the motivations to implement the so called "dynamic load" [1, 3, 6].

2.2.2. Low supply voltage technique

Most of the previous TFF-DTCs exhibit a significant loss in performance and even fail to function as the supply voltage drops below 1 V. This is mainly due to the fact that the biasing voltage occupies a large portion of the output swing. Reference[7] improved the tail current topology in the current-steering SCL, replacing the common-source topology of the tail current by a common-gate topology. With this circuit technique, the voltage headroom is increased by a considerable quantity.

2.2.3. Low power technique

In order to reduce the power consumption, a common source tail transistor is often used to limit the maximum current in the tracking mode[3]. In addition, the static current is eliminated whenever the circuit is inactive[6].

Besides the circuit techniques mentioned above, some layout techniques have emerged to improve the performance of the TFF-DTC, i.e. the ring-shaped transistor layout proposed in Ref. [1].

However, the conventional TFF-DTC has two problems, as follows.

Firstly, in the application of a wide band communication system, the reference frequency is generally designed as low as tens of MHz for the convenience of channel selection. However, such low frequency can hardly be achieved by the TFF-DTC, which explains why most existing dividers use the hybrid architecture.

Secondly, the power of the TFF-DTC increases dramatically when the operating frequency rises.

3. Proposed architecture and optimization method

3.1. DTC architecture

To overcome the problems mentioned above, a novel ultra-wide frequency range CMOS DTC and its optimization method are proposed. The topology of the proposed DTC is shown in Fig. 2[8].

This consists of two identical D-type latches, each of which is made up of the following transistors: M7 and M8 constitute the logic part, which functions only at tracking mode; M5 and M6 constitute the regeneration part, which functions only at latching mode; M2 and M3 are the conventional dynamic load; and M9 is used as the biasing for M7 and M8. Unlike the conventional TFF-DTC, three clock controlled extra transistors are added. As the frequency falls, the charge residing in the output node gradually leaks off and cannot be refreshed in time. This phenomenon causes the output voltage to drop and eventually make the DTC out of work. The introduction of M1 and M4 greatly alleviates this problem since they sink extra current to compensate the charge loss. M10 is used to turn off the regeneration part in tracking mode for power saving. According to Ref. [9], the proposed DTC also has a superior noise performance due to the absence of the extra tail transistor, as adopted as current mode logic in Ref. [4].

In the practical design, some principles should be followed. In this paper, we take the dynamic RC constant into consideration rather than the single load resistance, as described previously[3]. Therefore, the parasitic capacitive load is also involved, as we will see in the next section. Generally, a small output RC constant in tracking mode and a large one in latching mode are highly desirable. Besides the dynamic RC constant, the internal signal property also has a significant effect on the overall DTC performance. As explained later, compressing the internal signal swing is beneficial to the high frequency performance of the DTC. With these principles, the operating frequency range is greatly expanded. A typical design, shown in Section 4, has reached a maximum-to-minimum-frequency-ratio (MMFR) almost as high as 100.

3.2. Optimization method

Since all of the transistors in the proposed TFF-DTC are working under a large clock signal, it is not suitable to analyze

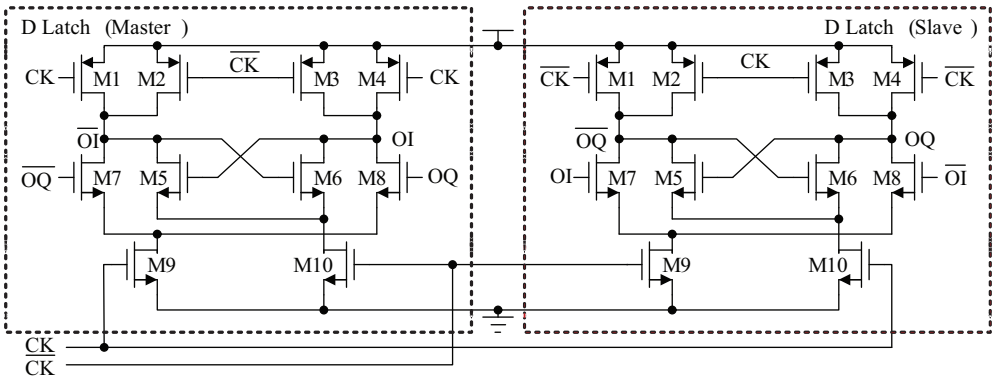

Fig. 2. Topology of the proposed DTC.

the circuit by a small-signal approach, as used in Ref. [7]. Reference [10] offered many beneficial guidelines for such analysis. In this section, an optimization method, based on a large-signal approach, is presented, which lends itself to a qualitative perspective to the design of each transistor from various tradeoffs.

(1) M7 and M8. Two design aspects ensure the fast tracking of the input signal: one is a small RC constant and the other is enough gain of the amplifier comprising M7 and M8, plus M2 and M3. Actually, only one of M7 and M8 is active. We assume that M7 is active, thus M3 pulls OI up to $V_{\rm DD}$, and M2 works in the linear region with its on-resistance as

$$R_{\rm on,\,23} = \frac{1}{\mu_{\rm p} C_{\rm OX} S_{23} (V_{\rm DD} - |V_{\rm THp}|)}, \tag{1}$$

where S_{23} is the aspect ratio of M2 and M3. The positive peak level $V_{\rm p+}$ is $V_{\rm DD}$ and the negative one $V_{\rm p-}$ can be obtained as

$$V_{\rm p-} = V_{\rm DD} - I_{\rm D,\,9} R_{\rm on,\,23}, \tag{2}$$

where $I_{\rm D,\,9}$ is the drain–source current of M9. From Eqs. (1) and (2), S_{23} trades off with $V_{\rm p-}$, so the larger S_{23} is, the higher the resulting $V_{\rm p-}$.

(2) M2 and M3. According to the large-signal principle, a signal with amplitude $V_{\rm p}$ and frequency f_0 can only be amplified as long as its slew rate (SR) satisfies

$$\mathrm{SR} \geqslant V_{\rm p} 2\pi f_0. \tag{3}$$

Assume the load capacitance is $C_{\rm L}$. Thus we have

$$\frac{I_{\rm D,\,9}}{C_{\rm L}} \geqslant \frac{1}{2} I_{\rm D,\,9} R_{\rm on,\,23} 2\pi f_0 \tag{4}$$

or

$$R_{\rm on,\,23} \leqslant \frac{1}{2\pi f_0 C_{\rm L}}. \tag{5}$$

(3) M9. Low $V_{\rm p-}$ drives M9 into the linear region, resulting in a smaller drain–source current and further decreasing the transconductances of M7 and M8, thus extra power is burned to maintain the same performance. Obviously, a tradeoff exists between $V_{\rm p-}$ and the power: the higher $V_{\rm p-}$ is, the lower the power that can be achieved. (4) M1, M4, M5 and M6. These four transistors constitute the well-known cross-coupled native

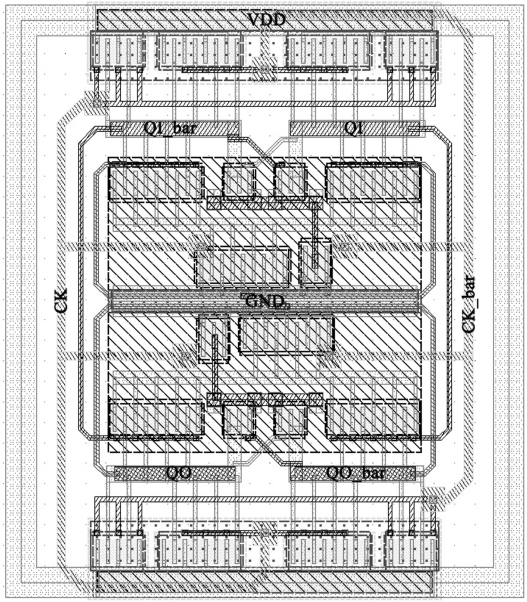

Fig. 3. Layout of the proposed DTC.

feedback loop which is widely used for signal regeneration purpose. The precondition below must be satisfied for such a circuit,

$$g_{\rm m,\,56} R_{\rm on,\,14} > 1. \tag{6}$$

Also, as mentioned previously, the selection of these transistors should make the output RC constant large enough, taking into account the parasitic capacitances involved. In addition, M1 and M4 sink some current to the output node, compensating the leakage current loss in the low frequency working condition. This arrangement extends the lower frequency limit significantly.

(5) M10. This transistor functions as the biasing for M5 and M6 when they are active, whereas it cuts off the current path when they are inactive. Also, $V_{\rm p-}$ can be tuned by changing the size of M10. S_{10}, $V_{\rm p-}$ lowers as S_{10} increases, which brings along another benefit that the maximum frequency limit is extended. (3) The qualitative relationship of the transistor sizes is recommended to be $S_9 > S_{78} > S_{23} > S_{14} > S_{10} > S_{56}$.

From the analyses above, the following design conclusions can be addressed:

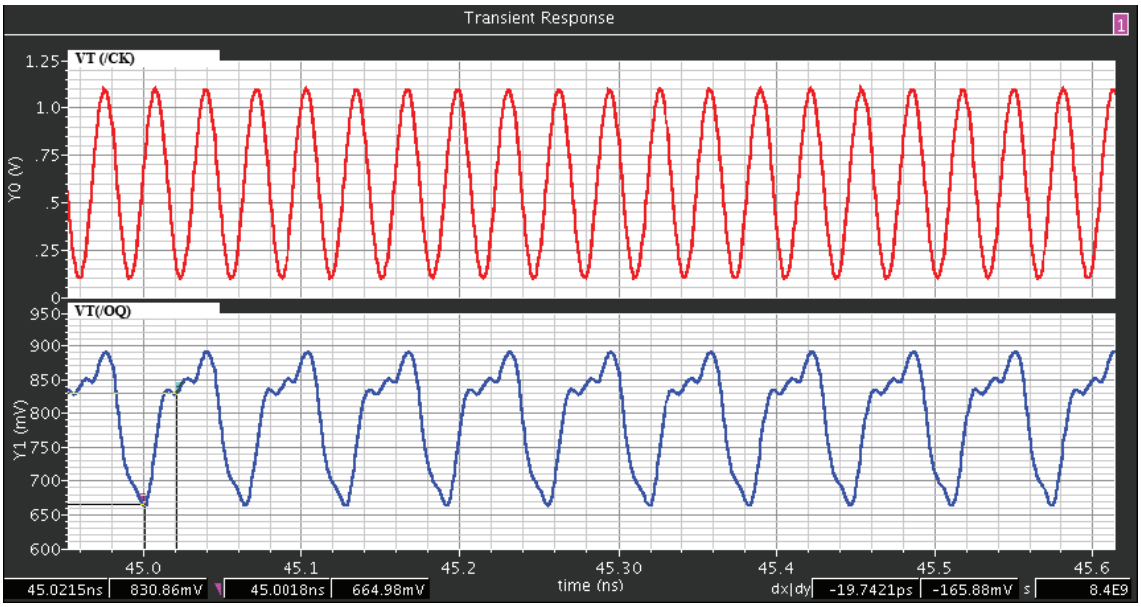

Fig. 4. Post-layout simulation result of the proposed DTC @ 29.6 GHz.

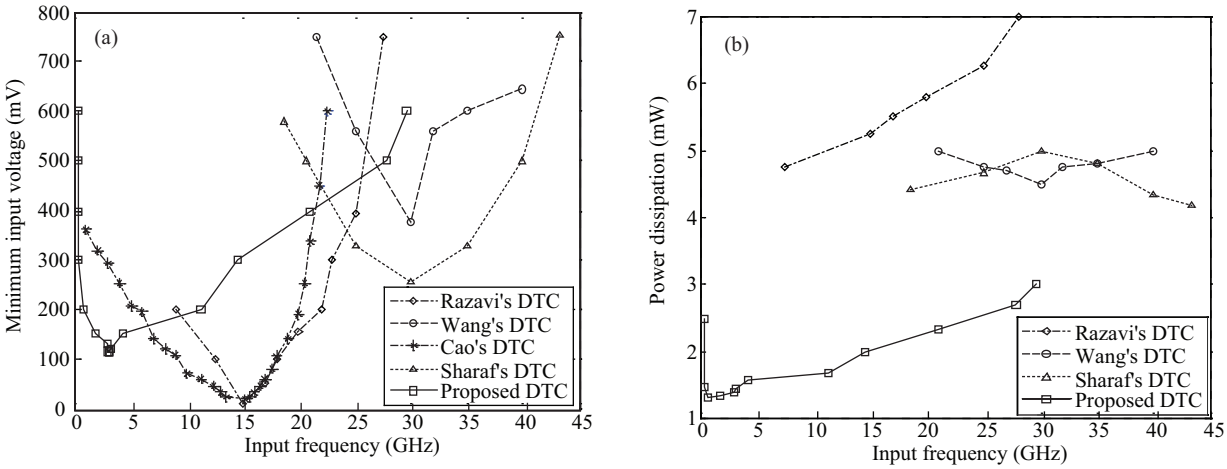

Fig. 5. DTC performance comparisons. (a) Input sensitivity. (b) Power dissipation.

Table 2. Aspect ratios of proposed DTC (units: nm).

Transistor	W/L	Transistor	W/L
M1/M4	4800/130	M5/M6	2200/130
M2/M3	8400/130	M7/M8	9600/130
M9	10400/130	M10	3400/130

(1) Large S_{14} can extend the lower limit of the operating frequency.

(2) Small S_{10} can extend the higher limit of the operating frequency as well as save power.

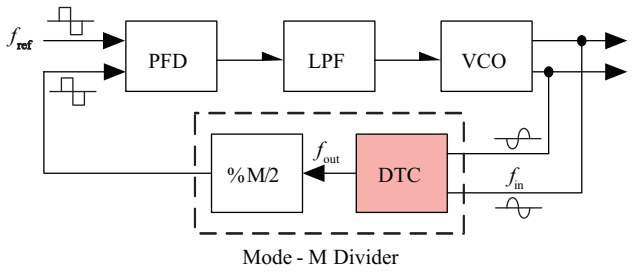

Fig. 6. Block diagram of target PLLs for the proposed DTC.

4. Application case

According to the proposed optimization method, a typical optimal design is shown in Table 1. This is fabricated by a SMIC 0.13 μm 1P8M RF CMOS process with a 1.2 V power supply. Since the proposed DTC covers a large scale of frequency, the layout must be designed as symmetrical as possible (see Fig. 3). Figure 4 gives the post-layout simulation result at the maximum operating frequency. The performance comparisons between the proposed DTC and another three published DTCs are summarized in Table 2, and their input sensitivity and power versus input frequency are sketched in Fig. 5[1, 3, 6, 10].

From Table 3 and Fig. 5, we can see that the proposed DTC has the largest MMFR and a medium minimum input voltage which can drive the circuit into correct function, whereas it

Table 3. Comparisons of the proposed DTC with published DTCs.

DTC	Razavi[1]	Sharaf[6]	Cao[11]	This work
Process	0.1 μm CMOS	0.13 μm CMOS	0.13 μm CMOS	0.13 μm CMOS
Power supply (V)	1.2	1.5	1.5	1.2
Max. operating freq. (GHz)	5	43	22.5	29.6
Min. operating freq. (GHz)	N/A	19	1	0.32
MMFR	N/A	2.3	22.5	92.5
Power consumption (mW)	2.6 @ 5 GHz	4.4 @ 19 GHz, 5.0 @ 43 GHz	1.86 @ 22.5GHz	1.97 @ 360 MHz, 2.71 @ 29.6 GHz

only uses half of the power as consumed by its counterparts.

As two application cases, the proposed DTCs are implemented in two integer phase-locked loops (PLLs) as the foremost blocks of the divider whose inputs are directly from two different VCOs (see Fig. 6). One is fed with a 4224 MHz input frequency, and the other has a 10 GHz input frequency. The experimental results show that the overall in-band phase noise is –94 dBc/Hz @ 10 kHz[8] and –84 dBc/Hz @ 10 kHz, respectively.

5. Conclusions

We have presented a novel ultra-wide frequency range TFF-DTC circuit in SMIC 0.13 μm RF CMOS and an optimization method which strives to illustrate the important aspects of transistor sizing, revealing the complex tradeoffs between power supply, working frequency and power consumption. Both the circuit topology and the optimization method have been favored by the post-layout simulation results, and also partially verified by the experimental results from two integer PLLs which integrated it as the foremost block of their integer dividers to divide 4224 MHz and 10 GHz operating frequencies.

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