Multi-bias capacitance voltage characteristic of AlGaN/GaN HEMT*

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Abstract: The method of multi-bias capacitance voltage measurement is presented. The physical meaning of gate–source and gate–drain capacitances in AlGaN/GaN HEMT and the variations in them with different bias conditions are discussed. A capacitance model is proposed to reflect the behaviors of the gate–source and gate–drain capacitances, which shows a good agreement with the measured capacitances, and the power performance obtains good results compared with the measured data from the capacitance model.

Key words: AlGaN/GaN HEMT; multi-bias CV curves; non-linear; CV model
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1. Introduction

GaN material possesses fundamental electronic properties that make it an ideal candidate for high power, high frequency and high temperature electronic devices[1−3]. Since the demonstration of the first GaN based transistor, rapid progress has been made in the development of GaN-based HEMT devices[4]. The main obstacle to progress has been trap effects and current collapse, as a result of which the large signal model of GaN HEMT is also a sticky issue.

The RF performance of the GaN HEMT is often degraded by a series of physical effects that limit either charge density or charge transport, which are related to the traps in the surface and the interface between the buffer layer and the substrate[5, 6]. Capacitance voltage (CV) characteristics are widely used as a diagnostic tool for semiconductors. In many cases, the CV curves can be directly associated with the impurity of the semiconductor device. The CV measurement can be used to characterize the elastic strain relaxation in the device structure[7], and it has proved to be useful in analyzing interface states, Schottky barriers, threshold voltage characteristic, etc. The CV characteristic also provides more information about the nonlinearity of the device for the large signal model.

The usual CV measurement just applies the voltage to the gate, which is only one bias to get the Schottky barrier capacitance. In this paper, a direct way to measure gate–source capacitance (C_{gs}) and gate–drain capacitance (C_{gd}) is presented. We give the interpretation of the physical meaning of C_{gs} and C_{gd}, and also discuss the variation trend of the capacitances with the bias gate–source voltage (V_{gs}) and drain–source voltage (V_{ds}). New equations are introduced to model C_{gs} and C_{gd}, which gives a good result compared to the measured data.

2. Device structure and fabrication

The layer structure of the device used in this study was grown on a semi-insulation 4H-SiC substrate. The epitaxial layer consisting of a 3 μm unintentionally doped GaN buffer layer, a 1 nm AlN spacer layer, a 25 nm $Al_{0.2}Ga_{0.8}N$ barrier layer, and 3 nm GaN on top. The device was a 0.2 μm gate length and 100 μm (100 × 1) gate width T-shaped AlGaN/GaN HEMT. An averaged electron mobility of 1250 $cm^2/(V{\cdot}s)$ and a sheet carrier density of 1.4×10^{13} cm^{-2} were obtained by room-temperature Hall measurement. The AlGaN/GaN HEMT fabrication commenced with metallizing by high-vacuum evaporation in the drain and source, and the ohmic contacts were formed by depositing the metals Ti/Al/Ti/Au and then carrying out rapid thermal annealing (RTA) at 870 ℃ for 50 s in N_2 ambient. All these steps resulted in a low ohmic contact resistivity of 10^{-6} Ω·cm. After ion implantation, Si_3N_4 film used for passivation was grown by PECVD. A gate recess was etched using a fluorine-based and subsequent chlorine-based ICP process. Then, the T-shaped Schottky gate was formed by Ni/Au evaporation and the subsequent lift-off process. Finally, an Au air bridge was deposited by electroplating in order to connect the source area.

3. Measurement details

The values of C_{gs} and C_{gd} can be obtained from the measured small signal S parameters in different biases, followed by the extraction of C_{gs} and C_{gd} using appropriate algebraic transformations on the measured scattering matrices, the disadvantages of which are the complex calculations and the adjustment of average values in the frequency range with so many bias points. The direct way of measurement is simpler. Multi-bias C_{gs} and C_{gd} on wafer property measurements were performed by an HP4284A LCR meter and an HP6624A power source with a cascade summit 9000 probe station. The HP4284A has five ports, Lc, Lp, Hp, Hc and ground, also with a guard which is the outers of Lc, Lp, Hp, Hc connected together. The high port is the connection of Hp and Hc, while the low port is accounted for by Lp and Lc.

The test block diagram of C_{gs} measurement is shown in

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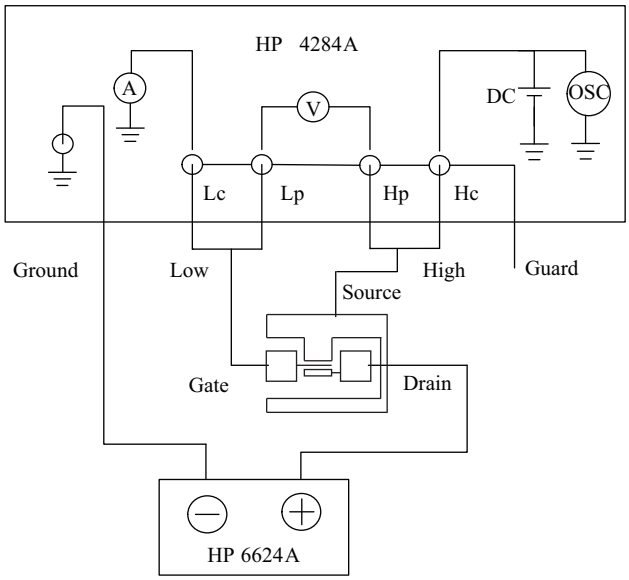

Fig. 1. Test block diagram of gate–source capacitance C_{gs}.

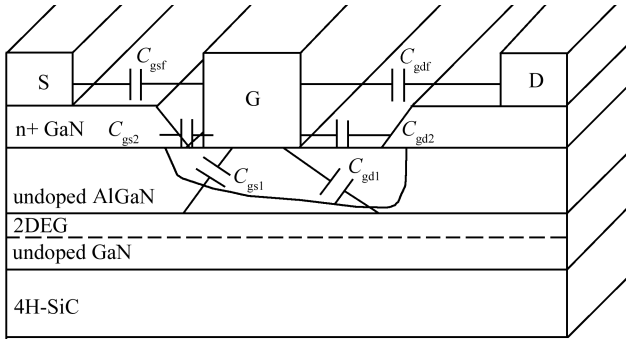

Fig. 2. Schematic diagram of parasitic capacitances in the AlGaN/GaN HEMT.

Fig. 1. The high and low ports of the HP4284A were connected to the source and gate, respectively, to supply V_{gs}, and the drain–gate voltage (V_{dg}) was supported by HP6624A. With the bias changing, C_{gd} could be measured in the same way. Finally, the relative voltage V_{ds} had to be calculated to get the CV curves related to V_{gs} and V_{ds} rather than V_{gs} and V_{dg}. The results would be inaccurate if current flowed through the low port, so the gate was connected to the low port to avoid the influence of current. The device was turned on if V_{gs} was above the threshold voltage. Drain-source current went through the channel when $V_{ds} > 0$. The current had a great impact on the capacitances, especially C_{gd}. In order to avoid trap effects, a frequency of 1 MHz was selected for the internal oscillator of the LCR meter[8].

4. Analysis and results

As depicted in Fig. 2, the cross sectional layout of the given HEMT structure has identified the regions where the parasitic capacitances are located. C_{gsf} and C_{gdf}, the values of which are very small, are interelectrode capacitances between each electrode metallization, and they can be removed by the open de-embeded structure. C_{gs1} depends on the details of the depletion under the gate, mainly coupling the gate to the low-resistivity 2DEG region under the gap between the gate and source. Strictly speaking, it is a distributed capacitance. C_{gs2} is the fringing capacitance between the gate and source metallization effectively extended by the GaN cap layer. C_{gs} lumped as a single element in the equivalent circuit model is composed of C_{gs1}, C_{gs2} and C_{gsf}, and the main part is C_{gs1}.

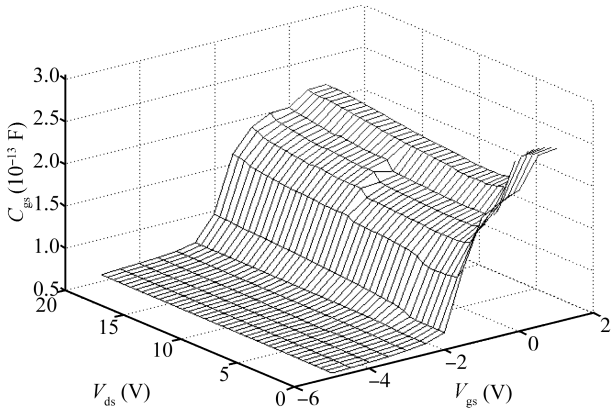

Fig. 3. Measured C_{gs} at various applied bias V_{gs} and V_{ds}.

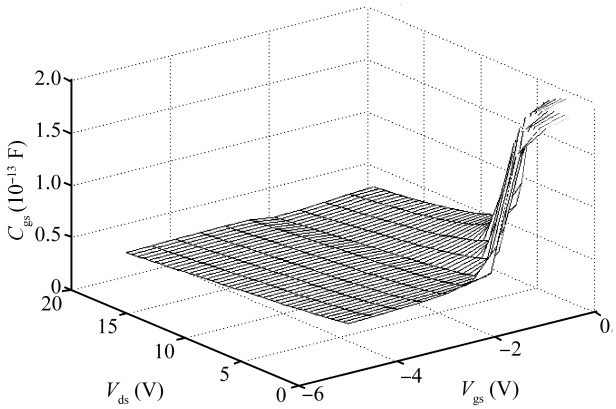

Fig. 4. Measured C_{gd} at various applied bias V_{gs} and V_{ds}.

C_{gd} has a similar composition to C_{gs}. As the main component of C_{gd}, C_{gd1} is associated with the charges in the depletion region at the drain edge of the space–charge layer, primarily generated and modulated by the gate–drain voltage (V_{gd}). C_{gd2} is also the fringing capacitance between the gate and drain metallization extended by the GaN cap layer. C_{gs} and C_{gd} are the rate of change of charge on the gate electrode with respect to V_{gs} and V_{gd}, and all contain three components given by Eqs. (1) and (2), so they may be a little larger than the values extracted by the S parameters.

$$C_{gs} = \left.\frac{\partial Q_g}{\partial V_{gs}}\right|_{V_{gd}=\text{const}} = C_{gs1} + C_{gs2} + C_{gsf}, \quad (1)$$

$$C_{gd} = \left.\frac{\partial Q_g}{\partial V_{gd}}\right|_{V_{gs}=\text{const}} = C_{gd1} + C_{gd2} + C_{gdf}. \quad (2)$$

The capacitance relies on the width of the depleted space–charge region in the device depending on the applied voltage. Figures 3 and 4 show, respectively, the curves of C_{gs}

and C_{gd} at different V_{gs} and V_{ds} biases. It is noted that C_{gs} increases with increasing V_{gs}. When $V_{gs} < -3$ V, the device is pinched off, and the channel layer under the gate electrode is fully depleted, so C_{gs} is only dominated by the width of the depleted region, keeping almost constant[9]. There is a sudden increase around $V_{gs} = -2$ V, because the carriers under the gate begin to travel, the drain–source current is flowing through the channel, then the decrease in the depletion width with more positive V_{gs} results in the rapid increase in C_{gs}, and it can be concluded that the threshold voltage is between –3 and –2 V. C_{gs} just becomes a little larger with increasing V_{ds}, which indicates insensitivity in the depletion at the source edge of the gate.

C_{gd} increases with the increase in V_{gs}, but decreases with the increase in V_{ds}. Except for the fact that the distance from drain to gate is longer than that from source to gate, the HEMT structure is essentially symmetric, so C_{gd} has the same trend as C_{gs}, varying with V_{gs}. The electric field reaches the peak value at the drain edge of the gate, and begins to decrease between the gate and drain. The carrier density falls as the channel height increases beyond the drain end of the gate, which also leads to a fall in charge[10]. As V_{ds} increases, the point of the peak electric field approaches the source edge of the gate. The drain end of the channel is increasingly screened from the variations in gate bias, and C_{gd} gradually decreases with increasing V_{ds}[11]. When the drain–source current is going through the channel, the coupling capacitance induced by the current is superimposed on C_{gd}, which makes the value of C_{gd} much bigger on the working condition of the device. When C_{gd} is modeled, only the values of V_{gs} under the pinch off condition are chosen to make the curve fitting. This point is important.

The hyperbolic tangent function describes the gate and drain voltage dependencies well on the capacitances of GaN HEMT[12], so it is used to model C_{gs} and C_{gd}, as given in Eqs. (3) and (4)

$$C_{gs}(V_{gs}, V_{ds}) = C_{gs0}\left\{1 + \tanh\left[\Psi_1\left(V_{gs}\right)\right]\right\} \times \left\{1 + \Psi_2(V_{gs}, V_{ds}) \tanh\left[\Psi_3\left(V_{ds}\right)\right]\right\}, \quad (3)$$

$$C_{gd}(V_{gs}, V_{ds}) = C_{gd0}\left\{1 + \tanh\left[\Psi_4\left(V_{gs}\right)\right]\right\} \times \left\{1 + \Psi_5(V_{gs}, V_{ds}) \tanh\left[\Psi_6\left(V_{ds}\right)\right]\right\}. \quad (4)$$

C_{gs0} and C_{gd0} are the values of capacitance at V_{gs} = 0 V and V_{ds} = 0 V, on the condition of which discrepancy between C_{gs0} and C_{gd0} is feeble.$\Psi_1$and Ψ_4 are the polynomials of V_{gs}, Ψ_3 and Ψ_6 are the polynomials of V_{ds}, and Ψ_2 and Ψ_5 are the polynomials of V_{gs} and V_{ds} to describe the interaction of each other. The fitting of C_{gs} is given in Fig. 5. C_{gs} is small in the pinch off region, when the channel is turned on, and it begins to increase with the spread of depletion. The model of C_{gs} is accurate when $V_{ds} > 4$ V, but there is a sharp decrease from V_{ds} = 0 V to V_{ds} = 4 V. The knee voltage of the device is around 4 V. As the carriers underneath the gate begin to drift across the channel, the charge rate of the changes in voltage is very fast from the very beginning of V_{ds} is positive, which exhibits a high value of capacitance between the gate and source. Then, the charge rate is slow, and the carriers gradually reach saturation velocity. After the knee voltage, the change in charges with V_{ds} is steady, so the increase in C_{gs} is linear with increasing V_{ds}. For the same reason, there is a great drop in C_{gd} from V_{ds} = 0 V to 3 V. It can be seen that the values of C_{gd} change a bit with V_{gs}, as shown in Fig. 6, and the model gives a good result to the measured C_{gd}. As the current in the channel has a great effect on C_{gd} rather than C_{gs}, the model of C_{gd} just has to fit well under the pinch off condition.

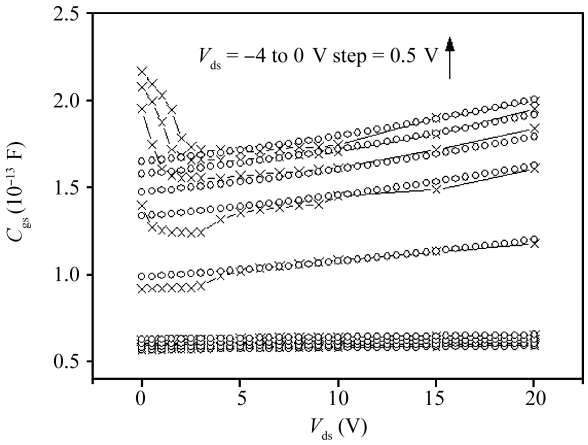

Fig. 5. Fitting of C_{gs}. The cross '×' is the measured data, the circle 'O' is the simulated data.

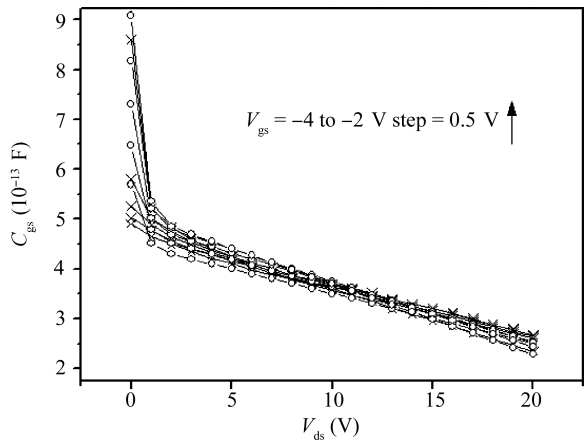

Fig. 6. Fitting of C_{gd}. The cross '×' is the measured data, the circle 'O' is the simulated data.

The relation between capacitance and voltage reflect the charge changes with voltage and microwave signal changes with frequency, which demonstrate the fluctuation with the alternate current signal. In GaN HEMT transistors, the accurate modeling of C_{gs} and C_{gd} can reflect the high frequency performance of the device; especially in predicting f_t and f_{max}. The CV characteristic is important for the device model, and the proposed model appears well suited to reproducing the function of the device. Combined with the Agilent EEHEMT1 current voltage characteristic[13], it is able to insert the model in a complex architecture using small or large signals to implement the nonlinear simulations in the Agilent ADS. The P_{out} and Gain can be obtained in the power sweep simulation with the whole nonlinear model, and the PAE can be calculated with Eq. (5):

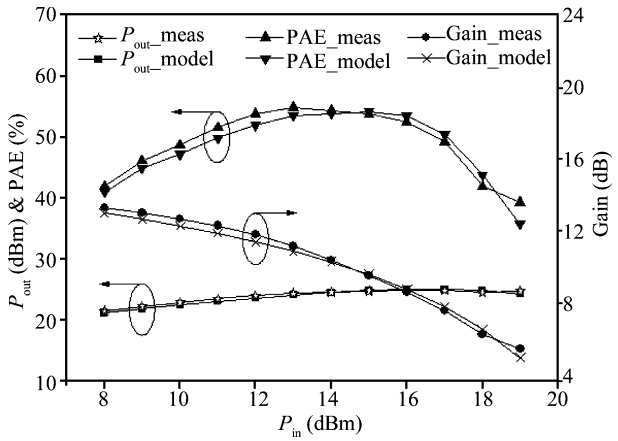

Fig. 7. Comparisons between power measurement and model simulation (V_{gs} = –2 V, V_{ds} = 20 V @ 8 GHz).

$$\mathrm{PAE} = \frac{P_{\mathrm{out}} - P_{\mathrm{in}}}{P_{\mathrm{DC}}} = \frac{P_{\mathrm{out}}}{P_{\mathrm{DC}}}\left(1 - \frac{P_{\mathrm{in}}}{P_{\mathrm{out}}}\right) = \frac{P_{\mathrm{out}}}{P_{\mathrm{DC}}}\left(1 - \frac{1}{\mathrm{Gain}}\right) = \frac{P_{\mathrm{out}}}{I_{\mathrm{ds}}V_{\mathrm{ds}}}\left(1 - \frac{1}{\mathrm{Gain}}\right). \quad (5)$$

Comparisons between the power measurements and simulation results obtained with the proposed capacitance model are shown in Fig. 7. The differences in P_{out} and Gain between measured and simulated data are about ±0.5 dB. The discrepancy of PAE between measured and simulated data is about ±5%, which is within an acceptable parameter range. It also gives good evidence for the capacitance model used in the non-linear simulation.

5. Conclusion

The multi-bias C_{gs} and C_{gd} are measured in a direct way. With the analysis of the physical meaning of the capacitances, the capacitance model is demonstrated to reflect the variations in the capacitance with V_{gs} and V_{ds}. It can be seen that the fittings of C_{gs} and C_{gd} are good compared to the measured capacitances, especially under high drain voltage. The comparisons between the power performance and the model simulation validate the approximation of the proposed capacitance model.

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