Negative bias temperature instability induced single event transient pulse narrowing and broadening*

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Abstract: The effect of negative bias temperature instability (NBTI) on a single event transient (SET) has been studied in a 130 nm bulk silicon CMOS process based on 3D TCAD device simulations. The investigation shows that NBTI can result in the pulse width and amplitude of SET narrowing when the heavy ion hits the PMOS in the high-input inverter; but NBTI can result in the pulse width and amplitude of SET broadening when the heavy ion hits the NMOS in the low-input inverter. Based on this study, for the first time we propose that the impact of NBTI on a SET produced by the heavy ion hitting the NMOS has already been a significant reliability issue and should be of wide concern, and the radiation hardened design must consider the impact of NBTI on a SET.

Key words: negative bias temperature instability; single event transient; narrowing and broadening
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1. Introduction

Negative bias temperature instability (NBTI) has become one of the most serious reliability concerns for highly scaled PMOS among the various reliability issues in modern CMOS technology[1−3]. The degradation mainly results from the depassivation of the Si–H bonds at the Si/SiO_2 interface in a 130 nm bulk silicon CMOS process[4]. At the same time, the radiation induced single event transient (SET) has also become a significant reliability issue with the circuit technology scaling down. It is predicted that by 2011, the soft error rate (SER) due to SETs will be comparable to the one due to single event upset (SEU)[5].

For the integrated circuits that need to operate for a very long time in a space radiation environment, long term reliability issues such as NBTI should be considered in addition to radiation induced reliability. The threshold voltage (V_{th}), saturated current and other important electrical parameters of the PMOS will be degraded over time due to NBTI, and this degradation can change the response of the devices to single event effects (SEEs).

With increasing pulse width of the SET, the SER also increases because the probability of latching the SET as a soft error is in direct proportion to the pulse width. If the pulse width is broadening with NBTI stress time, the SER induced by the SET is also increasing with time, and the probability of system failure also increases in the later periods of the space mission. So the pulse width of the SET is a very important factor in evaluating the reliability of the system, and it is very important to understand the impact of NBTI on the pulse width for the radiation hardened design.

The effect of the radiation induced total ionizing dose (TID) effects on NBTI, hot carrier injection (HCI) and time dependent dielectric breakdown (TDDB) has already been widely studied and produced many interesting results. A TID is found to enhance NBTI induced degradation, and these devices have much worse degradation than either irradiation or NBTI alone[6]; TID is shown to negatively affect the HCI degradation during subsequent hot carrier injection, and HCI degradation is more serious for annular NMOS than 2-edged one after radiation[7, 8]; TID is also shown to cause a small but measurable increase in TDDB lifetime at the worst-case irradiation bias[9]. The effect of radiation induced SEE on TDDB has also been studied, showing that heavy ion strikes reduce the TDDB lifetime on ultra-thin gate oxides[10]. These studies provided valuable information to predict the lifetime for long term use devices. To our best knowledge, there has still been no investigation into the effect of NBTI on SET, which may also provide valuable information for radiation hardened design.

In this paper, we will investigate the effect of NBTI on SET produced in an inverter based on 3D TCAD simulations. The heavy ion will hit the PMOS for the high-input inverter and the NMOS for the low-input inverter, a "0-1-0" SET pulse and a "1-0-1" SET pulse will produce at the output, and a SET pulse will narrow and broaden with time due to NBTI degradation, respectively. The simulation results will be presented and the mechanism will be discussed.

2. Simulation setup

The circuit used in the simulations is an inverter, as shown in Fig. 1(a); an ideal 5 fF capacitor is connected to the output. When the heavy ion hits the NMOS, the input of the inverter is held at ground, and the output voltage of the inverter keeps at the supply voltage V_{dd} ($V_{dd} = 1.2$ V in the simulations), after the heavy ion striking on the drain of the NMOS, a "1-0-1" SET pulse will be produced at the output. Similarly, when the heavy ion hits the PMOS in the high input inverter, a "0-1-0" SET pulse will be produced at the output.

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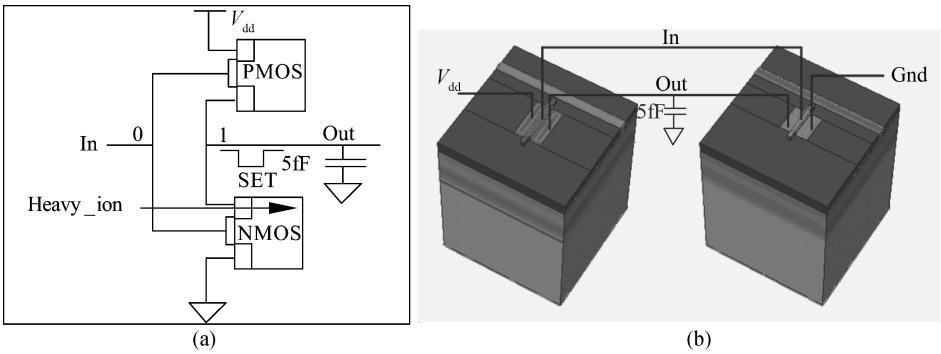

Fig. 1. Structure used in the simulations. (a) Circuit. (b) 3D numerical model.

Both the PMOS and NMOS are modeled with a 3D numerical model, as shown in Fig. 1(b). The widths/lengths of the devices are 1.28 μm/0.13 μm for the PMOS and 0.84 μm/0.13 μm for the NMOS, respectively. The devices used in our simulations are calibrated to SMIC 0.13 μm logic 1P8M Salicide process.

A Sentaurus TCAD_C_2009.06-SP2 from Synopsys is adopted in our work to perform structure construction and device simulation. The ion impact is simulated using the Sentaurus device-heavy-ion module[11]. An electron.-hole pair column is created in the devices, and the LET of the ion used in the simulations is 50 MeV·cm^2/mg and 5 MeV·cm^2/mg to produce the SET with and without full amplitude, respectively. The value is kept constant along the heavy ion track, and the length and the radius of the track are 4.5 μm and 0.1 μm, respectively. The ion is assumed to strike the center of the drain of the devices at normal incidence, and does not consider the effect of the incidence angle.

In the simulations, the Shockley-Read-Hall and Auger models are used for carrier recombination and generation, the band-gap narrowing model is used for intrinsic carrier concentrations, and the doping-dependent, band-gap narrowing, carrier-carrier-scattering and high-field models are used for mobility, and the hydrodynamic model is used for the carrier transport equation.

The produced donor interface traps have been added into the Si/SiO_2 interface of the PMOS to simulate the donor interface traps produced by NBTI stress. The simulation method is the same as the one used in Ref. [12], and has been proved to be able to achieve results consistent with the experimental results of Reddy[12].

A wide range of trap densities is simulated, and the density of the interface traps (N_{it}) is obtained from Eq. (1)[13]. Figure 2 shows the relationship between N_{it} and time; the parameters used in the calculations are consistent with those used in Refs. [4, 13], and the value of the parameters is calibrated to produce results consistent with Ref. [12], which gives a few experimental results of N_{it} based on a 130 nm bulk silicon CMOS process under a special NBTI stress condition; and for another process or NBTI stress condition, the value of the parameters can also be extracted by the experiments based on the target process and target NBTI stress conditions. The interface traps corresponding to different NBTI stress times are added into the Si/SiO_2interface of the PMOS; the modeling assumes that the distribution of the donor interface traps is equally spaced

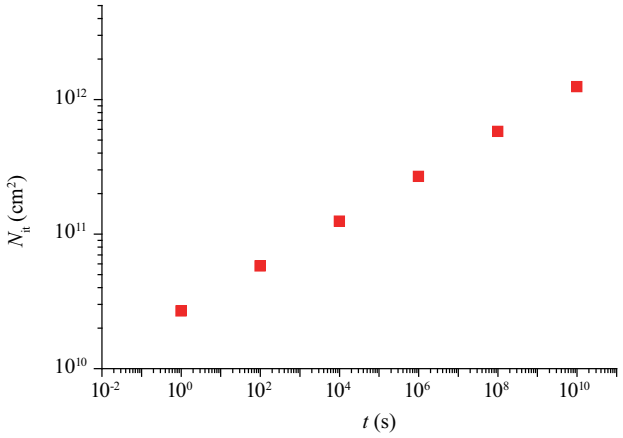

Fig. 2. Density of the interface traps versus NBTI stress time.

within the bandgap, located at the Si/SiO_2 interface, and uniformly placed across the length of the channel. Then the heavy ion strikes the center of the drain of the PMOS/NMOS to produce the SET pulse.

$$\Delta N_{it} = \left(\frac{k_H}{k_{H_2}}\right)^{1/3} \left(\frac{k_f N_0}{k_r}\right)^{2/3} (6D_{H_2}t)^{1/6}. \quad (1)$$

3. Results and discussion

3.1. Hits the PMOS in the high-input inverter

Figure 3 shows SET pulse waveforms at different NBTI stress times after the heavy ion striking the drain of the PMOS in the high-input inverter. The results show that the SET pulse is almost uncharged with time at low LET conditions. However, NBTI results in the SET pulse narrowing at high LET conditions, and the pulse width will narrow by 2.2% after 3 years (10^8 s).

In the simulations, the electrical parameters of the NMOS are almost unchanged with time, so the pulse narrowing is independent of the NMOS.

As shown in Fig. 4, after a heavy ion striking the drain of the PMOS, numerous electron–hole pairs are generated along the ion track. Holes can be collected quickly by the drain. However, the ionizing electrons will disturb the electric potential of the well and turn on the "source–channel–drain" parasitic P^+NP^+ bipolar transistor, and the source will inject holes into

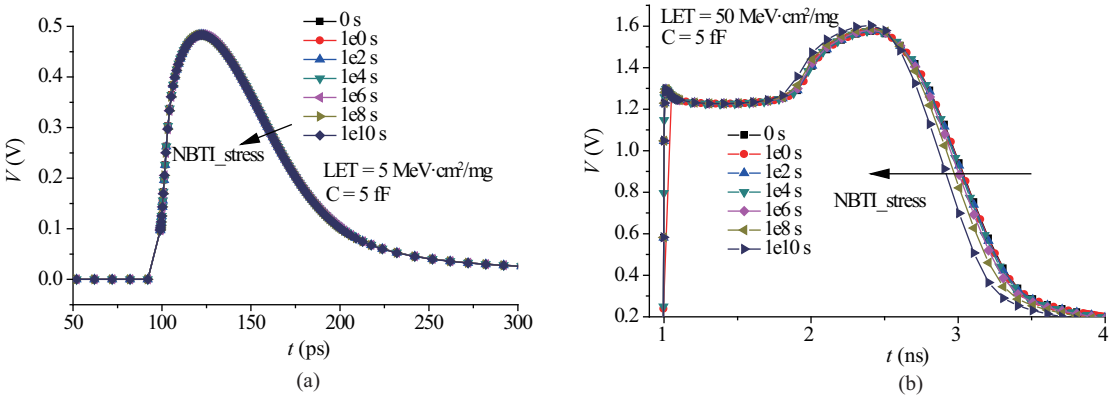

Fig. 3. SET pulse waveforms at different times. (a) Low LET. (b) High LET.

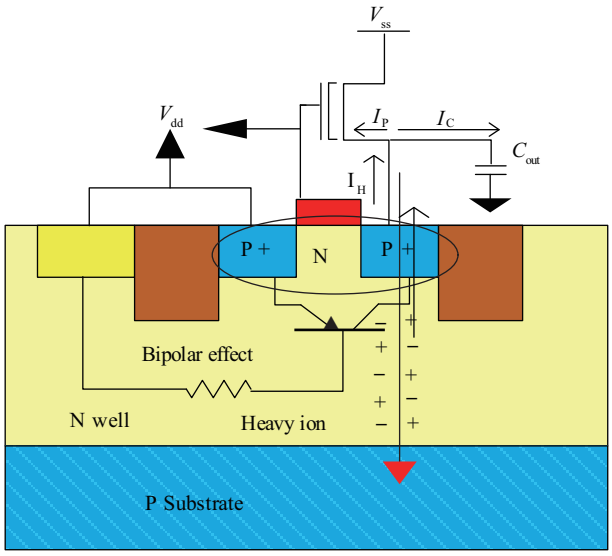

Fig. 4. Physical mechanism of the charge collection.

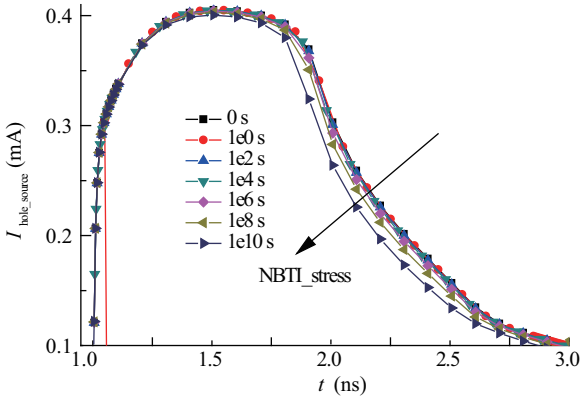

Fig. 5. Source injected hole current waveforms of the PMOS at different times.

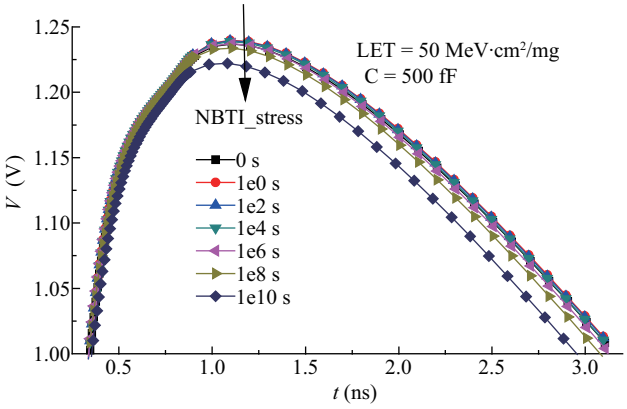

Fig. 6. SET pulse waveforms at different times.

the channel. These holes can pass through the channel and be collected at the drain, where they add to the original ion-induced holes and can cause increased charge collection. This is the well-known bipolar amplification effect.

In the channel region, the carriers are subjected to scattering by Si/SiO_2 interface phonons and interface roughness[11]. The channel mobility degradation caused by these effects will increase with increasing N_{it}, as shown in Eq. (2)[17], where K is an empirical constant, $K = (7.0 \pm 1.3) \times 10^{-13}$. The channel mobility will decrease with increasing N_{it}, so the hole current passing through the channel will decrease with time.

$$\mu_r = \frac{\mu_0}{1 + k\Delta N_{it}}. \quad (2)$$

When the LET is too low to ionize enough electrons to disturb the well potential, the parasitic P^+NP^+ bipolar transistor will not turn on, so the bipolar amplification effect will not affect the produced SET pulse, and further the pulse will be almost unchanged with time, as shown in Fig. 3(a). However, when the LET is high enough to turn on the parasitic P^+NP^+ bipolar transistor, the bipolar amplification effect will affect the produced SET pulse, and with the weakening of the bipolar amplification effect, the pulse width of SET with full amplitude will decrease with time, as shown in Fig. 3(b). Figure 5 further shows the corresponding source injected hole current waveforms of the PMOS at different times; the injected hole current is actually decreasing with time, and it also verifies that the weakening of the bipolar amplification effect is the main reason for the pulse narrowing. And under high SET conditions, the pulse amplitude of the SET without full amplitude will also decrease due to the weakening of the bipolar amplification effect, as shown in Fig. 6. In the simulations, the LET

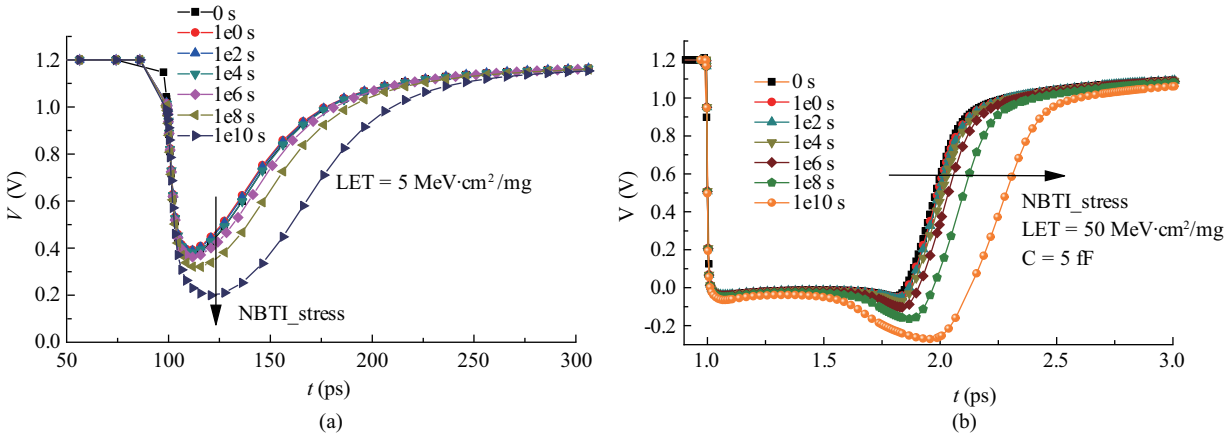

Fig. 7. SET pulse waveforms at different times. (a) Low LET. (b) High LET.

is the same as 50 MeV·cm^2/mg, but the capacitor connected to the output is 500 fF to produce the SET, which cannot appear at full amplitude. The results show that, when the LET is high enough to turn on the parasitic bipolar transistor, the amplification effect will significantly affect the pulse waveform of the SET. With the weakening of the bipolar amplification effect, the pulse width or amplitude will decrease with time for the SET with or without full amplitude.

3.2. Hits the NMOS in the low-input inverter

Figure 7 shows SET pulse waveforms at different NBTI stress times after the heavy ion striking the drain of the NMOS in the low-input inverter. When the LET is low enough and the full amplitude disappears, the pulse amplitude will increase with time, and the amplitude will increase by 6.1% after 3 years (10^8 s). When the LET is high enough and the full amplitude appears, the pulse width of the SET will increase with time, and the width will broaden by 9.6% after 3 years (10^8 s). The results show that the amount of broadening is already been comparable to the initial SET pulse after a few years (such as 3 years). The impact of NBTI on the pulse width of the SET has already been a significant reliability issue and should be of wide concern.

Due to NBTI degradation, $V_{\rm th}$ of the PMOS can increase with time, and the time dependent $V_{\rm th}$ degradation based on the power law of time. Alam et al established a series of analytical models for NBTI induced $V_{\rm th}$ degradation, and these models have been successfully used to calculate NBTI induced temporal performance degradation of digital circuits[14] and the critical electrical parameters degradation of SRAM array[15]. In DC stress conditions, $V_{\rm th}$ degradation follows a power law of time as follows[13],

$$\Delta V_{\rm th}(t)_{\rm DC} = (1 + {\rm m}_{\mu})\frac{q\Delta N_{\rm it}(t)}{C_{\rm ox}} = K_{\rm DC}t^{1/6}. \quad (3)$$

The saturated current of the PMOS ($I_{\rm dsat}$) can be approximately represented as[14]

$$I_{\rm dsat} \approx \frac{W_{\rm eff}\mu_{\rm eff}C_{\rm ox}}{L_{\rm eff}}(V_{\rm gs} - V_{\rm th})^{\beta}. \quad (4)$$

Then we can give the expression between a change in $I_{\rm dsat}$ and $V_{\rm th}$,

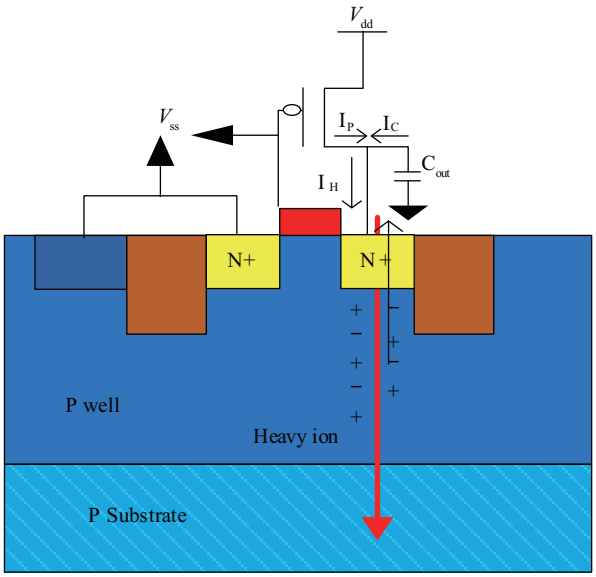

Fig. 8. Physical mechanism of the charge collection.

$$\frac{{\rm d}I_{\rm dsat}}{I_{\rm dsat}} = -\beta\frac{{\rm d}V_{\rm th}}{V_{\rm gs} - V_{\rm th}}. \quad (5)$$

Integrating it, we get

$$\int_{I_{\rm dsat0}}^{I_{\rm dsat0}-\Delta I_{\rm dsat}}\frac{{\rm d}I_{\rm dsat}}{I_{\rm dsat}} = -\beta\int_{V_{\rm th0}}^{V_{\rm th0}+\Delta V_{\rm th}}\frac{{\rm d}V_{\rm th}}{V_{\rm gs} - V_{\rm th}}, \quad (6)$$

$$\ln\left(1 - \frac{\Delta I_{\rm dsat}}{I_{\rm dsat0}}\right) = \beta\ln\left(1 - \frac{\Delta V_{\rm th}}{V_{\rm gs} - V_{\rm th0}}\right), \quad (7)$$

where $V_{\rm th0}$ is the threshold voltage before NBTI degradation, and $I_{\rm dsat0}$ is the corresponding saturated current of the PMOS. Using Taylor series expansion on both sides of Eq. (7) and neglecting the higher order terms, we get

$$\frac{\Delta I_{\rm dsat}}{I_{\rm dsat0}} \approx \beta\frac{\Delta V_{\rm th}(t)_{\rm DC}}{V_{\rm gs} - V_{\rm th0}} = LK_{\rm DC}t^{1/6}. \quad (8)$$

At the same time, the linear current of the PMOS ($I_{\rm dlin}$) can also be approximately represented as[16]

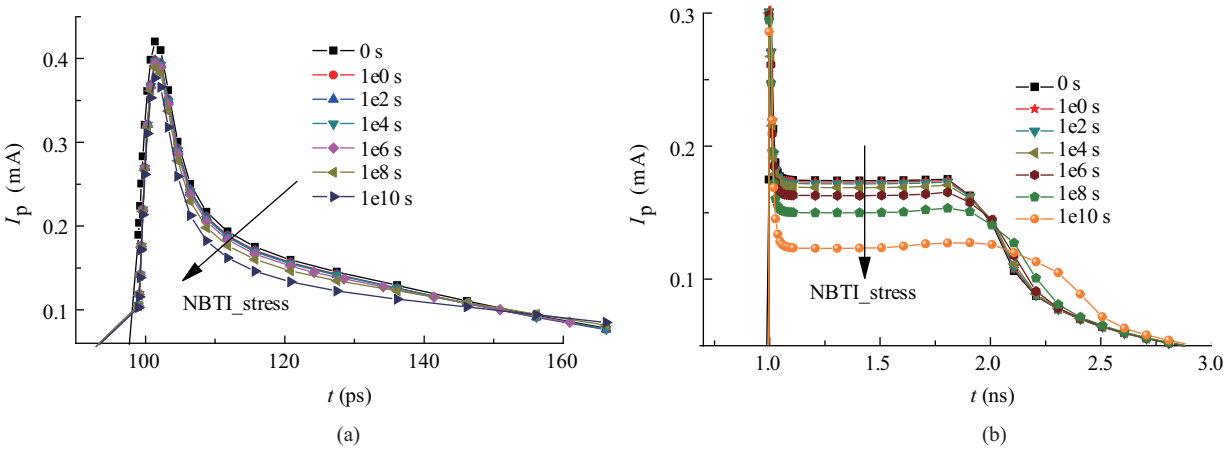

Fig. 9. Drain current waveforms of the PMOS at different times. (a) Low LET. (b) High LET.

$$\frac{\Delta I_{\rm dlin}}{I_{\rm dlin0}} \approx \frac{\Delta V_{\rm th}(t)_{\rm DC}}{V_{\rm gs}-V_{\rm th0}} = K_{\rm DC}t^{1/6}. \quad (9)$$

As expressed by Eqs. (8) and (9), $I_{\rm dsat}$ and $I_{\rm dlin}$ are degraded with time due to NBTI.

As shown in Fig. 8, in the process of charge collection, there is $I_{\rm H} = I_{\rm P} + I_{\rm C}$. At low LET conditions, the PMOS works in the linear region ($I_{\rm P} = I_{\rm dlin}$). As shown in Fig. 9(a), the degradation of $I_{\rm dlin}$ will result in the increasing of $I_{\rm C}$, and further disturb the potential of the output, so the pulse amplitude will increase with time, as shown in Fig. 7(a). When the LET is high enough and the plateau region appears, the PMOS works in the saturated region ($I_{\rm P} = I_{\rm dsat}$). As shown in Fig. 9(b), the saturated current of the plateau region decreases and the duration of the plateau region broadens with NBTI stress time. The pulse width of the SET is mainly determined by the duration of the plateau region, and then it broadens with the broadening of the plateau region.

4. Conclusion

The effect of NBTI on SET has been studied in a 130 nm bulk silicon CMOS process based on 3D TCAD simulations. The investigation shows that NBTI can induce the pulse width and amplitude of the SET narrowing when a heavy ion hits the PMOS in the high-input inverter. The weakening of the bipolar amplification effect is the main reason for the pulse narrowing. However, NBTI can induce the pulse width and amplitude of the SET broadening when a heavy ion hits the NMOS in the low-input inverter. The degradation of $I_{\rm dlin}$ and $I_{\rm dast}$ is the main reason for the pulse broadening. The investigation shows that the impact of NBTI on the SET produced by the heavy ion hitting the NMOS has already been a significant reliability issue compared to hitting the PMOS, and the radiation hardened design must consider the effect of NBTI on the SET.

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